A Low-Power 28-Gb/s PAM-4MZM Driver With Level Pre-Distortion

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***Abstract*—We present a PAM-4 optical modulator driver for Mach-Zehnder modulator (MZM), having the level pre-distortion functionality so that the ratio of level mismatch (RLM) can be optimized. The driver employs a newly proposed PAM-4 stacked source-series terminated (SST) structure with impedance control so that it can provide high output voltage swing with low power consumption. A prototype chip including data generators and serializers is fabricated in 28-nm CMOS technology with 0.016 mm^2 active chip area. With this, 28-Gb/s operation is achieved with 2.4 V differential output swing and 3.14 pJ/bit energy efficiency. It is experimentally demonstrated that our circuit can achieve larger than 95% RLM for a commercial $LiNbO_3$ MZM PAM-4 modulation.**

***Index Terms*—PAM-4, optical transmitter, MZM, SST driver, RLM, high-swing driver, impedance matching.**

I. Introduction

AS THE amount of data transmission required for many wireline interface applications continuously increases, the multi-level signaling technique such as Pulse Amplitude Modulation 4 (PAM-4) has become the technical solution of choice for overcoming the wireline bandwidth limitation [1]. In addition, there is a growing interest for employing optical interconnect solutions based on Si photonics for demanding applications such as data center interfaces. For these applications, PAM-4 Si photonic transceivers have been actively investigated [2]–[5]. Since direct modulation of the optical source is not possible in Si photonics, it is essential to have high-performance electro-optical (EO) modulators along with low-power electrical drivers. Presently, various types of Mach-Zehnder modulators (MZMs) are widely used due to its high bandwidth and reliable operation [6]. As the MZM utilizes the interference of phase-shifted optical signals for modulation, its optical output has raised-cosine dependence on the applied voltages as [7]

$$P_{out} = IL \cdot P_{in} \cdot \frac{1}{2} \cdot \left[1 + \cos(\pi \frac{V_{in}}{V_\pi} + \Delta\phi)\right], \quad (1)$$

where P_{in} and P_{out} are the input and output optical power, respectively, IL is the insertion loss, $\Delta\phi$ represents the phase difference between two MZM arms due to length or bias difference, V_{in} is the applied voltage, and V_π is the required voltage to have phase difference of π for the optical signals. Due to this non-linear characteristics, the modulated optical PAM-4 signals can have the degraded ratio for level mismatch (RLM) defined as [8]

$$RLM(\%) = 100 \times \frac{3V_{\min}}{V_{peak-to-peak}}, \quad (2)$$

where $V_{\min}$ is the amount of minimum eye opening and $V_{peak-to-peak}$ is the peak-to-peak amplitude of the outer eye, when the MZM is driven with equally spaced electrical signal levels. RLM is a key performance matrix for PAM-4 transmitters, where the minimum required RLM value is at least 95% in many applications [9], [10]. As an example, Fig. 1(c) shows the simulated eye-diagrams of 28-Gb/s PAM-4 MZM output when driven by electrical signals shown in Fig. 1(b). The simulated MZM is modeled from the measured DC shown in Fig. 1(a) and S21 (E-O) characteristics of a commercial 40GHz C-band MZM (Fujitsu FTM7939EZ [11]). Even though the operating point is biased at the quadrature point, which is the most linear operating point, the middle eye is slightly larger than top and bottom eyes due to MZM nonlinearity and this results in RLM of 87%. The smaller RLM corresponds to smaller eye opening among three different eye openings and results in the worse BER for PAM4 signals. Consequently, a PAM-4 driver which has the level pre-distortion functionality is of great importance for realizing PAM-4 optical transmitters having high RLM values.

There have been several reports for PAM-4 optical drivers [3], [12]–[15]. In [3], [14] and [15], the non-linear characteristics of EO modulators are compensated by driver circuits. In particular, [3] and [14] use CML drivers with which MSB, LSB signal amplitude can be controlled. However, CML drivers consumes a large amount of static power with 50Ω impedance matching. However, CML drivers

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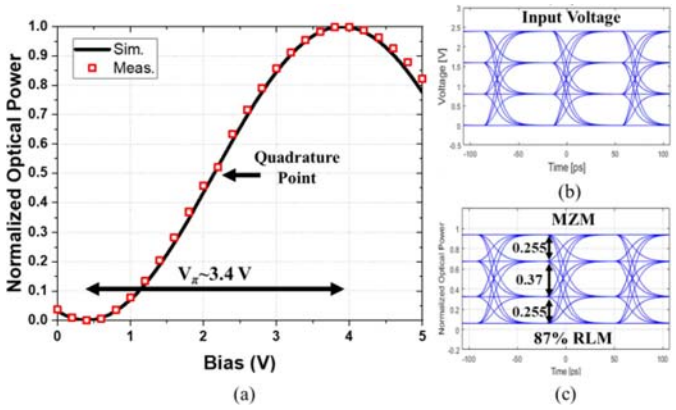


Fig. 1. (a) Measured and simulated MZM transfer curve, and (b) input PAM-4 signal for simulation and (c) MZM output PAM-4 signal.

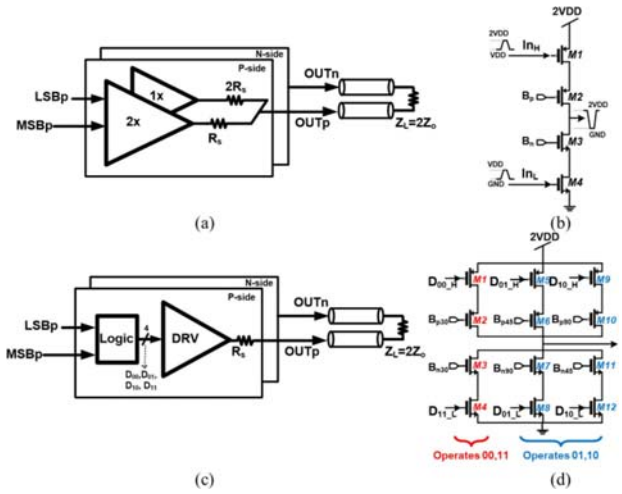


Fig. 2. Block diagram and schematic of (a), (b) conventional PAM-4 SST driver and (c), (d) proposed PAM-4 SST driver.

consumes a large amount of static power with 50Ω impedance matching. CML driver with open drain output would have smaller power consumption [16], [17], but their performance strongly depends on any interconnect parasitics, which is undesirable for many applications. A voltage-mode driver is used in [15] for low-power consumption, but MSB and LSB drivers are segmented to control the level distortion resulting in large power consumption. In this brief, we propose a new type of optical modulator driver circuit structure, in which a stacked source-series-terminated (SST) structure is employed for achieving low-power and high-swing operation. In addition, in our circuit, the analog impedance control can be achieved for impedance matching with low-power consumption even with PAM-4 level pre-distortion.

This brief is organized as follow. In Section II, the structure and implementation of the proposed level pre-distortion PAM-4 SST driver is described, and the impedance control scheme is explained. In addition, detailed transmitter circuit structures are given. Section III discusses the measurement results of the fabricated chip for 28-Gb/s PAM-4 operation. Section IV gives the conclusion.

II. PAM-4 Transmitter Structure

SST drivers for PAM-4 modulation have been used for low-power consumption and high-speed operation [18].

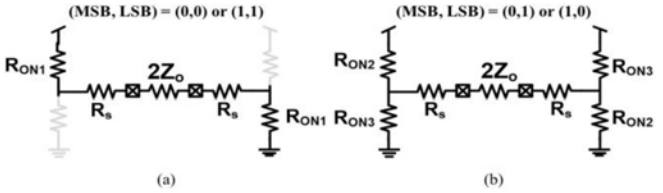


Fig. 3. Simplified schematic for impedance of the proposed driver circuit.

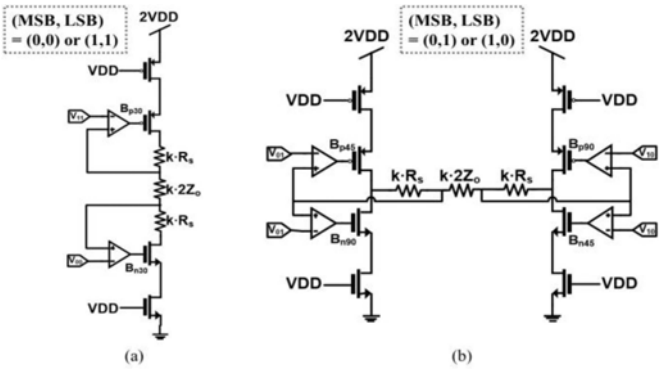


Fig. 4. Replica circuits for impedance control.

Fig. 2(a) shows the block diagram of the conventional PAM-4 SST driver. For the LSB path, both series resistance and the inverter-based driver are twice as large as those in the MSB path, making MSB signal twice as large as the LSB signal. Since modulator drivers usually require large output swing voltages typically over 2V, twice large supply voltage ($2V_{DD}$) is used. Fig. 2(b) shows the schematic of the conventional PAM-4 high swing inverter-based driver where $M_{2,3}$ MOSFETs are stacked to prevent breakdown. In_H signal is level-shifted from the original signal In_L, and B_p and B_n are the bias voltages for the impedance matching of the driver. Both B_p and B_n are connected to MSB and LSB drivers at the same time. But this structure cannot only tune the middle eye (01 and 10 level) of the PAM-4 signal since the amplitude change of MSB or LSB signal affects 00 and 11 levels. Therefore, we propose a new SST PAM-4 driver structure, with which only 01 and 10 levels can be changed.

The schematic of the proposed driver is shown in Fig. 2 (c) and (d). Pulsed signals (D_{00_L}, D_{01_L}, D_{10_L}, D_{11_L}) are generated whose low value is GND and high value V_{DD} for PAM4 output data 00, 01, 10, and 11, respectively. For the PMOS transistor operation, level-shifted pulsed signals (D_{00_H}, D_{01_H}, D_{10_H}, D_{11_H}) are generated by inverting D_{00_L}, D_{01_L}, D_{10_L}, D_{11_L} and adding V_{DD}. The operation of the driver can be separated into two parts: (00, 11) and (01, 10). These pulsed signals can be easily achieved with CMOS NANDs and NOR gates acting on MSB and LSB signals. As shown in Fig. 2(d), M_{1-4} transistors operate only when PAM-4 data are 00 or 11, but other M_{5-12} transistors operate only when data are 01 or 10. The bias voltages (B_{p30}, B_{p45}, B_{p90}, B_{n30}, B_{n45}, B_{n90}) are controlled so that the transistors have the adequate turn-on resistance, and their values are automatically generated by the replica circuits. Our driver has 24.6ps, 24.7ps rise- and fall-time.

Fig. 3 shows the simplified picture representing the impedance of the proposed driver circuit during different

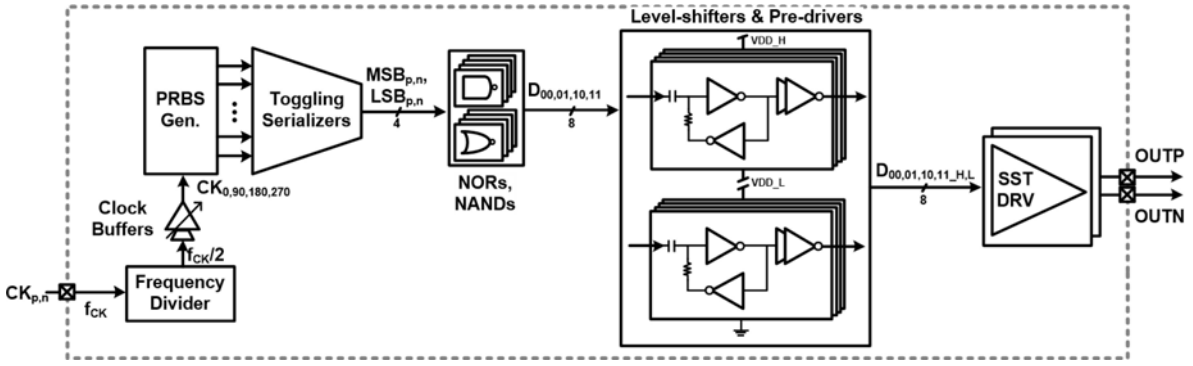


Fig. 5. Block diagram of proposed 28-Gb/s PAM-4 MZM Transmitter.

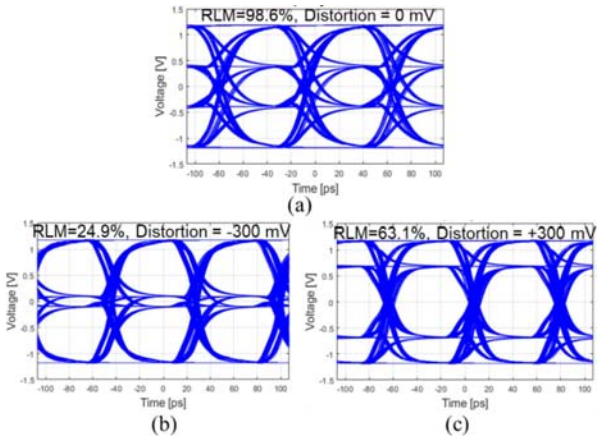


Fig. 6. Post-layout simulation results of the transmitter for 28-Gb/s PAM-4 operation with different pre-distortion levels.

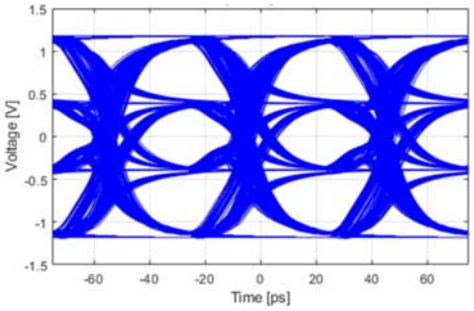


Fig. 7. 40Gbps simulation result of the driver with ideal load.

operations. Fig. 3(a) is the case when PAM-4 data are 00 or 11, so the sum of turn-on resistances of M_{1-2} or M_{3-4} transistors (R_{ON1}) and series resistances (R_s) should be Z_o. In the same way, $R_{ON2} \parallel R_{ON3} + R_s$ should be Z_o in Fig. 3(b). Different values for R_{ON2} and R_{ON3} cause current flow producing the voltage across the load impedance. With R_s chosen as 20Ω in our design, the value of R_{ON1}, R_{ON2}, and R_{ON3} is 30Ω, 45Ω, 90Ω, respectively, with a condition that R_{ON3} is twice larger than R_{ON2} by transistor sizing. To achieve these turn-on resistances, a replica circuit shown in Fig. 4 is used. Fig. 4(a) shows the replica circuit for (00,11) operation in which B_{p30}, B_{n30} provide the bias for 30Ω turn-on resistances (R_{ON1}) with 27dB loop gain. Fig. 4(b) shows the replica circuit for (01,10) operation in which B_{p45}, B_{n45}, B_{p90}, B_{n90} provide the bias for 45Ω, 90Ω turn-on resistances (R_{ON2} and R_{ON3}) with 45dB loop gain. For low-power consumption, the scaling factor (k) is chosen as 16 in this design, and the size of transistor is also scaled with a factor of 16. By controlling V_{10} and V_{01}, the desired PAM-4 output levels for 01 and 10 can be achieved.

Fig. 5 shows the overall architecture of the proposed transmitter. With quadrature-phase clocks, 8 × 3.5-Gb/s parallel PRBS31 data are generated. A 4:1 toggling serializer, which does not require clock signals and thus achieving low-power consumption [19], is used for generating 14-Gb/s MSB and LSB data. Serialized MSB and LSB data are connected to four NANDs and four NORs to generate D_{00}, D_{01}, D_{10}, D_{11} and go through latch-based level-shifters having VDD_H for $2V_{DD}$ and VDD_L for V_{DD}. SST drivers then provide 2.4V peak-to-peak swing as differential signaling with the supply voltage of 2.4V ($2V_{DD}$) and 100Ω load impedance. The supply voltage of 1.2V is higher than the nominal value of 1.0V for 28nm CMOS technology. This is necessary due to the large modulation voltage required for the MZM with which we test our driver. The post-layout simulation results for generated 28-Gb/s PAM-4 signals having 2.4V swing are shown in Fig. 6(a). With 300mV distortion of the reference level (V_{10} or V_{01}), the amplitude of the middle eye can be decreased or increased by the amount of 600mV as can be seen in Fig. 6(b) and (c), respectively. With the ideal load of 100 Ohm termination and 40GHz bandwidth, 40 Gb/s operation is possible as shown by the post-layout simulation result in Fig. 7.

III. Measurement Results

A prototype 28-Gb/s PAM-4 optical modulator driver is implemented in 28-nm CMOS technology. The fabricated chip microphotograph is shown in Fig. 8. The active chip area is 0.016mm^2. Fig. 9 shows the measured eye diagrams for the driver at 10-Gb/s and 28-Gb/s operation. For the measurement, a 10dB attenuator is used for oscilloscope protection. The measured output voltage swing shows amplitude of 748mV, which with 10dB attenuation corresponds to 2.37V amplitude for full swing. The measured eyes at 10-Gbs/s clearly show the level pre-distortion achieved. The reference level can be tuned up to ±300mV where the middle eye amplitude changes up to 800mV±600mV with 2.4V output swing. The driver operates

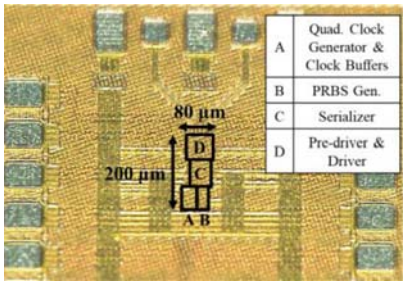


Fig. 8. Fabricated chip microphotograph.

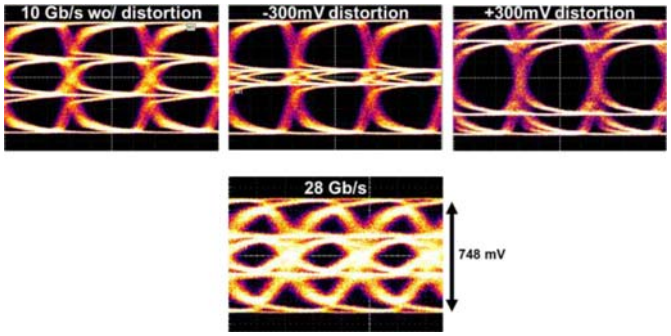


Fig. 9. Electrical measurement results for 10-, 28-Gb/s operation with different pre-distortion levels with 10dB attenuation.

successfully with this tuning capability up to 28-Gb/s with 748mV amplitude with 10dB attenuation. Fig. 10 shows the measured reflection coefficients (S11) at out (+) port without any input and the simulated differential reflection coefficients for different levels with 300mV reference level distortion. For the measurement, the driver output is set at 00 level since both MSB and LSB data are latched to GND when the data generator block is turned off. The measurement results agree well with the simulated results for 00 or 11 output level. 11 output level should provide the same reflection coefficients as 00 output level with or without distortion since the circuit structure is identical for both cases and the distortion is decoupled from the output level. For output levels of 10 or 01, S11 measurement is not possible as our circuit does not allow setting the output at the desired level. The simulated results for these show larger reflection coefficients due to PMOS and NMOS resistance changes caused by the level shift but they are below the minimum value required by the standard mask [9], [10].

For optical measurement, a set-up shown in Fig. 11(a) is used in which a laser source generates 3dBm input optical power for a commercial MZM (Fujitsu FTM7939EZ) driven by our driver. In addition, as shown in Fig. 11(b) on-board probing is used for high-speed I/O's so that the bonding wire effect can be minimized while low-speed I/O's are wire-bonded to pads on PCB and connected to cables. The modulated optical signal is converted to the electrical signal by a commercial optical receiver having 23-GHz bandwidth, and observed by a 20-GHz digital sampling oscilloscope. Fig. 12 shows the measured eyes. For 28-Gb/s operation, the measured eye-diagram was compared with the simulated eye-diagram to estimate BER, which was less than 2.5×10^{-5} satisfying the FP4-FEC threshold (2.4×10^{-4}). At 10-Gb/s

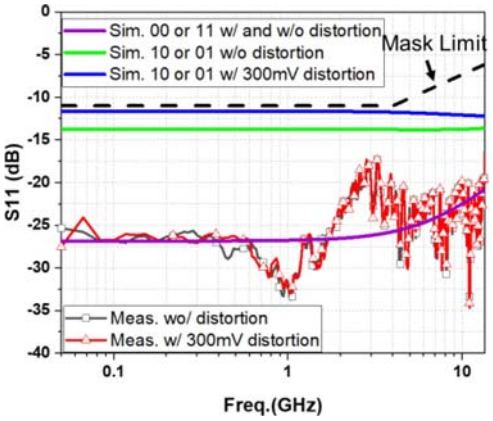


Fig. 10. Measured and simulated reflection coefficient (S11) for different level pre-distortions.

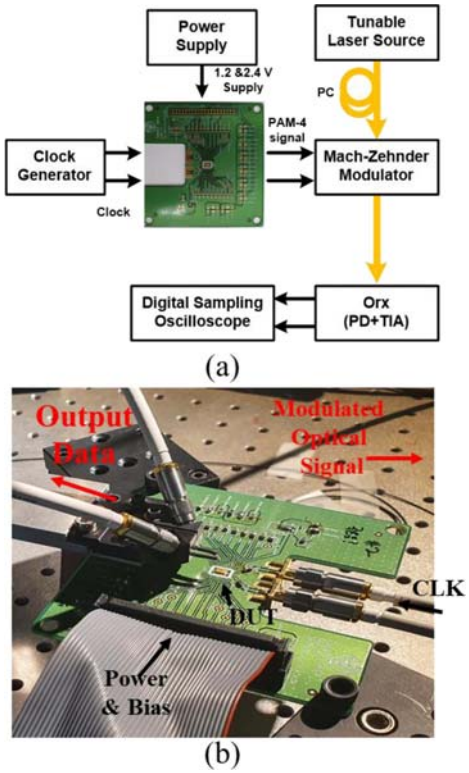


Fig. 11. (a) Block diagram and (b) photo of measurement setup for optical MZM transmission.

without any pre-distortion, the measured modulated optical eye shows 86% RLM. However, with −70mV reference level pre-distortion, RLM of 96.4% is achieved. Peaking in the eye diagram is believed due to the fact that our optical receiver has a peaked frequency response at around 12GHz. At 28-Gb/s, the MZM eyes can be optimized with 70mV level distortion, where the RLM is measured with output levels determined with the histogram provided by the oscilloscope. The degradation for measured optical eyes compared to electrical eyes is due to non-optimal performance of the optical receiver used in our measurement.

Fig. 13 shows the power consumption breakdown where the total power consumption is 115.02mW for 28-Gb/s operation

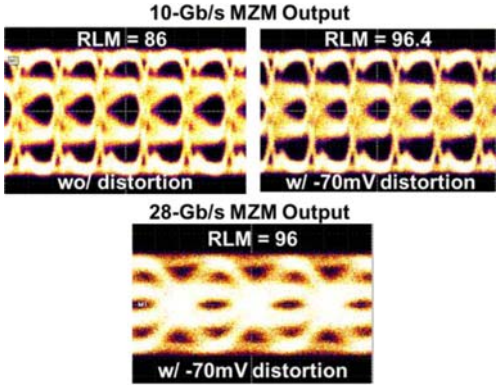
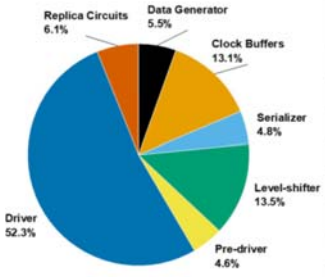


Fig. 12. Measured MZM output for 10-,28-Gb/s operations.



Circuit Block	Power (mW)
Data generator	6.3
Clock buffers	15.12
Serializer	5.56
Level-shifter	15.57
Pre-driver	5.27
Driver	60.19
Replica circuit	7.01
Total	115.02

Fig. 13. Power breakdown of the proposed transmitter.

TABLE I
PERFORMANCE COMPARISON FOR MZM DRIVERS

	[12]	[13]	[15]	[3]	This Work
Technology	130nm CMOS	65nm CMOS	16nm CMOS FinFET	90nm CMOS SOI	28nm CMOS
Data rate	20 Gb/s	36 Gb/s	56 Gb/s	56 Gb/s	28 Gb/s
Data Format	PAM4	PAM4	PAM4	PAM4	PAM4
MZM Type (Integration)	SiPh SEMZM (Wire-bond)	SiPh TWMZM (Wire-bond)	SiPh SEMZM (3D Integration)	SiPh TWMZM (Monolithic)	TWMZM (Cable)
RLM Optimization	No	No	Yes	Yes	Yes
Supply	1.2V, 2.4V	2.4 V	0.9V, 1.8 V	1.2 V	1.2V, 2.4V
Driver Topology	CML	VML	VML	CML	SST VML
Output Swing	2 V_{pp}	2.4 V_{pp}	1.8V_{pp}	2.16 V_{pp}	2.4 V_{pp}
Driver Power	290 mW	236 mW	708 mW*	268.8 mW	88.04 mW
Energy Efficiency (pJ/bit)	14.5	6.55	12.64*	4.8	3.14
Area (mm^2)	1.5 (Entire Die)	0.11	Not Reported	Not Reported	0.016 (Active area), 2.03 (Entire Die)

*Including PLL

and 88.04mW excluding data generator, serializer, and clock blocks. Table I shows the performance comparison of our results with previously reported MZM drivers. Our driver consumes the smallest amount of power with SST drivers and analog impedance calibration. The achieved maximum data rate is smaller than other works for our driver, which is due to significant bandwidth degradation of probe, attenuators, cables, and oscilloscope (totally 12-GHz bandwidth) used in our measurement set-up, not by the intrinsic characteristics of our driver. This bandwidth limitation can be overcome by feedforward equalization (FFE) or inductive peaking equalization.

IV. CONCLUSION

A 28-Gb/s PAM-4 optical modulator driver with SST driver for low power consumption is demonstrated in 28-nm CMOS technology. The driver provides level pre-distortion operation to compensate the non-linear characteristic of the MZM so that the RLM of the MZM output is achieved over 96% with pre-distortion of the signal.

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