Check for updates

Research Article Vol. 31, No. 9 / 24 Apr 2023 / Optics Express 13798

Optics EXPRESS

Single-photon avalanche diode fabricated in standard 55 nm bipolar-CMOS-DMOS technology with sub-20 V breakdown voltage

WON-YONG HA,[1] EUNSUNG PARK,[2,3] DOYOON EOM,[2,3] HYO-SUNG PARK,[2,3] DANIEL CHONG,[4] SHYUE SENG TAN,[4] MICHELLE TNG,[4] ELGIN QUEK,[4] CLAUDIO BRUSCHINI,[1] EDOARDO CHARBON,[1] WOO-YOUNG CHOI,[3,5] AND MYUNG-JAE LEE[2,6]

[1] *Institute of Microengineering, EPFL, Neuchâtel 2002, Switzerland*
[2] *Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology (KIST), Seoul 02792, Republic of Korea*
[3] *Department of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, Republic of Korea*
[4] *GLOBALFOUNDRIES Singapore Pte. Ltd., 60 Woodlands Industrial Park D Street 2, 738406, Singapore*
[5] *wchoi@yonsei.ac.kr*
[6] *mj.lee@kist.re.kr*

Abstract: This paper presents a single-photon avalanche diode (SPAD) in 55 nm bipolar-CMOS-DMOS (BCD) technology. In order to realize a SPAD having sub-20 V breakdown voltage for mobile applications while preventing high tunneling noise, a high-voltage N-well available in BCD is utilized to implement the avalanche multiplication region. The resulting SPAD has a breakdown voltage of 18.4 V while achieving an excellent dark count rate of 4.4 cps/μm^2 at the excess bias voltage of 7 V in spite of the advanced technology node. At the same time, the device achieves a high peak photon detection probability (PDP) of 70.1% at 450 nm thanks to the high and uniform E-field. Its PDP values at 850 and 940 nm, wavelengths of interest for 3D ranging applications reach 7.2 and 3.1%, respectively, with the use of deep N-well. The timing jitter of the SPAD, full width at half maximum (FWHM), is 91 ps at 850 nm. It is expected that the presented SPAD enables cost-effective time-of-flight and LiDAR sensors with the advanced standard technology for many mobile applications.

© 2023 Optica Publishing Group under the terms of the Optica Open Access Publishing Agreement

1. Introduction

Single-photon avalanche diodes (SPADs) are promising sensor devices enabling single-photon and time-of-flight (ToF) detection, and therefore they have a wide range of applications such as light detection and ranging (LiDAR), space navigation, three-dimensional (3D) face recognition and tracking, fluorescence correlation spectroscopy (FCS), ToF positron emission tomography (PET), etc. [1,2]. In particular, SPADs fabricated in a complementary metal-oxide- semiconductor (CMOS) technology have received a great amount of attention for the applications mentioned above because of their low-cost fabrication and monolithic integration capability. Moreover, with the CMOS scaling, a SPAD-based sensor can provide more functionalities with many transistors, while the fill factor of the SPAD is maximized. Using an advanced CMOS technology also offers an additional benefit to a sensor, in terms of power consumption. This is because advance technology is designed to be more power-efficient than older one, by providing high doped layers with less defects. This can be especially important for sensors in mobile applications that need to operate on a limited power source.

To develop a SPAD in advanced CMOS technology, there have been some attempts using 40~65 nm nodes [3–6], however, these SPADs show a high dark count rate (DCR), and a low photon detection probability (PDP), because of the reduced depletion width caused by the

#485424 https://doi.org/10.1364/OE.485424
Journal © 2023 Received 10 Jan 2023; revised 24 Feb 2023; accepted 17 Mar 2023; published 11 Apr 2023

Optics EXPRESS

increased doping concentration with the node scaling. One solution to overcome the performance degradation with the CMOS scaling is utilizing bipolar-CMOS-DMOS (BCD) technology, as it provides lower-doped layers compared to other CMOS technology. In addition, one can improve the PDP performance further with higher excess bias voltage, since high-voltage transistors are available in BCD. Recently, a BCD-SPAD achieving low DCR and high PDP has been reported by using a deep P-well/buried N-well junction [7], but the high breakdown voltage (V_{BD}) over 30 V is a high price to pay as many mobile applications prefer a SPAD having sub-20 V V_{BD}.

In this paper, we present a SPAD based on a shallow junction fabricated in 55 nm BCD technology. We conducted a technology computer-aided design (TCAD) simulation to check the E-field profile of the device at above its V_{BD} and characterized it in terms of I-V, light emission test (LET), DCR, afterpulsing probability (APP), PDP, and timing jitter. With these, we demonstrate that the proposed BCD-SPAD achieves low DCR and high PDP while confining its V_{BD} under 20 V.

2. Device structure and simulation

Figure 1 shows the proposed SPAD structure in 55 nm BCD technology. The SPAD is based on a shallow junction consisting of P + and high-voltage N-well (HVNW) with a deep N-well (DNW) underneath. Thanks to the low-doped HVNW, the device can prevent tunneling noise and improve its PDP, and by utilizing the DNW, it can further enhance its long-wavelength efficiency. The SPAD is designed and fabricated in a circular shape to alleviate the high E-field at the edge of the junction, and P-epi guard ring is implemented at the outside of the junction to prevent the premature edge breakdown. The diameter of the active junction and guard-ring width are 10 µm and 2 µm, respectively.

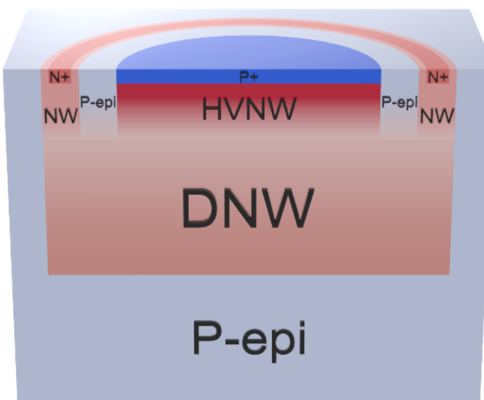


Fig. 1. Cross-sections of the BCD-SPAD.

To verify the effect of the guard ring, TCAD Sentaurus is used to simulate the E-field profile of the SPAD, and the results are shown in Fig. 2. It clearly shows that the premature edge breakdown is effectively prevented by the P-epi guard ring because its doping concentration is much less than the P + layer, and consequently, the E-field is uniformly formed in the intended planar junction between P + and HVNW.

Optics EXPRESS

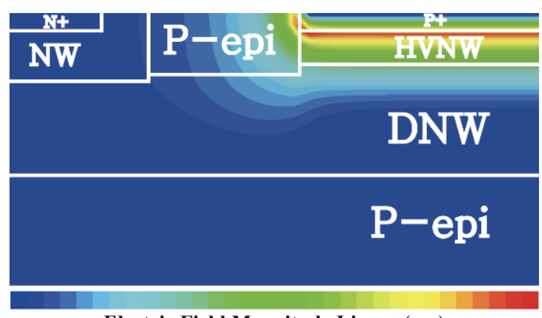


Fig. 2. E-field profiles of the BCD-SPAD at above its breakdown voltage.

3. Experimental results

The I-V characteristics of the SPAD with and without illumination were investigated with a device parameter analyzer and the results are depicted in Fig. 3. The V_{BD} of the SPAD is about 18.4 V achieving sub 20 V_{BD}.

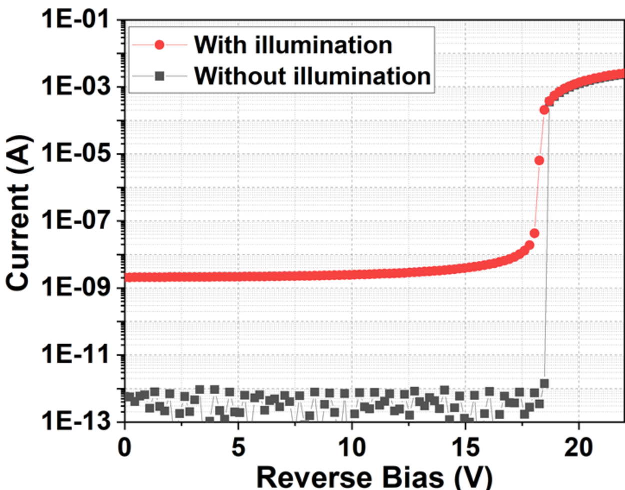
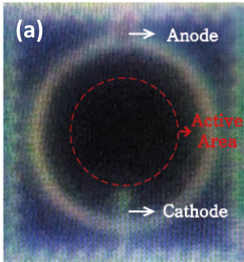


Fig. 3. I-V characteristics for the CMOS-SPAD under dark and illumination conditions.

LET was conducted in order to check the absence of the premature edge breakdown and the device active area as shown in Fig. 4 [8]. As the area emitting light is regarded as the avalanche region, Fig. 4(b), obtained at the excess bias voltage (V_{EX}) of 3 V, clearly demonstrates that a higher E-field than the critical E-field is uniformly formed at the junction of the SPAD, which corresponds well to the result of TCAD simulation shown in Fig. 2.

DCR characteristics were measured with an external passive quenching resistor of 100 kΩ and an oscilloscope, and the results are plotted in Fig. 5. During the measurement, the recharge time of the SPAD was about 1.3 µs. The DCR increases with V_{EX} because the increasing E-field with high V_{EX} enhances the avalanche breakdown probability and the carrier generation rate [9]. Although the SPAD is based on a shallow junction fabricated in an advanced technology node, it achieves excellent DCR performance thanks to the low-doped HVNW available in the BCD technology. It enables a wider depletion region and consequently prevent tunneling noise more effectually. The DCR of the SPAD is just 0.03 cps/µm^2 at $V_{EX} = 1$ V, and it shows a low DCR of

4.4 cps/μm^2 even at $V_{EX} = 7$ V. The inset of Fig. 5 shows measured DCR values at $V_{EX} = 7$ V with 9 different dies and it implies that the DCR uniformity is good.



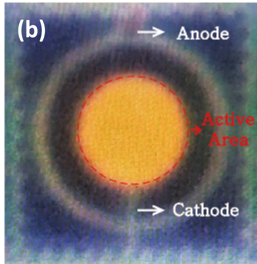


Fig. 4. Results of light emission test of the BCD-SPAD: (a) before V_{BD} and (b) at $V_{EX} = 3$ V.

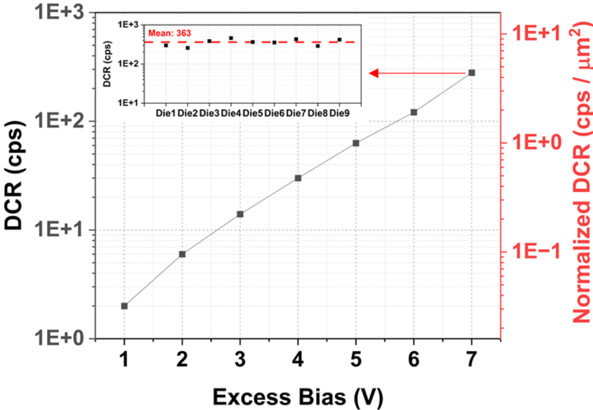


Fig. 5. DCR of the BCD-SPAD vs. V_{EX} at room temperature. The inset shows the SPAD DCR values at $V_{EX} = 7$ V obtaiend from 9 dies.

The DCR characteristics of the BCD-SPAD at different temperatures from -25 to 75 °C were investigated using a temperature chamber as shown in Fig. 6(a). It reveals that the DCR has a higher temperature dependence as the temperature increases. In order to analyze the dominant mechanisms of the DCR at the temperature conditions, activation energies were extracted from the Arrhenius plot as can be seen in Fig. 6(b). The activation energies indicate that trap-assisted thermal generation becomes the primary contributor to the SPAD DCR at above room temperature while tunneling is the main contributor at below room temperature.

The afterpulsing characteristics of the proposed device were checked using the inter-avalanche time histogram method as shown in Fig. 7 [8]. In the measurement, inter-avalanche time statistics were collected at $V_{EX} = 7$ V, with the dead time of 300 ns using an external quenching circuit. The APP of SPAD was estimated as 0.77% when the dead time is 300 ns.

PDP characteristics of the SPAD were measured from 400 to 950 nm at V_{EX} of 1, 3, 5, and 7 V as shown in Fig. 8. Since the afterpulsing phenomenon can result in the overestimation of the PDP values, its afterpulsing probability was already checked as shown in Fig. 7, which confirms that the PDP values were not affected by the afterpulsing. The PDP curves show ripples due to the interference when the light passes through the dielectric layers that have different refractive indices on the top of the SPAD [10]. The peak PDP of the SPAD is 70.1% at 450 nm. Although the PDP decreases as wavelength increases, as many photons are absorbed in the deeper region than in the shallow junction of the SPAD, the PDP in NIR still shows a considerable value, e.g.,

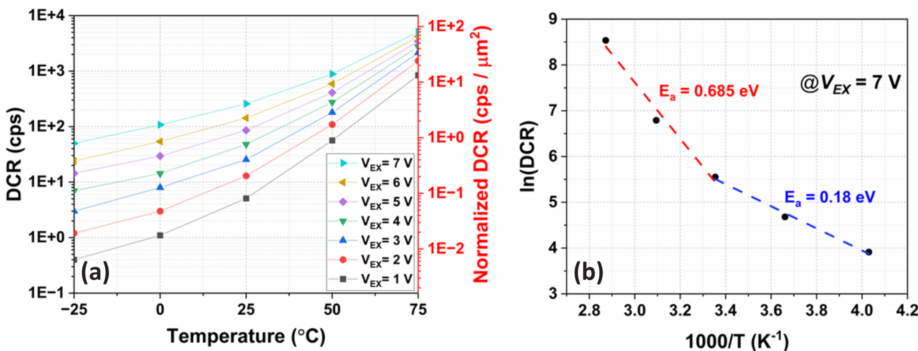


Fig. 6. (a) DCR vs. temperature characteristics of the BCD-SPAD at different V_{EX} and (b) Arrhenius plot of the BCD-SPAD at $V_{EX} = 7\,V$.

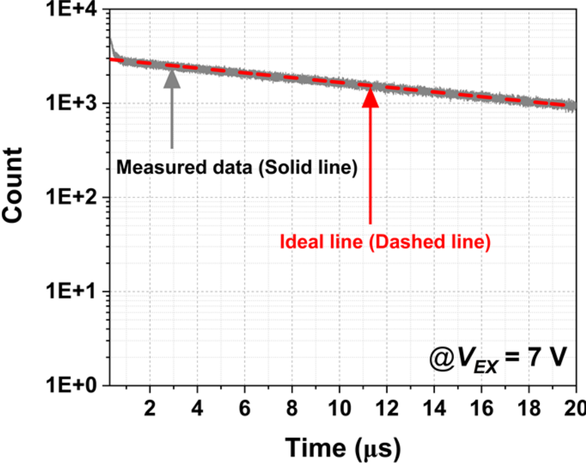


Fig. 7. Inter-avalanche time histogram of the BCD-SPAD.

PDP of 7.2 and 3.1% at 850 and 940 nm, respectively, where many 3D ranging technologies are interested in.

Timing jitter indicates the uncertainty of the time response of the SPAD, i.e., the uncertainty between actual and measured photon arrival time [11]. It was measured using the time-correlated single-photon counting (TCSPC) technique with an 850 nm picosecond pulsed laser when the repetition rate is 20 MHz and the V_{EX} is 7 V. To accurately measure the inter-arrival time between the laser pulse and SPAD pulse, an oscilloscope having high bandwidth and high sample rate was utilized. The measurement results are shown in Fig. 9. It achieves excellent timing jitter performance, 91 ps full width at half maximum (FWHM) and 224 ps full width at tenth maximum (FWTM), including the jitter of the laser and laser driver.

Table 1 shows the performance summary of the proposed BCD-SPAD and comparison with previously reported SPADs fabricated in advanced CMOS technology. Thanks to the BCD technology, the proposed SPAD achieves much better performance in terms of DCR, timing jitter, peak PDP, and PDP at 940 nm when compared to the SPADs fabricated in 40 nm and 65 nm CMOS technology [3–6]. Especially, it is notable that the proposed SPAD shows much lower DCR and much higher PDP compared to the CMOS-SPADs. When it comes to the comparison with the other BCD-SPAD based on a deep junction [7], the proposed SPAD achieves higher peak PDP, while showing comparable DCR. Although the previous BCD-SPAD shows higher

Optics EXPRESS

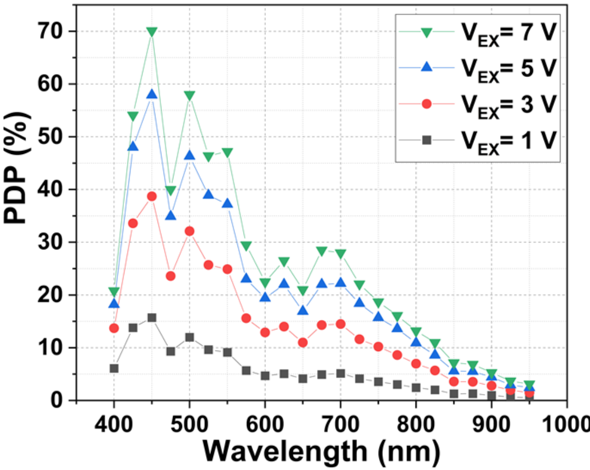


Fig. 8. PDP of the BCD-SPAD.

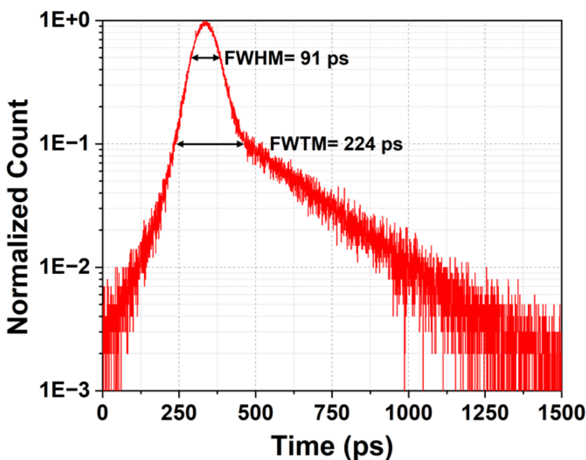


Fig. 9. Timing jitter of the BCD-SPAD.

PDP at 940 nm, the difference is not significant. Most of all, the proposed device has a great advantage in terms of the low V_{BD}, which is the crucial difference that makes the proposed SPAD more favorable in mobile applications. In other words, the proposed SPAD is the most optimized device for low-power applications among recently reported SPADs fabricated in advanced CMOS technology.

Table 1. Performance summary and comparison with CMOS-SPADs

	This Work	[3]	[4]	[5]	[6]	[7]
Technology	55 nm BCD	65 nm CMOS	40 nm CMOS	65 nm CMOS	65 nm CMOS	55 nm BCD
Active Junction	P+/HVNW	N+/PW	PW/DNW	PW/DNW	N+/PW	DPW/BNW
Guard Ring	P-epi GR	Modified NW	Virtual GR & STI	Less-doped NW	NW	Virtual GR
Active Area	63.6 μm^2	64 μm^2	n/a	2.8 μm^2	100 μm^2	60.8 μm^2
V_{BD}	18.4 V	9.1 V	n/a	9.6 V	9.52 V	31.5 V
V_{EX}	7 V	0.25 V	1 V	2 V	0.3 V	7 V
Normalized DCR	4.4 cps/μm^2	2.4 kcps/μm^2	n/a	285.7 cps/μm^2 [a]	138 kcps/μm^2	2.6 cps/μm^2
PDP peak @ Wavelength	70.1% @ 450 nm	5.5% @ 425 nm	45% @ 500 nm	9.2% @ 480 nm	2.1% @ 440 nm	62% @ 530 nm
PDP at 940 nm @ V_{EX}	3.1% @ 7 V	0.3% @ 0.25 V	3% @ 1 V	n/a	0.2% @ 0.3 V	4.2% @ 7 V
Timing Jitter (FWHM) @ λ, V_{EX}	91 ps @ 850 nm, 7 V	235 ps @ 637 nm, 0.4 V	140 ps @ 840 nm, 1 V	224 ps [b] @ 485 nm, 2 V	197 ps @ 685 nm, 0.3 V	52 ps @ 780 nm, 3 V

[a] Calculated using Fig. 3 of [5].
[b] Laser jitter is excluded.

4. Conclusion

This work presents a high-performance SPAD fabricated in 55 nm BCD technology. The proposed SPAD achieves a low DCR of 4.4 cps/μm^2 at $V_{EX} = 7$ V. It attains a peak PDP of 70.1% and PDP of 7.2 and 3.1% at 850 and 940 nm, respectively, at the same V_{EX}. In addition, the SPAD achieves a good timing jitter, 91 ps FWHM at 850 nm. All the performance is obtained while confining its breakdown voltage under 20 V, which can open the way for SPAD sensors to be utilized in many mobile applications.

Funding. Korea Institute of Science and Technology (2E32242).

Acknowledgments. This work was supported by the Korea Institute of Science and Technology (KIST) Institution Program (Grant No. 2E32242).

Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

References

1. F. Zappa and A. Tosi, "MiSPIA: microelectronic single-photon 3D imaging arrays for low-light high-speed safety and security applications," Proc. SPIE **8727**, 87270L (2013).
2. M.-J. Lee and E. Charbon, "Progress in single-photon avalanche diode image sensors in standard CMOS: From two-dimensional monolithic to three-dimensional-stacked technology," Jpn. J. Appl. Phys. **57**(10), 1002A3 (2018).
3. E. Charbon, H. J. Yoon, and Y. Maruyama, "A Geiger mode APD fabricated in standard 65 nm CMOS technology," in *International Electron Devcies Meeting* (IEEE, 2013) pp. 27.5.1–27.5.4.
4. S. Pellegrini, B. Rae, A. Pingault, D. Golanski, S. Jouan, C. Lapeyre, and B. Mamdy, "Industrialised SPAD in 40 nm Technology," in *International Electron Devcies Meeting* (IEEE, 2017) pp. 16.5.1–16.5.4.
5. X. Lu, M. Law, Y. Jiang, X. Zhao, P. Mak, and R. P. Martins, "A 4-μm Diameter SPAD Using Less-Doped N-Well Guard Ring in Baseline 65-nm CMOS," IEEE Trans. Electron Devices **67**(5), 2223–2225 (2020).
6. W. Jiang, Y. Chalich, R. Scott, and M. J. Deen, "Time-Gated and Multi-Junction SPADs in Standard 65 nm CMOS Technology," IEEE Sens. J. **21**(10), 12092–12103 (2021).
7. F. Gramuglia, P. Keshavarzian, E. Kizilkan, C. Bruschini, S. S. Tan, M. Tng, E. Quek, M.-J. Lee, and E. Charbon, "Engineering Breakdown Probability Profile for PDP and DCR Optimization in a SPAD Fabricated in a Standard 55 nm BCD Process," IEEE J. Sel. Top. Quantum Electron. **28**(2: Optical Detectors), 1–10 (2022).
8. C. Veerappan, "Single-Photon Avalanche Diodes for Cancer Diagnosis," Ph.D. dissertation (Delft University of Technology, 2016).

9. I. Vornicu, F. Bandi, R. Carmona-Galan, and A. Rodriguez-Vazquez, "Low-Noise and High-Efficiency Near-IR SPADs in 110 nm CIS Technology," in *European Solid-State Device Research Conference* (2019), pp. 250–253.
10. J. A. Richardson, L. A. Grant, and R. K. Henderson, "Low dark count single-photon avalanche diode structure compatible with standard nanometer scale CMOS technology," IEEE Photonics Technol. Lett. **21**(14), 1020–1022 (2009).
11. M.-J. Lee, P. Sun, and E. Charbon, "A first single-photon avalanche diode fabricated in standard SOI CMOS technology with a full characterization of the device," Opt. Express **23**(10), 13200–13209 (2015).