

ISSW 2022

The International SPAD Sensor Workshop

Focused on the study, modeling, design, fabrication, and characterization of SPAD sensors.

June, 13 - 15

Facilitated by

am^u OSRAM

ISSW 2022 **Workshop Program**

The International SPAD Sensor Workshop · June 13 - 15, 2022

CEST

Monday, June 13

08:15 – 08:30

Welcome and Introduction

David Stoppa, Sony Europe B.V. and Verena Vescoli, ams OSRAM
(Speaker Local Time CEST)

Session 1: SPAD Technologies

Session Chair: Sara Pellegrini, STMicroelectronics
Session Co-Chair: Robert Henderson, University of Edinburgh

08:30 – 09:00

Scalable Backside-Illuminated Charge-Focusing Silicon SPADs with Enhanced Near-Infrared Sensitivity

Edward Van Sieleghem, IMEC (Speaker Local Time CEST)

09:00 – 09:30

A Back Side Illuminated 3D-Stacked SPAD in 45nm Technology

Georg Roehrer, ams OSRAM (Speaker Local Time CEST)

09:30 – 10:00

New SPAD dspc – Third Generation

Daniel Gäbler, X-Fab (Speaker Local Time CEST)

10:00 – 10:30

Back-Illuminated SPADs in Stacked 40nm CIS Technology

Myung-Jae Lee, Korea Institute of Science and Technology (Speaker Local Time CEST +7h)

10:30 – 10:45

Break

10:45 – 11:15

A Challenge for 3µm SPAD Pixel Using Embedded Metal Contact on Deep Trench Pixel Isolation

Jun Ogi, Sony Semiconductors Solutions Corporation (Speaker Local Time CEST +7h)

11:15 – 11:45

Multi-Megapixel 3D-Stacked Charge Focusing SPAD Image Sensors

Kazu Morimoto, Canon (Speaker Local Time CEST +7h)

11:45 – 12:15

Sherbrooke Frontside Illumination SPAD Architecture and Preliminary Performances

Jean-François Pratte, Université de Sherbrooke (Speaker Local Time CEST -6h)

12:15 – 13:05

Lunch and Sponsor Talks

Back-Illuminated SPADs in Stacked 40nm CIS Technology

Eunsung Park^{1,2}, Won-Yong Ha^{1,2}, Dae-Hwan Ahn¹, Hyuk An³, Suhyun Yi³, Kyung-Do Kim³, Jongchae Kim³, Woo-Young Choi², and Myung-Jae Lee¹

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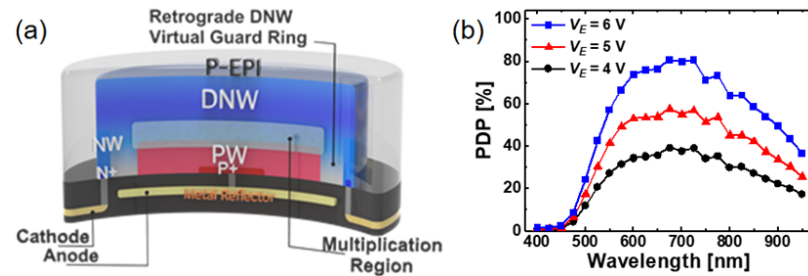


Fig. 1: (a) Cross-section of the back-illuminated SPAD and (b) its PDP performance.

We present a wide spectral-range back-illuminated single-photon avalanche diode (SPAD) in stacked CMOS image sensor (CIS) technology. Fig. 1(a) shows the cross-section of the back-illuminated SPAD fabricated in SK hynix 40 nm CIS technology. The SPAD is based on the P-well(PW)/Deep N-well (DNW) junction, and a virtual guard ring based on the retrograde DNW surrounds the junction to prevent the premature breakdown at the edge of the junction.

The SPAD is implemented in a circular shape with an active area diameter of 5 μm , 2 μm guard ring, and 0.5 μm cathode, resulting in a fill factor of 25%. The guard-ring and cathode sizes were chosen as conservative design parameters, and therefore the fill factor can be improved in future generations with optimized parameters and the use of microlens.

The breakdown voltage of the SPAD is about 23.2 V at room temperature. At the excess bias voltage of 6 V, the SPAD has a dark count rate (DCR) of 70 cps/ μm^2 and exhibits acceptable DCR, below 1000 cps/ μm^2 , even at 90 $^\circ\text{C}$.

Thanks to the wide multiplication region, deep DNW, and metal reflector, the SPAD can achieve a high photon detection probability (PDP) as well as a wide spectral range. As shown in Fig. 1(b) it achieves the PDP of 81% at 675 nm and 39.2% at 940 nm wavelength with the excess bias voltage of 6 V.

The SPAD achieves, to the best of our knowledge, the highest PDP among reported back-illuminated CMOS SPADs so far. We expect that this SPAD can play a key role in various applications such as ToF, LiDAR, AR/VR, robots, drones, biomedical imaging, security, etc.

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Myung-Jae Lee received the Ph.D. degree from Yonsei University, South Korea, in 2013. From 2013 to 2017, he was a Postdoctoral Researcher with TU Delft, The Netherlands, and from 2017 to 2019 he was a Scientist with EPFL, Switzerland. Since 2019, he has been a Principal Investigator with Korea Institute of Science and Technology (KIST), South Korea. He has published 80+ papers in international journals and conferences. He holds 5+ patents and has received 10+ awards.

