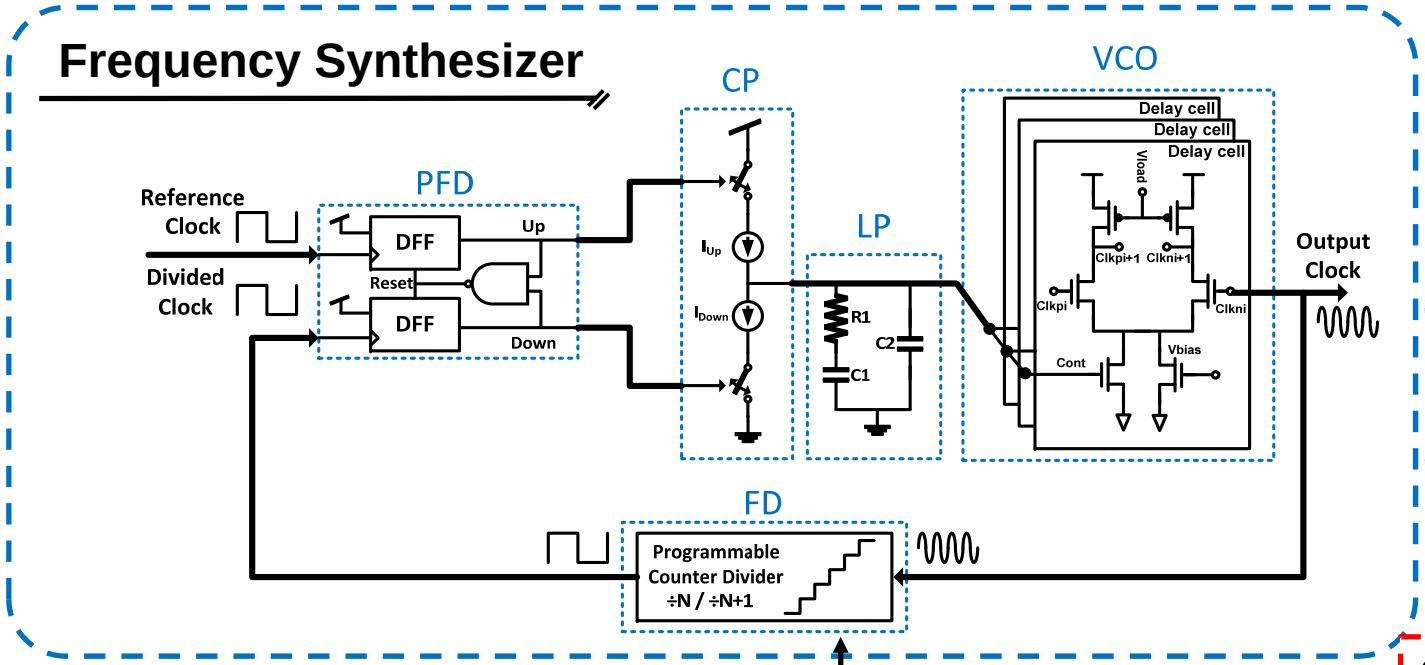
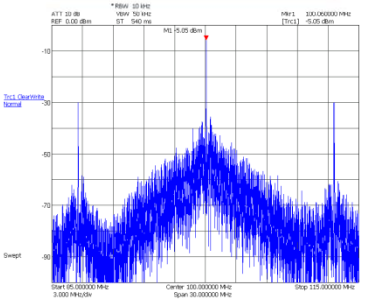
PLL-Based Fractional-N Frequency Synthesizer



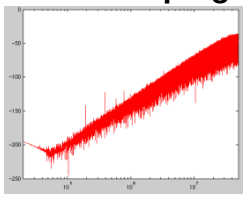
Output clock Power spectrum density



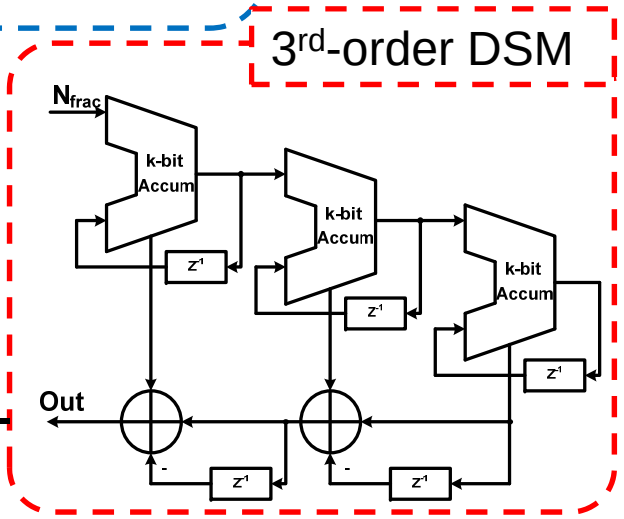
PLL-based fractional-N frequency synthesizer

- ✓ Input : 12.5 MHz
- ✓ Output : 50 ~ 250MHz
- ✓ Resolution : 50 kHz
- ✓ Integer code : 5 bit
- ✓ Fractional code : 7 bit
- ✓ RMS Jitter : 0.0007 UI

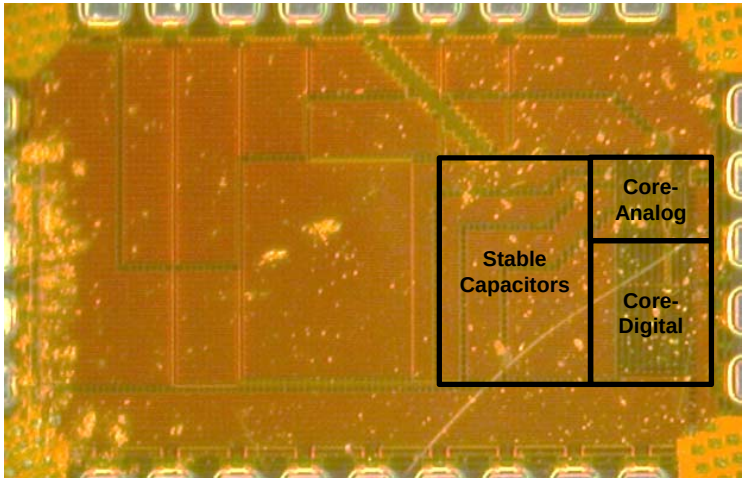
Noise shaping



Dividing ratio control



PLL-Based Fractional-N Frequency Synthesizer



Die photographs

2011 SoC 학술대회 Presentation

- Successfully achieves fractional-N frequency synthesizer for frequency synthesis from 50 MHz to 250 MHz with 50 kHz frequency resolution.
- There is no fractional spur, clean output clock.
- Delta-sigma modulator design technique of this fractional-N frequency synthesizer was presented in 2011 SoC학술대회.

[Study of Spur Reduction Technique for MASH Delta-Sigma Modulator]