# Phase/frequency detectors for high-speed PLL applications

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Two new phase/frequency detectors (PFDs) are proposed that can overcome the speed and jitter limitations of conventional PFD schemes. One of the proposed circuits has a reset time of 0.32ns and the other a reset time of 0.03ns during the phase-locked loop capture process, according to HSPICE simulation with 0.8μm CMOS process parameters.

*Introduction:* There is increasing demand for low-jitter, high-speed phase-locked loops (PLLs) for applications such as data transfer systems and mobile communication systems. In a PLL, a phase/frequency detector (PFD) monitors phase and frequency differences between the input signal ($R$) and voltage-controlled oscillator (VCO) output ($V$), and generates an up signal (Up) if $R$ leads $V$ and a down signal (Dn) if $R$ lags $V$ [1]. With conventional PFDs such as reported in [2, 3], the Up and Dn pulses cannot be shorter than a certain minimum width, even if $R$ and $V$ have no phase difference, in order to avoid the dead-zone problem.

When both Up and Dn signals exist simultaneously, the two current paths of the charge pump are shorted. This perturbs the VCO control voltage and results in PLL jitters [4]. We propose new PED schemes that minimise this problem.

*Proposed schemes:* Conventional PFDs as described in [2, 3] are made up of two dual edge-triggered, resettable D-type flip-flops (DFFs) with their outputs connected to the AND gate. The output of the AND gate becomes logic one when the output signals of both DFFs are logic one, and this in turn resets both DFFs. Consequently, both Up and Dn signals remain logic one until the reset signal goes through the AND gate and the reset path of the DFFs. The reset time can be easily detertmined to be several gate delays. For example, the PFDs shown in Fig. 14 of [2] and Fig. 6 of [3] have six gate delays for their reset time.

A significant reduction in reset time can be made with the proposed scheme (PFD1) shown in Fig. 1. PFD1 consists of two resettable ratioed latches [5], OR and AND gates. This circuit is designed to be operated in the negative-edge triggered mode. The ratioed latch operates in the following manner. When the input to N1 is logic one, N2 and P2 remain in the cut-off state because the $W/L$ ratios of N1 and P1 are designed such that the node voltage

at node 1 always remains below the threshold voltage of N2, keeping the Up signal the same. When the input to N1 is logic zero and the input to P1 is logic one, the voltage at node 1 remains at the ground level, and the Up signal can be pulled up to logic one only by P2. If the input to P1 changes from logic one to logic zero, the voltage at node 1 is set to logic one. At the same time, the Up signal is pulled down to logic zero by N2 because of the *W/L* ratios of P2 and N2. The OR gate removes overwriting in outputs and the AND gate changes the Up and Dn signals from logic one to logic zero. The reset path of PFD1 is three-gate delays, as shown in bold lines in Fig. 1.

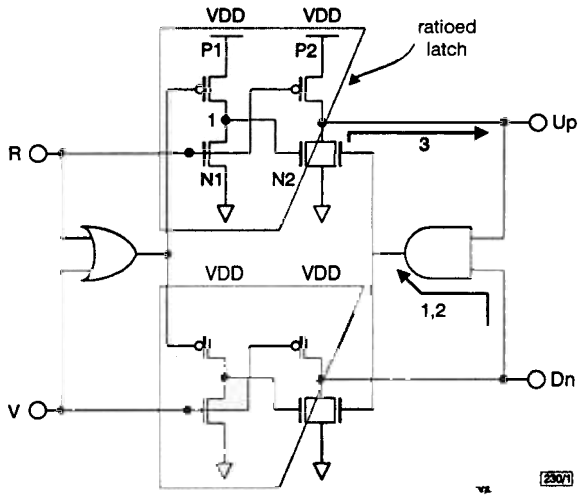


**Fig. 1** *Schematic diagram of PFD1*

The PFD reset time can be reduced further by using two reset paths as in the circuit (PFD2) shown in Fig. 2. PFD2 consists of two resettable ratioed latches, two inverters, and one NOR gate, and operates in the negative-edge triggered mode (as does PFD1). When the Dn signal changes from logic zero to logic one, the input to P6 is pulled down to logic zero by the reset path through inverter. Thus, Up signal remains at logic zero even when *V* changes from logic one to logic zero. Through this reset path, the output voltage is set below the turn-on voltage of the charge-pump switch. The other reset path uses a NOR gate and by this, the Up signal changes from logic one to logic zero when both the *R* and *V* signals become logic one. Consequently, the reset time is reduced significantly even though the reset path is three gate delays.

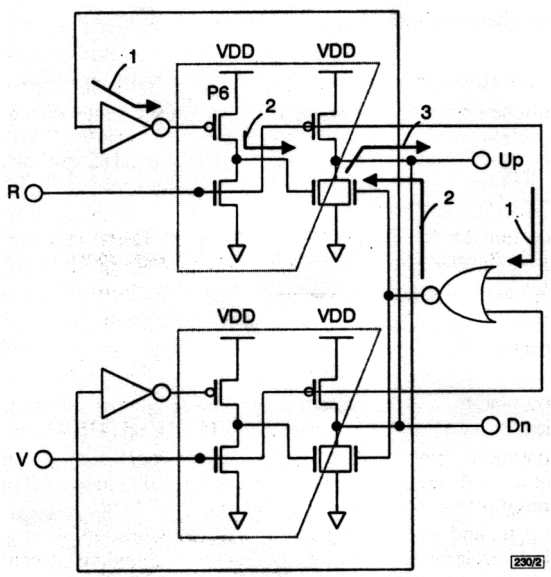


**Fig. 2** *Schematic diagram of PFD2*

*Simulation results:* To evaluate the performance of the proposed PFDs, HSPICE simulation was performed using 0.8μm standard CMOS process parameters. For simulation, the *R* and *V* signals were assumed to have 4ns duration, and *R* leads *V* by 0.3ns. For simplicity, simulation was carried out with the PFD block alone, and it was assumed that the required Up and Dn signal levels for turn-on voltage of the charge-pump switch are 2.0V, and the supply voltage 5V. Fig. 3*a* shows the simulation results for PFD1. The reset time is 0.32ns and the propagation delay is 0.11ns. The simulation results for PFD2 are shown in Fig. 3*b*. The reset time is only 0.03ns and the propagation delay is 0.095ns. It should be noted that the reduced reset time is only valid for the PLL capture process. For the PLL lock-in process, PFD2 has a similar performance as PFD1. Although simulation results for both PFD1 and PFD2 show tails in the Up and Dn signals, this may not cause problems when they are kept below the turn-on voltage of the charge pump switches.

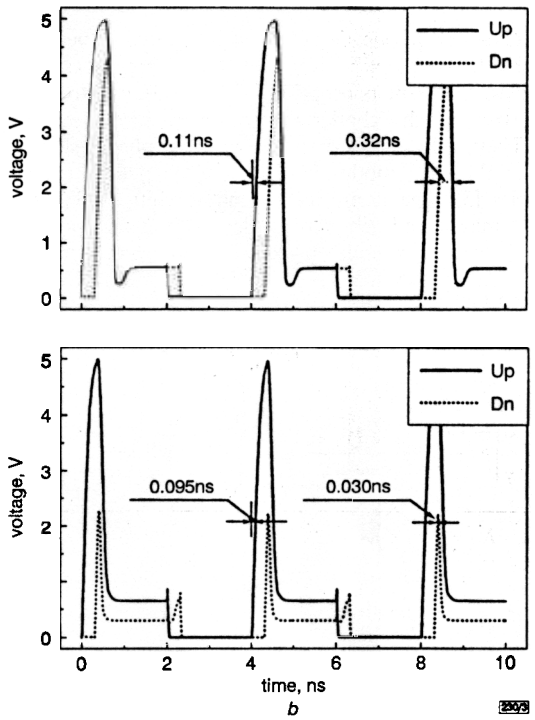


**Fig. 3** *Simulation results for Up and Dn characteristics of proposed PFDs*

*a* PFDI
*b* PFD2

*Conclusion:* Two phase/frequency detectors, PFD1 and PFD2, are proposed that can significantly improve the speed and jitter performance of conventional PFDs. According to HSPICE simulation, PFD1 has a reset time 0.32ns and PFD2 of 0.03ns. It is expected that these circuits will find useful applications in the realisation of high-speed and low-jitter PLLs.

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