PERGAMON

Solid-State Electronics 45 (2001) 1673–1678

SOLID-STATE ELECTRONICS

Design and analysis of a new self-aligned asymmetric structure for deep sub-micrometer MOSFET

Chang-Soon Choi [a], Kyung-Whan Kim [b], Woo-Young Choi [a,*]

[a] *Department of Electrical and Electronic Engineering, 120-749 Yonsei University, Shinchon-dong 134, Seodaemun-gu, Seoul, Republic of Korea*

[b] *Memory R and D Division, Hyundai Electronics Industries, San 156-1, Ami-ri, Bubal-eub, Ichon-si, Kyungi-do, Republic of Korea*

Received 12 September 2000

Abstract

A new self-aligned asymmetric structure (SAAS) is proposed for deep sub-micrometer MOSFET and its device characteristics are analyzed. The proposed structure enables the source, drain and channel to be designed independently without additional lithography steps. SAAS with lateral asymmetric channel and highly doped source extension improves driving capability and short channel behavior without sacrificing hot carrier reliability. Based on the results of hydrodynamic device simulation over a wide range of process conditions, it is shown that highly doped asymmetric halo provides enhanced velocity overshoot and suppressed drain-induced barrier lowering. By employing asymmetric highly doped source extension, the degradation of driving capability is suppressed that can be caused by the increased parasitic resistance in highly doped asymmetric halo. © 2001 Published by Elsevier Science Ltd.

Keywords: Velocity overshoot; Halo doping; Asymmetric structure; Self-aligned; Device simulation

1. Introduction

The demands for higher integration levels and higher device performance have led to the scaling of MOSFETs down to the 0.1 μm regime. As the device feature size shrinks to 0.1 μm dimension, the velocity overshoot has received significant attention because it is directly related to the improvement of driving capability and transconductance [1,2]. However, the adverse effect caused by substantially increased parasitic resistance in lightly doped drain (LDD) region severely degrades the device performance. To overcome such limitation, highly doped LDD extension is required, but this gives negative influence on the short channel effects and the device reliability.

One attractive way to improve device performance without sacrificing reliability is the use of asymmetric MOSFET structures, which has been discussed extensively in recent years [3–9]. These structures have inherent advantage that source and drain regions can be designed independently, even though they need additional masks and complex layout steps. It makes the device design more suitable for improving the driving capability while maintaining the hot carrier reliability.

Several types of asymmetric structures have been proposed and experimentally demonstrated. Asymmetric LDD structures with the heavily doped deep junction at source side while lightly doped extension at drain side have been proposed to reduce the parasitic resistance at source side [3,4]. However, it is difficult to employ such structures to sub-0.1 μm MOSFET because the short channel effects are worsened due to the absence of the LDD extension at the source side. Lateral asymmetric channel structures have been proposed and introduced to SOI devices in order to take full advantage of the velocity overshoot and suppress the short channel effects [5–9]. It has non-uniform channel doping profile with a localized pileup region next to source extension as a result of asymmetric halo. As the channel length is scaled down below 0.1 μm, the asymmetric halo doping

* Corresponding author. Fax: +82-2-312-4584.
E-mail address: wchoi@yonsei.ac.kr (W.-Y. Choi).

0038-1101/01/$ - see front matter
PII: S0038-1101(01)00132-0

concentration must be increased in order to fully suppress the drain-induced barrier lowering (DIBL) and to provide the acceptable threshold voltage. However, it causes serious degradation of device performance due to the increased parasitic source resistance caused by charge compensation [10]. In addition, the fabrication processes of previously reported asymmetric structures have poor feasibility in sub-0.1 μm regime because they require additional masks and precise alignments.

In this study, we present a novel self-aligned asymmetric structure (SAAS) without the problems mentioned above, and verify that the new lateral doping scheme provides many advantages for improving device performance while maintaining good short channel behaviors and reliability. All the analyses used in this paper are based on the two-dimensional process and device simulations [11,12]. Section 2 describes the proposed fabrication steps and the design concepts for SAAS. In Section 3, the device characteristics are discussed by comparing SAAS with the previously reported asymmetric structures, and the reasons for the improvement of device performance in SAAS are explained.

2. Proposed process and design concepts

The key fabrication steps for n-channel SAAS MOSFET are schematically shown in Fig. 1. After 38 Å thick gate oxide is grown on (1 0 0) p-type wafer, poly-Si is deposited for gate material. Poly-Si is doped with $POCl_3$ and the pad oxide is deposited on the poly-Si. Next, the pad oxide on the gate–source area is etched away using lithography and dry etching process. Nitride film is deposited and etched to form a sidewall as shown in Fig. 1(C). In the sidewall formation, the thickness of nitride film determines the poly-gate length. This sidewall masking technique has been employed in 0.1 μm MOSFET technology and reported to have better uniformity of line width compared with e-beam lithography [13]. After the exposed poly-Si is anisotropically etched, the highly doped source extension is formed by As^+ (1×10^{15} cm^{-2}, 10 keV) implantation. The asymmetric halo implantation with BF_2^+ (2×10^{13} cm^{-2}, 65 keV, 25°) is performed to make lateral asymmetric channel profile. In order to prevent damages during the subsequent steps, nitride is deposited for capping the source region and etched by dry etching or CMP until the pad oxide reveals as shown in Fig. 1(E). After the pad oxide is etched, the exposed poly-Si is etched by dry etching. The LDD extension is formed using As^+ (5×10^{13} cm^{-2}, 10 keV) implantation. The remaining nitride is removed by H_3PO_4. After the 1000 Å sidewall formation, the deep source/drain junctions are formed with As^+ (6×10^{15} cm^{-2}, 40 keV) implantation, followed by rapid thermal annealing (1050°C, 10 s). The following process steps are identical to those of the conventional MOSFETs.

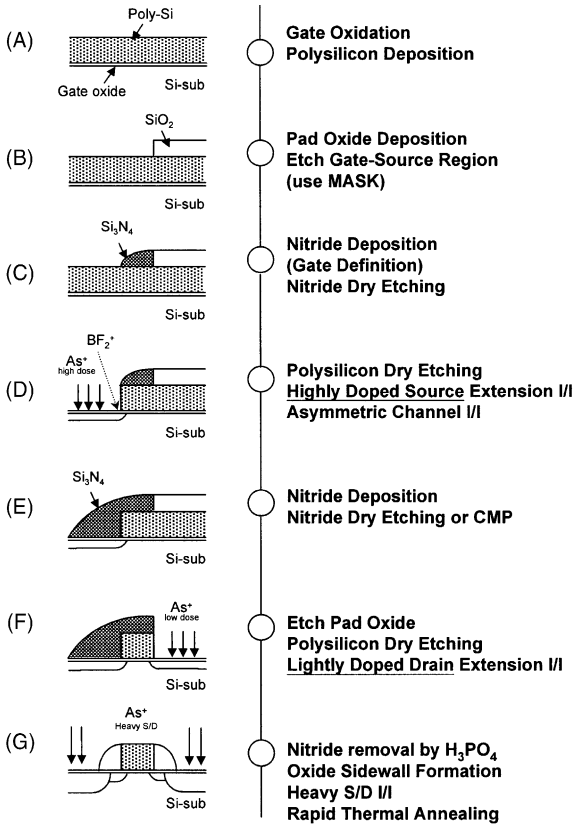

Fig. 1. Proposed fabrication steps for SAAS n-channel MOSFETs.

As discussed above, we use only one lithography step for gate–source definition (Fig. 1(B)). Therefore, the proposed fabrication process for SAAS is expected to solve the self-alignment problem without additional masks, and independent optimization of the channel and the source/drain regions is possible for high performance and reliability.

To optimize the SAAS design idea for high performance and reliability, extensive simulations are performed using the process and device simulators, TSUPREM-4 and MEDICI [11,12]. The schematic cross-section of n-type SAAS MOSFET is given in Fig. 2(a). The structure is similar to the conventional MOSFET except for asymmetric LDD and asymmetric channel. Fig. 2(b) shows the simulated two-dimensional doping profile of SAAS. Fig. 2 indicates that SAAS has the asymmetric channel profile along the $Si–SiO_2$ interface. It also has the highly doped source extension in opposition to the LDD extension. From these figures, SAAS differs from the conventional MOSFET structures in that it has localized highly doped channel next

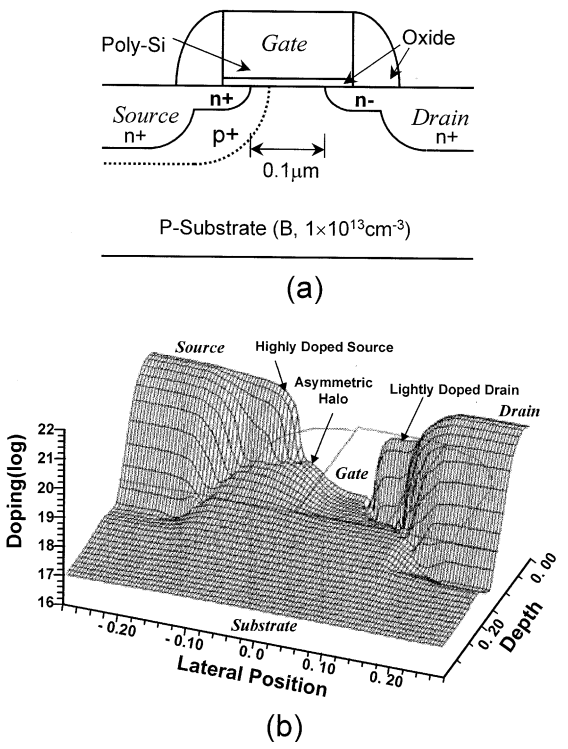

Fig. 2. (a) Schematic cross-section of SAAS nMOSFET. (b) Surface plots of the impurity concentration of SAAS that is used for the simulation analysis.

to the highly doped source and gradually lowered channel at the LDD.

The structural concepts of SAAS are expected to show several advantages on device characteristics in deep sub-micrometer MOSFET. Highly doped source may alleviate increased parasitic resistance caused by the highly doped halo which is employed to further enhance the velocity overshoot and to suppress the short channel effects. In the drain side, LDD extension and gradually lowered channel are expected to effectively suppress the hot carrier induced reliability problems. In addition, high built-in electric field created by the doping concentration gradient of the asymmetric channel improves the non-equilibrium carrier transport, the velocity overshoot, at the source side [5]. This should benefit the driving capability and the circuit operation speed. Consequently, it is possible to achieve high performance without sacrificing the hot carrier reliability in SAAS.

3. Device characteristics and discussion

To explain the attributes of this new doping scheme, we analyzed and compared the device characteristics of four nMOSFET structures with numerical simulations. The main features of SAAS and previously reported structures are compared in Table 1. A-Chan and A-Drain represent the asymmetric nMOSFETs with asymmetric channel and asymmetric drain, respectively. It should be noted that the two different halo doses (5×10^{12} cm^{-2}, 2×10^{13} cm^{-2}) are selected for investigating the influence of halo doping concentration on the device characteristics in asymmetric drain (SAAS) and symmetric drain (A-Chan) structures. Conv represents the conventional LDD nMOSFET with uniform channel. For fair comparison, all structures have the effective channel length of 0.1 μm, the punchthrough stopper of B^+ (3×10^{12} cm^{-2}, 40 keV), the substrate doping of 1×10^{13} cm^{-3} and the threshold voltage of about 0.33 V. The uniformly doped channels in the case of Conv and A-Drain structures are formed by the threshold adjustment implantation (BF_2^+, 5×10^{12} cm^{-2}, 90 keV) before the gate oxidation. The process conditions mentioned above are kept the same for all the samples while the asymmetric channel and the source/drain related process conditions are changed as shown in Table 1.

Fig. 3 shows the short channel characteristics (V_T roll-off, DIBL) of these structures. As shown in Fig. 3(a), the asymmetric channel structures (SAAS, A-Chan) do not experience the V_T roll-off effect even in the 0.1 μm dimension because the high boron concentration at the source side results in the reverse short channel effect [5]. On the other hand, the uniform channel structures (A-Drain, Conv) have serious V_T roll-off

Table 1
Main features of four structures used for simulation analysis[a]

Label	Source	Channel	Drain
SAAS (2×10^{13})	1×10^{15} cm^{-2}	Asymmetric 2×10^{13} cm^{-2}	5×10^{13} cm^{-2}
SAAS (5×10^{12})	1×10^{15} cm^{-2}	Asymmetric 5×10^{12} cm^{-2}	5×10^{13} cm^{-2}
A-Chan (2×10^{13})	5×10^{13} cm^{-2}	Asymmetric 2×10^{13} cm^{-2}	5×10^{13} cm^{-2}
A-Chan (5×10^{12})	5×10^{13} cm^{-2}	Asymmetric 5×10^{12} cm^{-2}	5×10^{13} cm^{-2}
A-Drain	1×10^{15} cm^{-2}	Uniform 5×10^{12} cm^{-2}	5×10^{13} cm^{-2}
Conv	5×10^{13} cm^{-2}	Uniform 5×10^{12} cm^{-2}	5×10^{13} cm^{-2}

[a] Uniform channel is formed by BF_2^+ (5×10^{12} cm^{-2}, 90 keV) implantation. Asymmetric channel is formed by BF_2^+ (5×10^{12} cm^{-2} or 2×10^{13} cm^{-2}, 65 keV, 25°) implantation only at the source side.

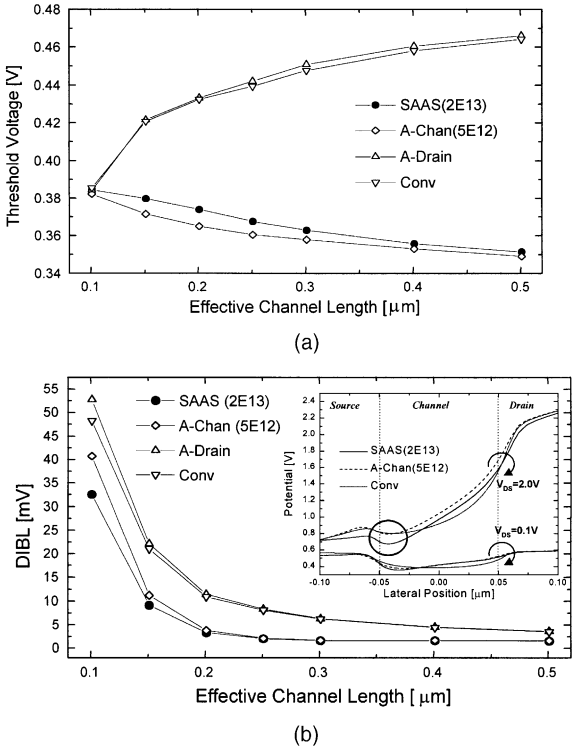

Fig. 3. (a) Threshold voltages (b) DIBL [V_{GS} ($V_{DS} = 0.1$ V)–V_{GS}($V_{DS} = 2.0$) at $I_D = 10^{-7}$ A/μm] as a function of effective channel length in SAAS and other structures. The inset shows the simulated potential distribution along the channel.

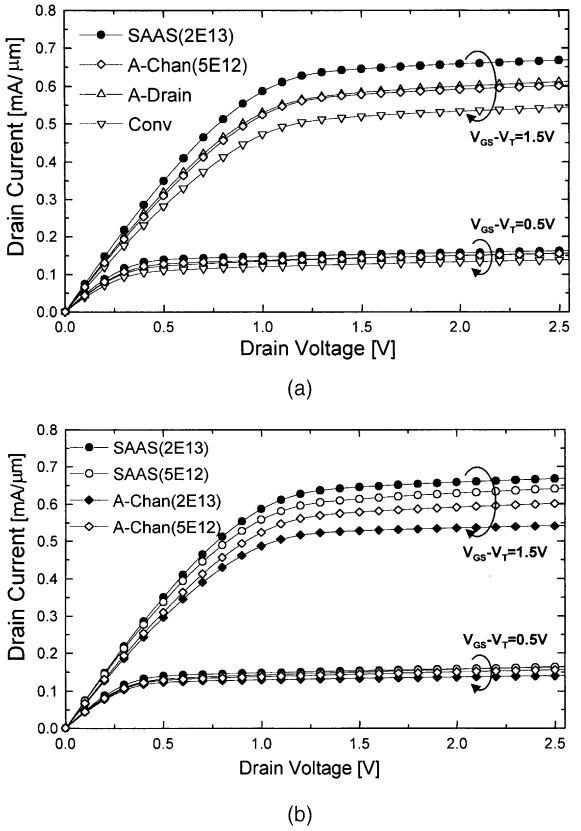

Fig. 4. (a) Simulated I_D–V_D characteristics of SAAS and other structures. (b) The I_D–V_D characteristics of SAAS and asymmetric channel structure (A-Chan) under the different asymmetric halo doping conditions.

effects. Fig. 3(b) shows the DIBL characteristics of these structures. The uniform channel structures have worse DIBL characteristics than those of the asymmetric channel structures. In these structures, A-Drain with the highly doped source shows the worst DIBL characteristics. In the asymmetric channel structures, DIBL is well controlled due to the large potential barrier generated by the highly doped channel next to the source extension, which limits the spread of the depletion region from drain to source. It is confirmed by the inset of Fig. 3(b) in which the surface potentials are plotted along the channel. The figure also indicates that DIBL will be further improved if higher doped halo is adopted in the case of SAAS. From these results, highly doped asymmetric halo is needed to effectively suppress the short channel effects.

Fig. 4(a) shows the simulated I_D–V_D characteristics for SAAS and compared structures. We can clearly observe higher current driving capability of SAAS than those of any other compared structures. Fig. 4(b) shows the influence of asymmetric halo dose on the driving capability in SAAS and A-Chan. It is shown that A-Chan with higher dose halo implantation results in the degradation of driving capability. On the contrary, the driving capability of SAAS is enhanced by higher dose halo implantation.

To explain the reason for the enhancement of driving capability in these structures, we simulated the electron velocity and the electric field along the channel using hydrodynamic simulator with energy balance equation, which has been reported to reasonably predict the enhancement of driving current caused by the velocity overshoot [2].

Fig. 5(a) shows the average electron velocity of SAAS and compared structures along the interface. For the asymmetric channel structures, the electron velocity rises rapidly at the source side and it causes the velocity overshoot phenomenon. Therefore, the origin of the improved driving capability in asymmetric structures (SAAS, A-Chan) is attributed to the high carrier velocity at the channel next to source. Furthermore, SAAS with higher doped halo further enhance the electron velocity at the source side. This result indicates that the halo dose is closely related to the electron velocity.

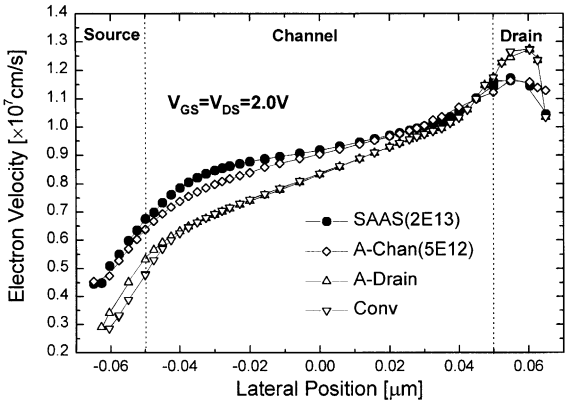

Fig. 5. (a) Simulated average electron velocity distributions of SAAS and other structures and (b) simulated average electron velocity distributions of SAAS and A-Chan structure under the different asymmetric halo doping conditions ($V_{GS} = V_{DS} = 2.0$ V).

Fig. 5(b) shows the influences of halo dose on the electron velocity along the channel. From this figure, we know that the electron velocity at channel depends on the channel profiles, not the source/drain. As the halo dose increases, the electron velocity at the source also increases. As shown in Fig. 4(b), the highly doped halo results in the improvement of driving capability in SAAS, which can be explained by the enhancement of electron velocity. On the contrary, A-Chan shows the decreased driving current level as the halo dose increases. This is because the halo interacts with LDD and causes the source resistance to be increased, which is a key factor for the saturation current levels [10]. It makes the A-Chan undesirable for scaling down to 0.1 μm regime while maintaining adequate short channel behaviors. In other words, increasing the asymmetric halo doping in order to suppress the short channel effects and to enhance the velocity overshoot results in the degradation of driving performance in conventional (symmetric) drain structures. However, SAAS is less sensitive to such effects because of having the highly doped asymmetric source extension with low parasitic resistance.

Fig. 6(a) and (b) show the simulated lateral electric field profiles and net doping concentration along the interface for the four structures, respectively. It can be seen that the electric fields of asymmetric channel structures are much higher those of uniform channel structures at the channel next to the source, while the electric fields of uniform channel structures exceed those of the asymmetric channel structures at the drain end of channel. In the asymmetric structures, the high electron velocity as seen in Fig. 5(a) is due to the large electric field and its gradients produced by the localized highly doped channel next to the source extension as shown in Fig. 6(b). The inset of Fig. 6(b) is the magnification of the net doping concentration at the source side. The figure shows that the net doping of A-Chan is much lower than those of other structures. This means that the

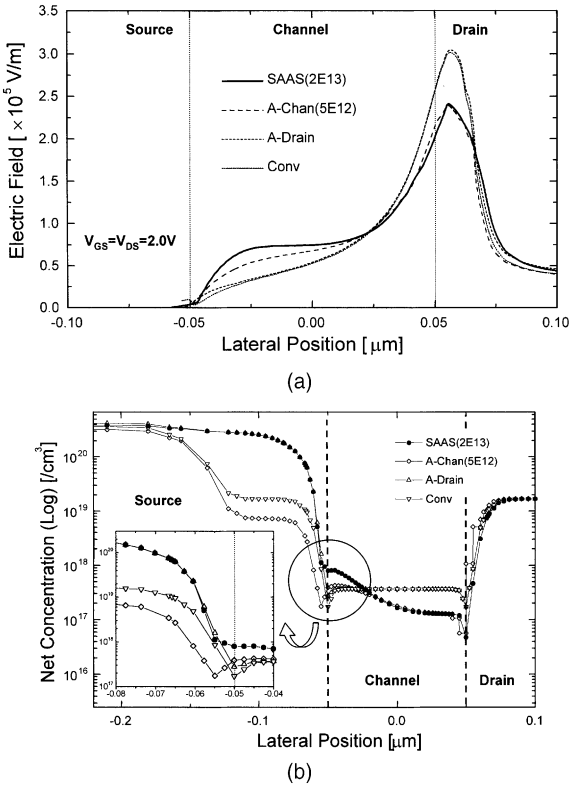

Fig. 6. (a) Simulated lateral electric field distributions across the channel. (b) Net doping profiles of SAAS and compared structures at 1.5 nm away from Si–SiO_2 interface. The inset shows the net doping profiles at the source area.

parasitic resistance at the source side is increased due to the charge compensation. As a result, the symmetric drain structure (A-Chan) is not advantageous in the respect of driving capability if highly doped halo is employed, which was already discussed and shown in Fig. 4(b). On the contrary, SAAS has the highest net doping level at the source side in the compared structures. The reason is that highly doped source as well as highly doped channel promises high net doping concentration. Consequently, SAAS with high net doping at the source extension is effective in alleviating the increasing parasitic resistance caused by the highly doped halo.

In addition, Fig. 6(a) indicates that the magnitudes of the drain electric field among asymmetric channel (SAAS, A-Chan) structures are approximately 22% less than those of uniform channel (A-Drain, Conv) structures. It is because the gradually lowered channel at the lightly doped drain as shown in Fig. 6(b) results in the decreased lateral electric field. Since the hot carrier degradation is exponentially dependent on the electric field at drain, SAAS with the lower electric field at the drain junction is expected to effectively suppress the hot carrier induced degradation.

4. Conclusion

A novel SAAS which can solve the problems of asymmetric MOSFET design and process complexities has been proposed for 0.1 μm MOSFET technology. The main objective is to achieve high device performance without sacrificing reliability using asymmetric doping scheme. Asymmetric channel with highly doped source extension can be realized without additional masking steps in SAAS. Two-dimensional simulations verify that SAAS is very effective in providing improved short channel behaviors, current driving capability and reliability in 0.1 μm dimension.

References

[1] Assaderaghi F, Ko PD, C Hu. Observation of velocity overshoot in silicon inversion layers. IEEE Electron Dev Lett 1993;14(10):484–6.
[2] Song J-H, Park Y-J, Min H-S. Drain current enhancement due to velocity overshoot effects and its analytic modeling. IEEE Trans Electron Dev 1996;43(11):1870–5.
[3] Horiuchi T, Homma T, Murao Y, Okumura K. An asymmetric sidewall process for high performance LDD MOSFETs. IEEE Trans Electron Dev 1994;41(2):186–90.
[4] Chen J, Tao J, Fang P, C Hu. 0.35 μm asymmetric and symmetric LDD device comparison using a reliability/speed/power methodology. IEEE Electron Dev Lett 1998;19(7):216–8.
[5] Odanaka S, Hiroki A. Potential design and transport property of 0.1 μm MOSFET with asymmetric channel profile. IEEE Trans Electron Dev 1997;44(4):595–600.
[6] Shin H, Lee S. An 0.1 μm asymmetric halo by large-angle-tilt implant (AHLATI) MOSFET for high performance and reliability. IEEE Trans Electron Dev 1999;46(4):820–2.
[7] Shen C-C, Murguia J, Goldsman N, Peckerar M, Melngailis J, Antoniadis D. Use of focused-ion-beam and modeling to optimize submicron MOSFET characteristics. IEEE Trans Electron Dev 1998;45(2):453–9.
[8] Cheng B, Rao V, Woo J. Exploration of velocity overshoot in an high-performance deep sub-0.1 μm SOI MOSFET with asymmetric channel profile. IEEE Electron Dev Lett 1999;20(10):538–40.
[9] Pavanello M-A, Martino J-A, Dessard V, Flandre D. Analog performance and application of graded-channel fully depleted SOI MOSFETs. Solid-State Electron 2000;44:1219–22.
[10] Hwang H, Lee D-H, Hwang J-M. Degradation of MOSFETs drive current due to halo ion implantation. IEDM Tech Digest 1994;567–70.
[11] Technology Modeling Associate TSUPREM-4, version 6.5, 1998.
[12] Technology Modeling Associate MEDICI, version 4.1, 1998.
[13] Sung S-K, Choi Y-J, Lee J-D, Park B-G. Realization of ultra-fine lines using sidewall structures and their application to nMOSFETs. J Korean Phys Soc 1999;35:S693–6.