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LETTER

A New Charge Pump PLL with Reduced Jitter

SUMMARY A new charge pump is proposed which provides improved jitter characteristics for a phase-locked loop (PLL). The PLL with the proposed charge pump is implemented with 0.6 μm CMOS technology. The measured RMS output jitter is as much as 28% smaller than that of a PLL with a previously reported charge pump structure.

key words: charge pump, phase-locked loop (PLL), jitter characteristics

1 Introduction

A charge pump is widely used in the phase-locked loop (PLL) for many applications [1], [2]. Figure 1 shows the block diagram of the charge-pump PLL. Ideally, two outputs of Phase/Frequency Detector (PFD) should have the same logic values and the charge pump output should be fixed when the PLL is locked. However, this does not happen in real circuits as the charge pump circuit usually has asymmetric features that cause the fluctuation in the Voltage Controlled Oscillator (VCO) control voltage and PLL output phase noise. In order to minimize this problem, a new charge pump structure has been proposed [3]. The PLL circuit that has the proposed charge pump is realized and its jitter characteristics are compared with those of a previously reported charge pump PLL [4].

2. Design of Phase-Locked Loop

Figure 2 shows the conventional charge pump structure (Type I) [4]. When either UP or DN signal is logic '1' and the other is logic '0,' FST or SLW node is charged and the other node is discharged, respectively. This provides the VCO control voltage required for PLL operation. When the PLL is locked, both UP and DN signals are logic '0' as there is no phase/frequency difference between PLL input and output. In this case, current paths represented by dotted lines in Fig. 2 are established, and FST, SLW node voltages should remain fixed. However, if FST, SLW node voltages differ from the initial bias voltages, they drift because the current driving capabilities of PMOS and NMOS transistors lying in the same current path are not the same. The amount of FST, SLW node voltage drift increases as the difference between the node and bias voltages increases. Consequently, PLL jitter characteristics get worse as its operation frequency moves away from the center frequency.

A new charge pump structure (Type II) that minimizes the above problem is shown in Fig. 3. This charge pump uses a self-biased method and functions as a differential charge pump. It has current mirrors which establish current path ② from path ① when both UP and DN signals are logic '1.' When UP and DN signals are both logic '0,' PMOS and NMOS transistors are all turned off. The FST and SLW node voltages should remain fixed, as there is no leakage path. As a result, the PLL output jitter is reduced. When UP and DN signals are both logic '1,' which happens during the PFD reset time, a FST, SLW node voltages in both charge pump structures can drift. However, this is not a major

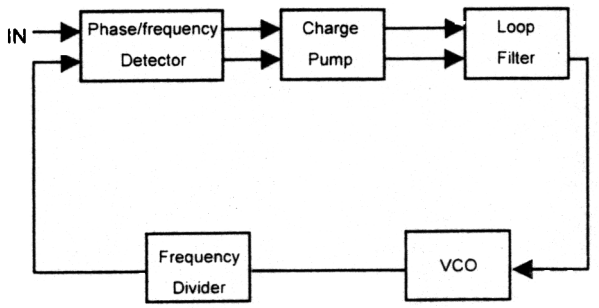

Fig. 1 Block diagram for phase-locked loop.

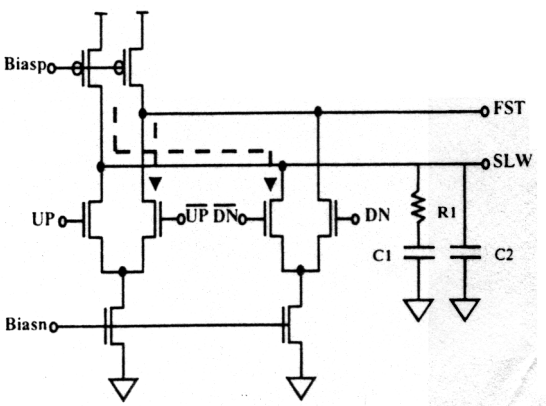

Fig. 2 Schematic diagram for conventional charge pump (Type I).

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†The authors are with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, 120-749, Korea.

††The author is with Samsung Electronics, Korea.

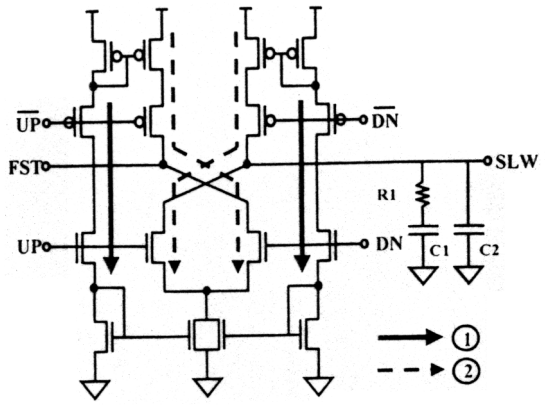


Fig. 3 Schematic diagram for newly proposed charge pump (Type II).

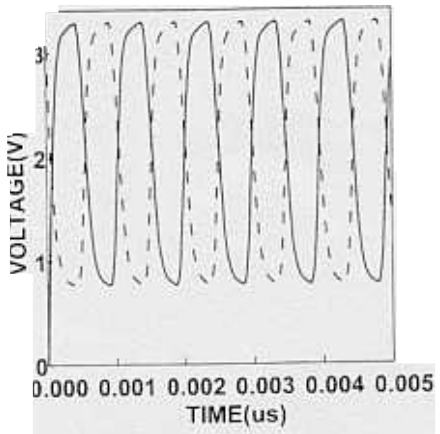


Fig. 4 Differential outputs of VCO.

problem because the duration of the PFD reset time is relatively small.

To compare the performance between the conventional charge pump (Type I) and the newly proposed charge pump (Type II), two PLL circuits are designed each of which includes Type I or Type II charge pump. Each PLL has a conventional PFD [5], a four-stage frequency divider (1/16) made up of four dynamic D-type flip-flops [6], and a second-order on-chip loop filter. The loop filter parameters ($R_1 = 5000\,\Omega$, $C_1 = 200\,\text{pF}$ and $C_2 = 20\,\text{pF}$) are chosen so that the damping factor of the closed-loop transfer function is 0.707. This corresponds to the loop bandwidth of 3.3 MHz. For the VCO, a six-stage differential ring oscillator is used. Each ring oscillator stage is composed of a differential NMOS pair with variable resistance loads made of PMOS devices operating in the triode region. Figure 4 shows the SPICE simulation results for VCO output at the oscillation frequency of 1.03 GHz. Figure 5 shows the simulated transient responses of VCO control voltages for two PLL circuits having different charge pumps (Type I, Type II). For the simulation, the input frequency is 35.7 MHz and the locked VCO frequency is 571 MHz. It is shown that the PLL with Type II charge

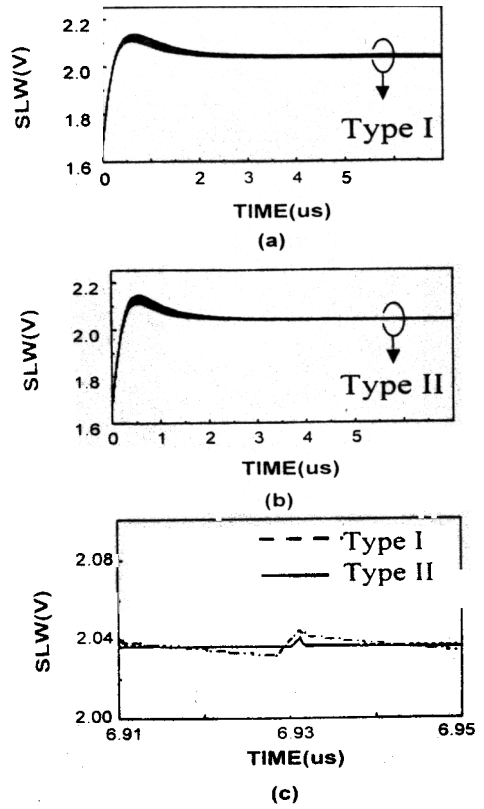


Fig. 5 The transient variations of the control voltage. (a) Type I, (b) Type II, (c) The magnified waveforms.

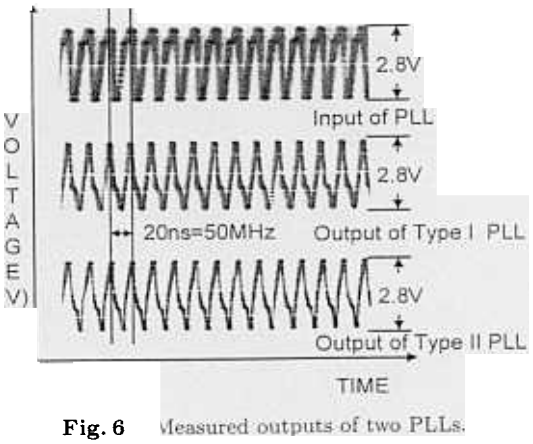


Fig. 6 Measured outputs of two PLLs.

pump has smaller voltage variation once it is locked.

3. Experimental Results

Figure 6 shows measured output of two PLLs locked with 50 MHz input signals. For both PLLs, the measured locking range of VCO frequency is from 532 to 800 MHz. The total power consumption including I/O buffers is about 130 mW for both PLLs. Table 1 summarizes the PLL characteristics. As shown in Table 1, Type II PLL with the new charge pump structure shows improved jitter characteristics in the entire frequency

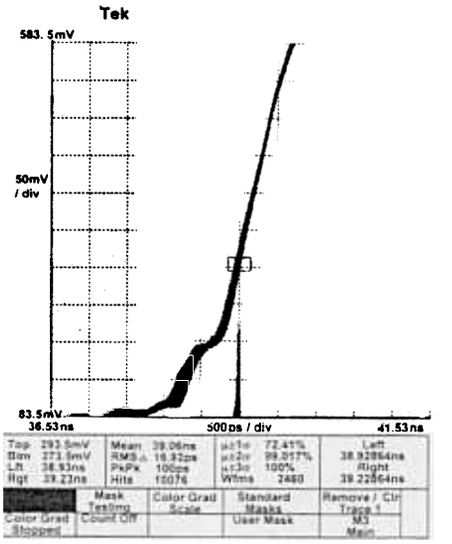
Table 1 PLL characteristics.

		Type I	Type II
Technology		0.6-um CMOS	
Supply Voltage		3.3V	
Power Consumption		130 mW	
Locking Range		532 - 800 (MHz)	
jitter(rms)	532MHz	19.03ps	14.59ps
	657MHz	11.44ps	10.71ps
	800MHz	16.92ps	12.10ps

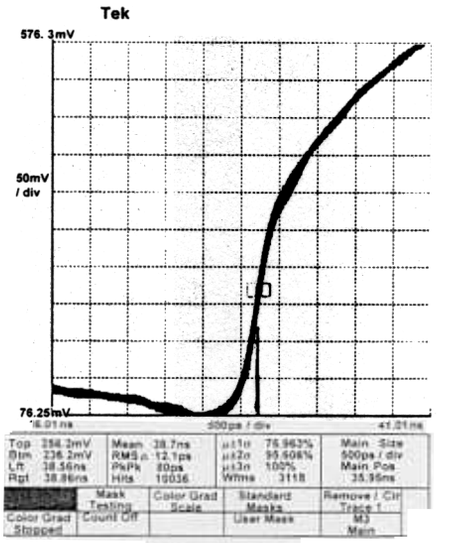
range and the improvement is much pronounced at frequencies away from the PLL center frequency as expected. The jitter measurement is carried out using Tek 11801C digital sampling oscilloscope by applying 3.3 V_{p-p} periodic pulse signals supplied by HP 81101A pulse generator. Figure 7 shows the measured jitter characteristics of Type I (a) and Type II (b) PLL at 800 MHz. It should be noted that the measured PLL output jitter has a considerable contribution from the signal source used. The measured RMS jitter for the signal source alone is 13.8 ps at 41 MHz.

4 Conclusion

A new low-jitter charge pump PLL is realized. In the experimental results, the new charge pump PLL has reduced jitter characteristics than the conventional structure. This is because the leakage current paths for the charge pump output are blocked when the PLL was locked. Consequently, the charge pump output voltages remain stable. The measured PLL RMS jitter is as much as 28% less than that of the PLL with a previously reported charge pump structure. The new charge pump PLL can be useful for implementing high-speed and low-jitter clock data recovery (CDR) circuits.



(a) Type I PLL



(b) Type II PLL

Fig. 7 PLL output jitter characteristics (f_{DIV} = 50 MHz, f_{VCO} = 800 MHz).

Acknowledgments

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