PAPER

A 1.25-Gb/s Digitally-Controlled Dual-Loop Clock and Data Recovery Circuit with Enhanced Phase Resolution

Chang-Kyung SEONG[†a)], **Seung-Woo LEE**[††], ***Nonmembers***, ***and*** **Woo-Young CHOI**[†], ***Member***

SUMMARY A new 1.25-Gb/s digitally-controlled dual-loop clock and data recovery circuit is realized. To overcome jitter problems caused by the phase resolution limit, the CDR has two phase generation stages: coarse generation by a phase interpolator and fine generation by a variable delay buffer. The performance of the proposed CDR was verified by behavioral and transistor-level simulations. A prototype CDR chip fabricated with 0.18 μm CMOS process shows error-free operation for ±400 ppm frequency offset. The chip occupies $165 \times 255\ \mu m^2$ and consumes 17.8 mW.

key words: *dual-loop clock and data recovery (CDR), phase interpolator, phase resolution*

1. Introduction

As demands for a large amount of data traffic increase, high-speed switch chips are becoming very important for network systems. Since dozens of transceivers are often integrated in a single switch chip, low power consumption, small die area, and robustness to switching noises coupled from adjacent blocks are required for Clock and Data Recovery circuits (CDRs) in each channel [1].

The dual-loop CDR has several advantages over a typical Phase-Locked Loop (PLL)-based structures. Because the dual-loop CDR generates a clock signal using phase interpolator (PI) instead of Voltage-Controlled Oscillator (VCO), the jitter is not accumulated in the phase tracking process. The dual-loop CDRs can be realized with either analog or digital control. The digitally-controlled type is more robust to noises and can be implemented in a relatively small area without physical capacitors. In a noisy environment subject to switching noises from adjacent digital logic cores, the digitally-controlled dual-loop CDR is widely used in the multi-channel applications [2], [3].

However, it can suffer from jitter performance degradation due to self-dithering [4]. This is caused by the nature of inherent discrete phase generation of the digitally-controlled phase interpolator. Consequently, the phase resolution of the digitally-controlled dual-loop CDR is a critical design parameter for jitter performance.

In this paper we propose a new configuration of digitally-controlled dual-loop CDR that has enhanced phase resolution. In Sects. 2 and 3, an overview of the conventional digitally-controlled dual-loop CDR and its problems are presented, respectively. The structure of a new CDR is given in Sect. 4. Section 5 shows experimental results of a prototype chip. Finally, conclusions are given in Sect. 6.

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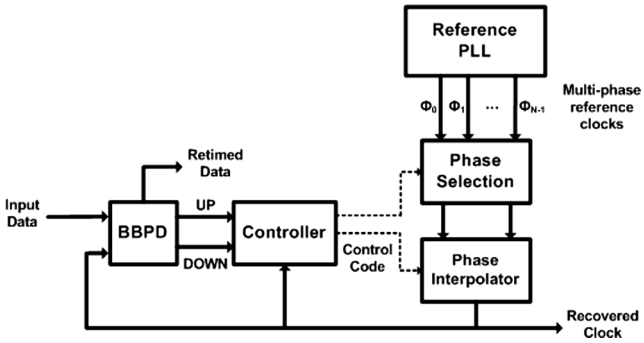


Fig. 1 Block diagram of conventional clock and data recovery circuit.

2. Conventional Digitally-Controlled Dual-Loop Clock and Data Recovery Circuit

A block diagram of the conventional digitally-controlled dual-loop CDR is shown in Fig. 1. The dual-loop CDRs share a reference PLL supplying reference clock signals. The CDR core consists of Bang-Bang Phase Detector (BBPD), controller, phase selection circuit and PI. The CDR receives an even number of reference clock signals having equally spaced and uniformly distributed phases from the reference PLL. The phase selection circuit takes two adjacent phases that contain the desired output phase. The PI produces the target phase by interpolating selected two phases. The BBPD compares phases of the interpolated clock and data so that the controller can produce the control word for the next output phase. It generates "UP" or "DOWN" pulse when the recovered clock has a later or earlier phase than data, respectively. Then, the controller decides the next phase that the phase selection circuit and PI should produce by counting up or down its state. As a whole, the CDR forms a negative feedback loop and aligns the clock to input data.

3. Effect and Limit of Phase Resolution

The phase resolution of the digital-controlled CDR is the most important factor which determines the CDR dynamic performance. Three important issues are: jitter generation, jitter suppression and frequency offset tracking ability.

Unlike analog-controlled CDR, digital-controlled CDR generates jitters even for clean input data having no jitters. Because it generates the quantized phase, the edge of recovered clock dithers around the edge of input data with the quantization error even in locked state. This quantization error is inversely proportional to the phase resolution. Moreover, some clock latencies in the loop degrade the jitter generation performance [5]. Specifically, additional one clock latency causes the output phase to dither more as many as two phase steps, one forward and one backward, and the CDR loop becomes more unstable.

In the aspect of the jitter suppression, the phase resolution is directly related to the open loop gain, or loop bandwidth. The phase step that the CDR can jump in one clock cycle is determined by the phase resolution. For a higher resolution the phase movement of the recovered clock is insignificant even if there are jitters in the input data. This means that the recovered clock does not track the input jitter well. Therefore, the higher phase resolution causes a narrower jitter bandwidth and better jitter rejection ability. Inversely, the CDR with the narrow jitter bandwidth can not track a large frequency offset. Since the transmitter and receiver are synchronized to different external oscillators, they usually operate at different frequencies. In most Ethernet standards, frequency offset up to ± 100 ppm is allowed. Consequently, the CDR should track the maximum frequency offset of 200 ppm in the worst case.

The phase resolution of CDR is lower-bounded by the frequency offset tracking ability and upper-bounded by both jitter generation and suppression performance. Phase resolution should be increased to reduce the jitter generation and reject the input jitter sufficiently, but limited not to lose locking by frequency offset.

A typical structure of digitally-controlled PI is shown in Fig. 2. It performs weighted-sum of two quadrature clock signals. The current DACs, which supply currents mapped to the weighting coefficients for each of two clocks, can be constructed in two types, binary-weighted and thermometer type. The binary-weighted DAC is simpler and more efficient than the thermometer DAC. However, the binary-weighted DAC has a critical drawback in dynamic current-switching. When the Most Significant Bit (MSB) is turned on or off and a large current source is instantly activated, the current overshoot and dynamic phase jump can happen. The amount of phase overshoot is about 5.6° even in 4-bit controlled PI in circuit-level simulation. Therefore, more phase overshoot is expected for higher phase resolution. On the other hand, there is no current overshoot in thermometer DAC since it has no large current source. But it is very bulky especially for higher resolution DAC.

It is very difficult to realize the PI which has phase resolution higher than 4-bit, i.e. 16-level, with small area and no dynamic overshoot in both types. By using 4-phase reference clocks, the total phase resolution of CDR is increased to four times of PI resolution. Consequently, 6-bit CDR with 4-phase reference clocks and 4-bit PI has the minimum phase step of 5.63°. Considering clock latencies more than two cycles by the BBPD and controller, it is not small enough since peak-to-peak self-dithering becomes ±3 phase steps, or 33.75°, at least.

4. Proposed Digitally-Controlled Dual-Loop Clock and Data Recovery Circuit

A new structure of digitally-controlled dual-loop CDR with enhanced phase resolution is presented in Fig. 3. As a whole, the dual-loop system consists of reference PLL and CDR core. The CDR core receives two differential quadrature phase clocks from the reference PLL. Two 2:1 MUXs make up two adjacent phases that contain the desired phase by selecting the inverted or non-inverted version of the reference clocks. For the purpose that the CDR has a simple structure but higher phase resolution, the target phase is generated by the combination of 16-level thermometer PI and Digitally-Controlled Delay Buffer (DCDB) having 4-level variable propagation delay. By fine tuning of the in-

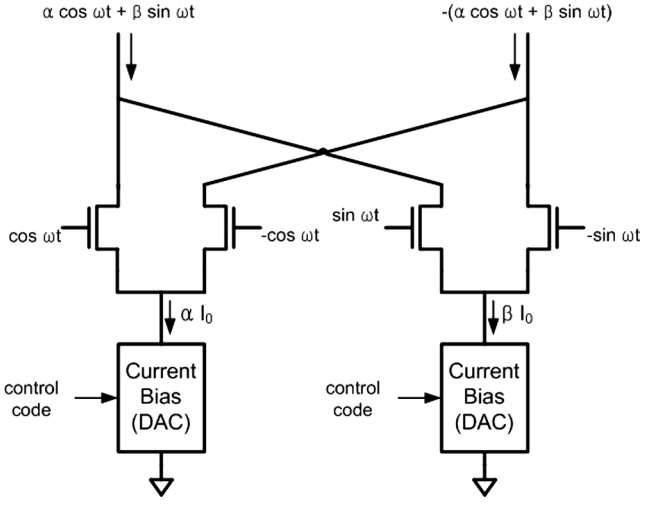


Fig. 2 Schematic of phase interpolator.

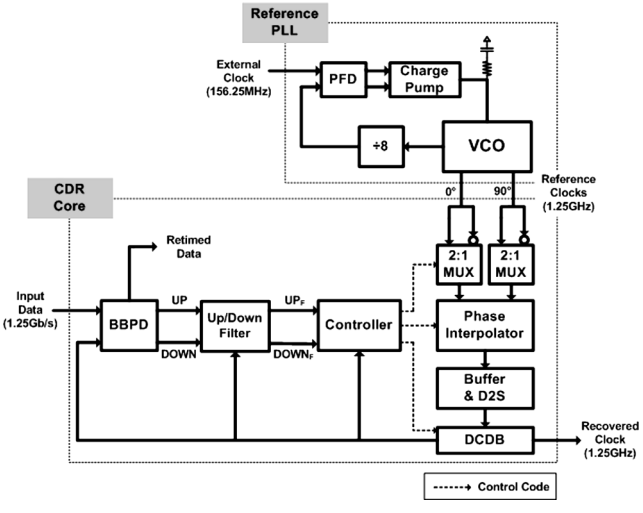


Fig. 3 Block diagram of the proposed clock and data recovery circuit.

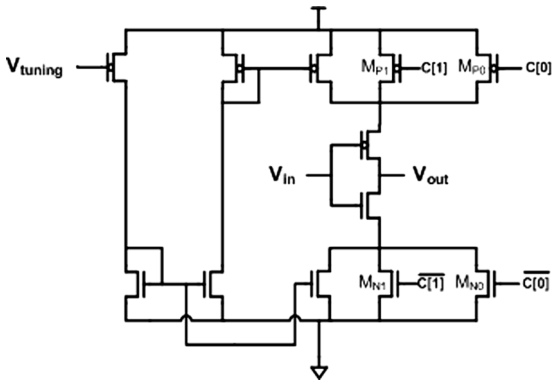


Fig. 4 Schematic of digitally-controlled delay buffer.

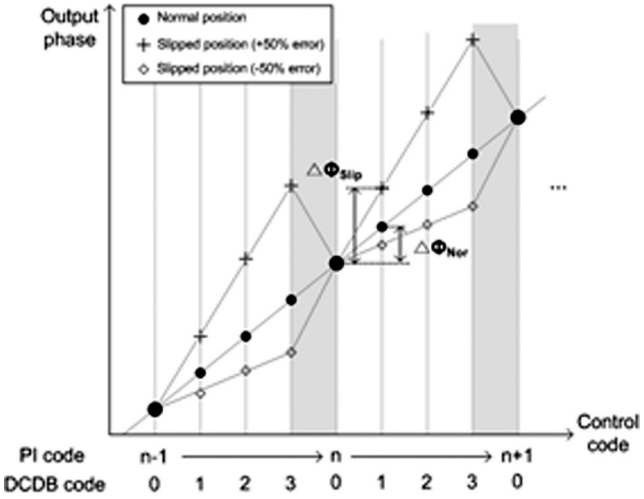
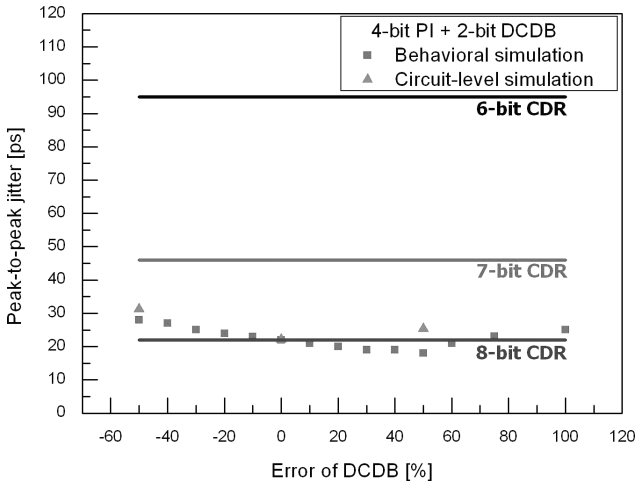


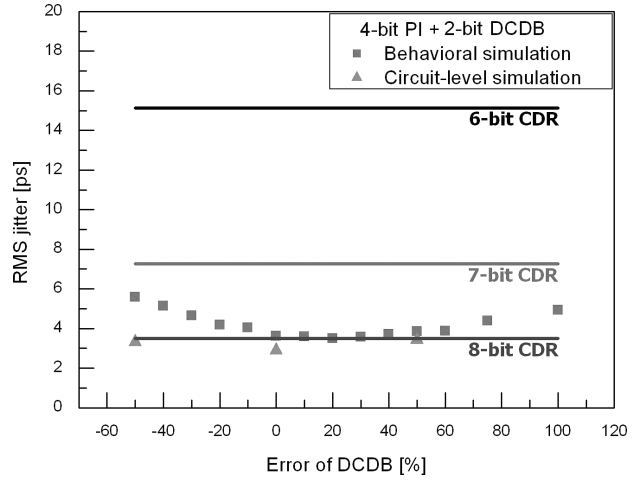
Fig. 5 Concept of delay error of DCDB.

terpolated phase, the DCDB increases the total phase resolution multiplied by four without more reference clock phases. Since the DCDB is a simple current-starved CMOS inverter as shown in Fig. 4, only a small amount of additional die area and power consumption is required. The DCDB was designed so that its delay can be controlled by the tuning voltage V_{tuning} for the purpose of testing. The 2-bit up/down filter after the BBPD reduces unwanted phase dithering by generating output pulses only when two and three consecutive UP or DOWN pulses are produced [6], respectively.

It is not guaranteed that the DCDB provides the exact amount of desired delay due to variations of process, supply voltages, and temperature. When the DCDB delay is different from the desired value, the phase transfer curve can be non-monotonic as well as nonlinear as illustrated in Fig. 5. In the figure, large black circles correspond to the output phases of PI. Three small circles between adjacent large black circles are the delayed version of PI output phase by DCDB, respectively. Crosses and diamonds deviating from the black circles correspond to the slipped output phases of DCDB with +50% and −50% error, respectively. Shadowed regions are where the phase transfer is suddenly changed. In this work, delay error of DCDB is defined as follows.



(a)



(b)

Fig. 6 Jitter generation vs. delay error of DCDB (a) Peak-to-peak jitter (b) RMS jitter.

$$Err_{DCDB}(\%) = \frac{\Delta\phi_{Slip} - \Delta\phi_{Nor}}{\Delta\phi_{Nor}} \times 100 \quad (1)$$

where Err_{DCDB} is an defined delay error of DCDB, $\Delta\phi_{Slip}$ is a slipped phase step due to variations, and $\Delta\phi_{Nor}$ is a normal phase step.

Figures 6(a) and (b) show peak-to-peak and RMS jitter generation versus delay error of DCDB in behavioral simulation using CPPSIM [7]. All simulations were performed without input jitter and under 200 ppm frequency offset to verify jitter generation of the CDR. Three horizontal solid lines correspond to the simulated output jitter of conventional 6-bit, 7-bit and 8-bit CDR models using only 4-bit, 5-bit and 6-bit PI, respectively. Rectangular dots mean the jitter generation of the proposed CDR obtained by behavioral simulations for various amounts of delay errors from −50% to 100%. As a result, measured jitter performance of the proposed CDR is comparable to conventional 8-bit CDR for relatively wide range of DCDB error.

Although there are nonlinear and non-monotonic phase transfers at the edge of two interpolated phases with DCCB

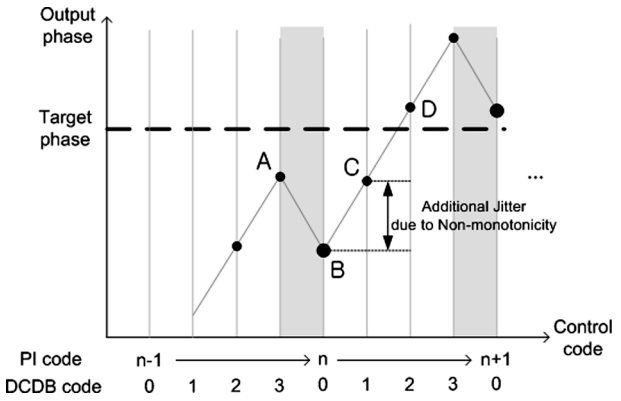


Fig. 7 Behavior of CDR loop with non-monotonic phase transfer.

delay error shown in the shaded region in Fig. 5, the entire effective phase resolution is clearly increased. Figure 7 shows the behavior of CDR loop with non-monotonic phase transfer due to DCDB error. Suppose that the output phase of the CDR is initially placed at the position *A* and the target phase is the dashed line. The BBPD in the CDR will generate UP pulse to advance the output phase but the actual next output phase will be at the position *B* due to the non-monotonicity. Therefore, the BBPD will generate UP pulses until the output phase reaches to the position *D*. The amount of additional jitter will be as much as one bit delay by DCDB. Since one-bit delay increases when DCDB has larger delay error, larger jitter generation will be caused by larger DCDB error. But this is not significant jitter because one-bit delay of DCDB is about 1.4°.

In circuit-level simulation, jitter generation performance of the CDR was also measured for various delay errors, which are shown as triangles in Figs. 6(a) and (b). The delay error was set by the manual control of V_{tuning}. It was also observed that the jitter generation level is flat for a wide variation of delay errors. It appears that metastability of D-flipflops in the BBPD allows some dead-zones, which cause less dithering of the recovered clock in the circuit-level simulation than behavioral simulation as shown in the plots.

5. Experimental Result

The prototype chip was fabricated in 0.18 μm CMOS technology and the die photograph is presented in Fig. 8. The output jitter was measured at frequency offset of 200 ppm for various delay errors by tuning V_{tuning}. Figure 9 shows measured output clock signals for −50% (a) and 50% delay error (b) of DCDB. Measured peak-to-peak and RMS jitters are plotted in Fig. 10. Flat jitter performance for DCDB was verified for DCDB errors ranging from −50% to 50%. For errors exceeding 100%, however, the output jitter rapidly increases since phase transfer characteristics of PI and DCDB becomes severely nonlinear. Overall jitter performance is degraded compared to simulation results, probably due to jitters and noised from PLL and output buffers.

Table 1 summarizes the performance of the CDR. The

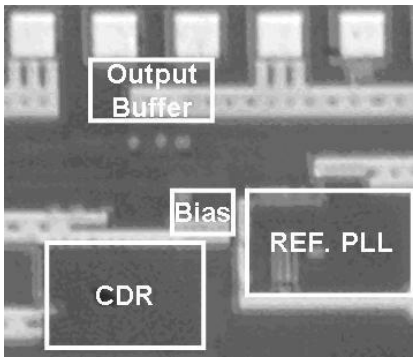
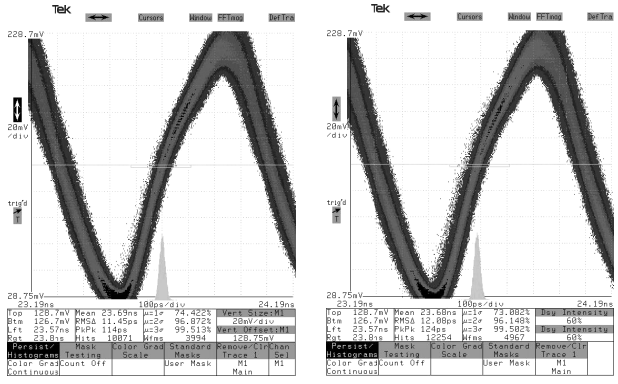


Fig. 8 Die photograph.



(a) (b)

Fig. 9 Measured waveform of the recovered clock (a) −50% delay error (b) +50% delay error.

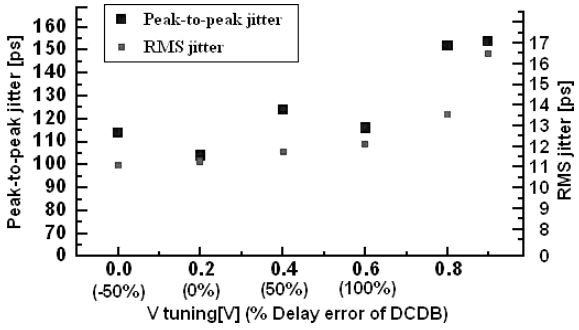


Fig. 10 Measured output jitter vs. delay error of digitally-controlled delay buffer.

Table 1 Chip summary.

Process	0.18 μm CMOS
Power consumption	17.8 mW (CDR core)
Die area	CDR core : 165 × 255 μm^2
Frequency tolerance	± 400 ppm
Bit Error Rate	error-free (30 minutes)

CDR covered frequency offset of 400 ppm, which is wide enough for most Giga-bit Ethernet applications.

To evaluate jitter rejection ability, input jitter was added by transmitting input data with 200 ppm frequency offset through 2 m PCB trace with 3.5 m cable. As shown in

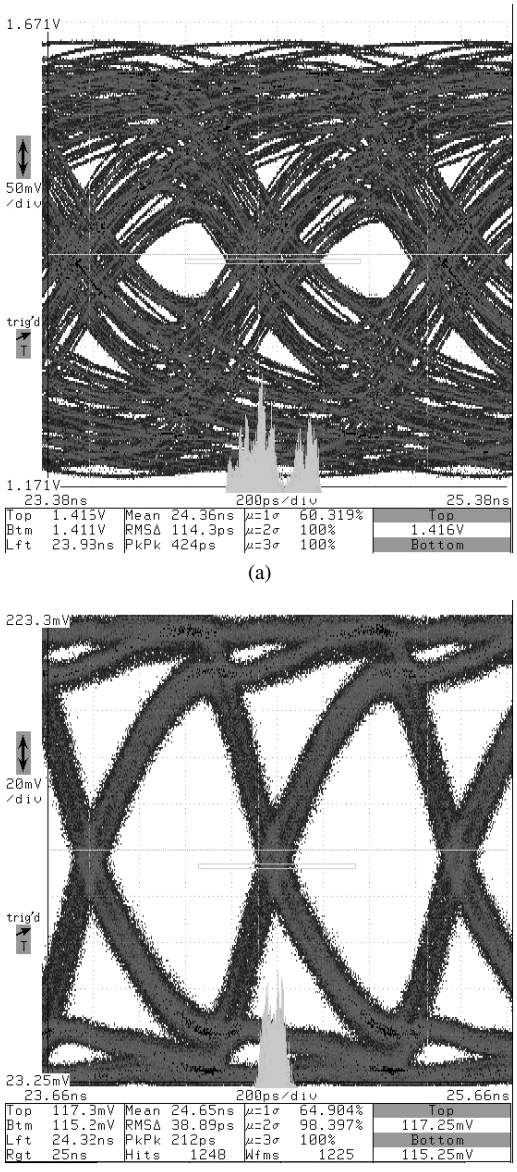


Fig. 11 Measured eye-pattern of transmitted data and retimed data (a) transmitted data through 2 m PCB trace and 3.5 m cable, $0.47UI_{p-p}$ eye opening (b) recovered data : $0.735UI_{p-p}$ eye opening.

Fig. 11, the CDR successfully recovered data from severely closed data. The CDR operated without bit errors at least for 30 minutes.

6. Conclusion

This paper presents a new configuration of digitally-controlled dual-loop CDR to increase effective phase resolution. The phase resolution can be easily increased by inserting DCDB with little additional power and chip-area. It is verified that the DCDB improves the jitter performance for the wide range of delay error. A prototype chip is fabricated in 0.18 μm CMOS technology. The CDR achieves 256-level, or 8-bit, effective phase resolution and can cover ±400 ppm frequency offset. The chip consumes 17.8 mW at 1.8 V and has the area of $255 \times 165\,\mu m^2$.

Acknowledgments

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