1.25/2.5-Gb/s Dual Bit-Rate Burst-Mode Clock Recovery Circuits in 0.18-μm CMOS Technology

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***Abstract*—A burst-mode clock recovery circuit with a novel dual bit-rate structure is presented. It utilizes two gated oscillators to align the clock with data edges and can operate in half-rate clocking mode, doubling data throughput, as well as in full-rate clocking mode. The gated oscillator reset-phase control scheme causes the starting phase of gated oscillators to alternate repeatedly between 0° and 180° according to the current clock phase. A prototype chip was designed with the 0.18-μm CMOS technology, and a 1.25/2.5-Gb/s dual-mode operation was verified by measurement.**

***Index Terms*—Burst-mode clock recovery, dual bit rate, gated oscillator, passive optical network (PON).**

I. Introduction

CLOCK recovery techniques based on phase-locked loop (PLL) or surface acoustic wave filters take a major portion of commercial clock recovery chips because of their excellent jitter suppression performances. However, they are not suitable for burst-mode receivers since it takes too much clock acquisition time (long preamble bits) for them to acquire clock phases from data packets. Fast clock acquisition is a major requirement for burst-mode receivers.

A number of fast clock acquisition techniques [1]–[3] for burst-mode clock recovery have been proposed so far. Among them, the gated oscillator approach [1], [2] provides instantaneous locking with a very simple structure. It is a very attractive solution for such burst-mode applications as local area network and passive optical network (PON) in which jitter accumulation is not a major problem [4], since no repeaters are required. In addition, all-pass characteristics of the gated-oscillator-based clock recovery scheme offer decent jitter tolerance up to high frequency [5].

Recently published gigabit-rate PON standards (e.g., gigabit PON and Ethernet PON) [6], [7] use burst-mode transmission at 1.25 Gb/s, and it is expected to be doubled to 2.5 Gb/s in the near future. Therefore, a dual bit-rate clock recovery circuit that supports both 1.25 and 2.5 Gb/s can be very useful. In this paper, we present a novel burst-mode clock recovery circuit that can operate in half-rate mode, doubling the data rate, as well as in full-rate clocking mode.

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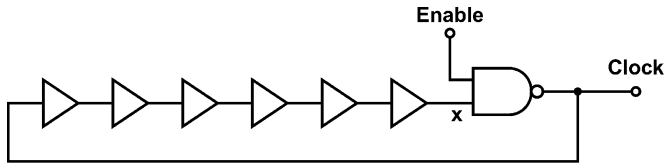

Fig. 1. Schematic diagram of gated oscillator.

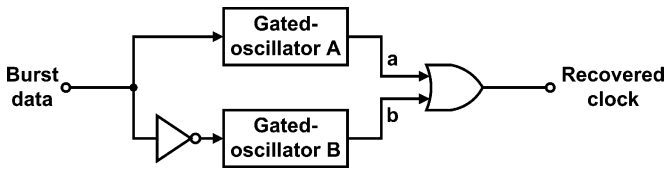

Fig. 2. Schematic diagram of GOCRC.

II. Gated-Oscillator-Based Clock Recovery

Fig. 1 shows a schematic diagram of a gated oscillator. A delay line and a gate stage, which are depicted as a NAND gate, make a ring oscillator. The gate stage is a switch that opens and shorts the clock output path. It can be realized with a logic gate as well as a multiplexer. When "Enable" is high, "Clock" is inverted "x," which forms a feedback for oscillation.

When "Enable" goes to low, "Clock" goes to high by the NAND gate no matter what "x," is, and the oscillation stops. Oscillation can be restarted by setting "Enable" high. This operation forces the oscillation to start with the falling edge or 0° clock phase. Consequently, the "Clock" signal is automatically aligned with the "Enable" signal.

Gated-oscillator-based clock recovery circuit (GOCRC) utilizes this capacity to align clock signals to data bits. Fig. 2 shows the schematic diagram of GOCRC. Two gated oscillators are turned on and off alternately by "Burst data" acting as an "Enable" signal.

In real circuit implementation, variable delay lines are used for gated oscillators so that voltage-controlled oscillators (VCOs) can be realized. The oscillation frequencies should be set in the vicinity of the data rate. This can be done by sharing the VCO control voltage of a PLL with a replica oscillator locked at the reference clock.

When "Burst data" is high, "Gated oscillator A" runs and generates data-aligned clock. When "Burst data" is low, "Gated oscillator B" runs and generates clock. Then, recovered clocks for each oscillator are combined by an OR gate to make the complete clock signal. Fig. 3 shows signal waveforms.

Even though the PLL uses an identical VCO for control voltage generation, there can be mismatches in oscillation frequencies among gated oscillators and the frequency biasing

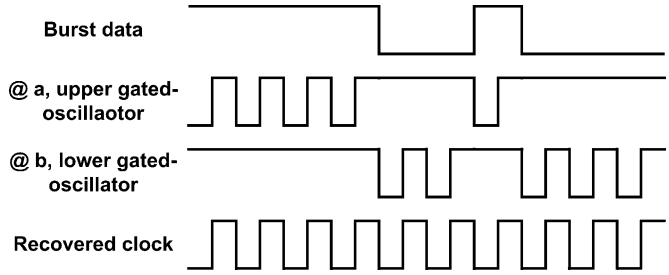

Fig. 3. Clock recovery using a gated oscillator pair.

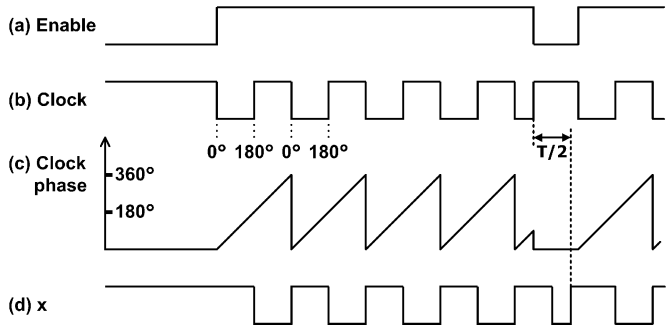

Fig. 4. Gated oscillator waveform in detail.

PLL. This mismatch causes a drift in clock phases when a long consecutive identical digit (CID) is applied. Therefore, run-length limiting coding scheme such as the 8b10b code is indispensable [5]. In our previous paper [8], it was found that oscillation frequencies of identical oscillator circuits fabricated on the same die can vary up to 2% or 3% in a typical CMOS process. Assuming that one oscillator is 3% faster or slower than the other, the 8b10b code whose maximum length of CID is five gives a clock-phase shift of 0.15 unit interval (UI) at worst case. This should be tolerable in most clock recovery applications.

III. Proposed Half-Rate Clock Recovery Principle

As described in Section II, the GOCRC shown in Fig. 2 aligns falling edges of the clock signal to data transitions. Consequently, rising edges can be used for bit decision because they should be at the midpoint of bits. In half-rate clocking, bits are located by both falling edges and rising edges. For GOCRC to do this, the gated oscillators should be able to align both rising edges and falling edges of clock to data transition, which cannot be done by GOCRC shown in Fig. 2.

Fig. 4 shows signal waveforms in gated oscillator in Fig. 1. As described in Fig. 4, low "Enable" makes both "Clock" and "x" to be fixed to high, bringing the clock phase to 0°. In half-rate clocking, there must be a way to bring and fix it to 180° to locate bits that come with rising edges. It takes half of the clock period for oscillation to be settled down, because even after the feedback path is opened, the clock signal will still propagate through the delay line until it reaches node "x." Therefore, once it stops, high "Enable" should be avoided during the next half clock period. This is a critical problem in half-rate clocking mode where it is possible that clock signals have to be realigned at every half clock period.

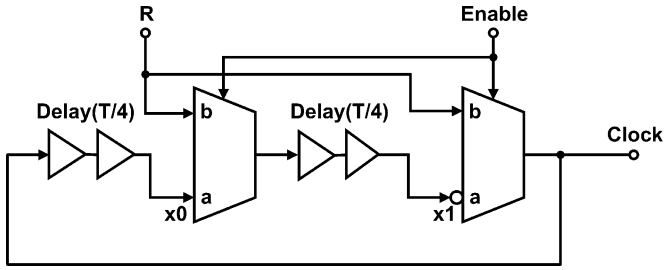

Fig. 5. Proposed gated oscillator circuit for half-rate clocking.

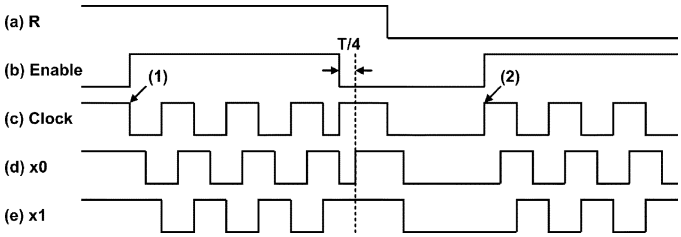

Fig. 6. Waveforms of proposed gated oscillator.

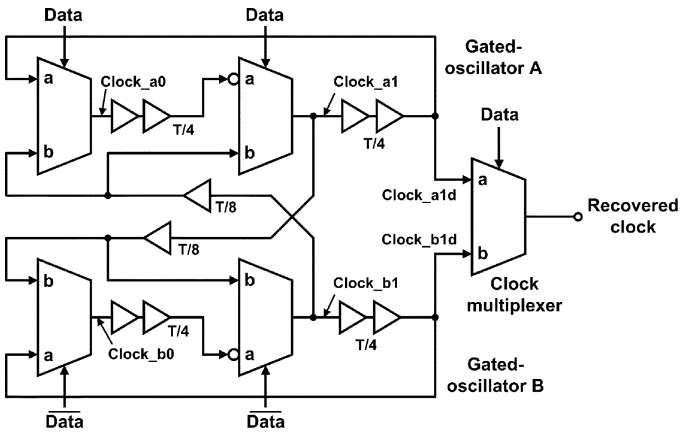

Fig. 7. Proposed dual bit-rate GOCRC.

With these observations, the gated oscillator structure is modified as shown in Fig. 5, in which high "Enable" selects "a" and low "Enable" selects "b."

Two multiplexers are used as gate stages that divide the delay line into two quarter-period lengths. Doing that, it becomes possible to select the proper clock phase for alignment between 0° and 180° by setting "R." Furthermore, it takes only a quarter clock period for a clock signal to propagate, because the delay line is chopped into T/4 lengths by gate stages. Waveforms in the operation are shown in Fig. 6. It is shown that the starting phase of the gated oscillator alternates between 0° and 180°, depending on "R." In Fig. 6, (1) and (2) correspond to cases starting from falling edge (0°) and starting from rising edge (180°), respectively.

Fig. 7 shows a half-rate clock recovery circuit implementation, and Fig. 8 shows the signal waveforms in its operation. The first bit, which is high, causes "Gated oscillator A" to oscillate. Then "Clock_a1" is automatically aligned to the data. In this case, the rising edge of the clock signal is aligned to the rising edge of the data signal. If the succeeding bits are still high,

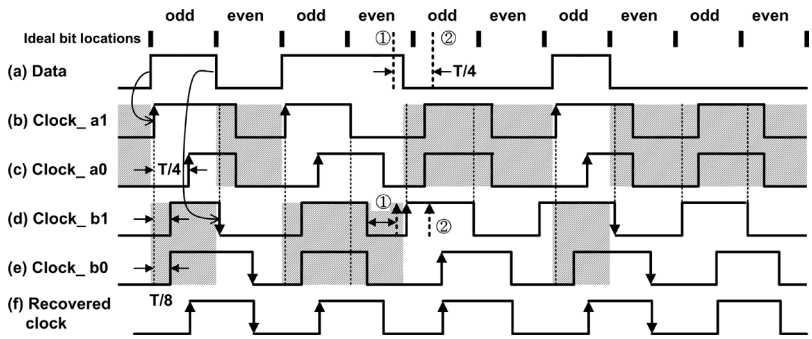

Fig. 8. Waveforms of proposed dual bit-rate GOCRC.

which means that "Data" is not changed, it will continue to oscillate and keep producing clock signal.

The second bit, which is low, causes "Gated oscillator A" to stop oscillation and "Gated oscillator B" to begin oscillation. Then "Clock_b1" is aligned to the data. Because "odd" bits and "even" bits have different clock phases (0° or 180°), gated oscillators have to track the clock signal even when they are stopped. If not, they will not know which clock phase they should produce when another data transition arrives. The shadowed regions show this tracking behavior. When "Data" is high, "Clock_a1" sets "Clock_b0" and "Clock_b1," and when "Data" is low, "Clock_b1" sets "Clock_a0" and "Clock_a1." T/8 delays are inserted in the paths to enhance jitter immunity. Without them, the stopped oscillator might be set up too early and miss data transitions right after wide bits. With them, the proposed circuit can tolerate wide bits as well as narrow bits, causing data transitions later and earlier up to T/8. Therefore, data transitions are allowed in T/4-wide widow. It is noted as (1) and (2) in Fig. 8. The narrow bit (1) will not guarantee oscillator settling time of T/4, and the wide bit (2) will set up the oscillator too early.

Each gated oscillator produces the half portion of the clock, and their T/4 delayed versions are combined by "Clock multiplexer" to locate the recovered clock at the midpoints of the data bits. The "Data" signal is used as the selector of clock multiplexer because its polarity reflects the oscillator generating clock at that time.

IV. Dual Bit-Rate Operation

Modified gated oscillator in Fig. 4 can also be used for full-rate clock recovery by fixing "R" to a constant logic value. Then, it will operate in the same way as the conventional one shown in Fig. 1.

By utilizing this programmability, the clock recovery circuit shown in Fig. 7 can be used for full-rate clock recovery as well as half-rate clock recovery. In our design, it was implemented by adding two multiplexers with a constant value for one input (not shown in Fig. 7) in the T/8 delay path. The additional multiplexers are controlled by the external mode-selection signal.

V. Simulation Results

A clock recovery circuit described earlier and a frequency biasing PLL were designed with the 0.18-μm CMOS technology, and its functionality was verified by SPICE simulation.

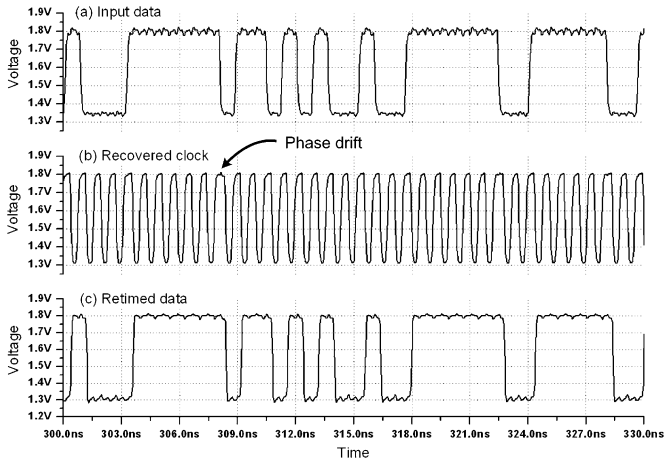

Fig. 9. Input data, recovered clock, and retimed data waveforms from 1.25-Gb/s full-rate clock recovery simulation. (a) and (c) 1000111111011010100100111111001111100.

Fig. 9 shows 1.25-Gb/s input bit stream, recovered clock signal and retimed data bits when it operates in full-rate clock recovery mode. MATLAB-generated random bit sequence was used for data input.

Fig. 10 shows 2.5-Gb/s input bit stream, recovered half-rate clock signal and data sampled at rising and falling edges when it operates in half-rate clocking mode.

Pulsewidth distortion (PWD) in recovered clock waveform after long CIDs were observed. It is caused by clock-phase drift due to frequency mismatch between the clock-recovering gated oscillator pair and the replica oscillator in frequency biasing PLLs, resulting in deterministic jitter. The 0.18- and 0.21-UI of peak-to-peak deterministic jitters were estimated for the 1.25- and 2.5-Gb/s operations, respectively, for 3% frequency mismatch when the maximum run length of CID was 5 bits. Data bits were correctly retimed because enough timing margin for decision is secured even with this amount of jitter.

VI. Prototype Chip and Measurement Results

Designed circuit was laid out and fabricated with the 0.18-μm CMOS technology. A prototype chip was directly attached to a test board assembly using the chip-on-board (COB) technique. Fig. 11 shows a microscopic photograph of the fabricated prototype chip. The clock recovery core occupies only 160 μm $\times$

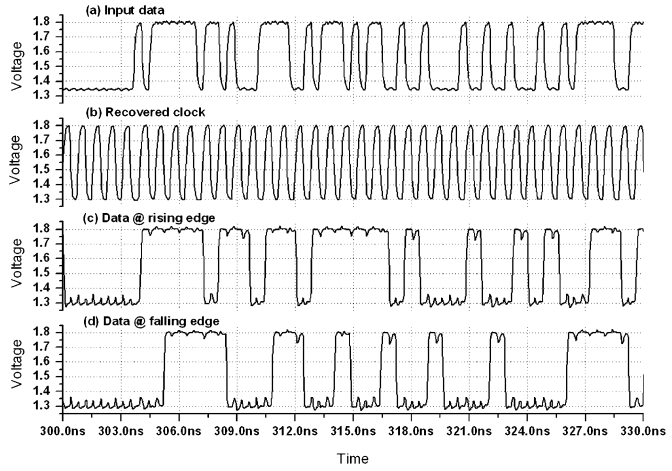

Fig. 10. Input data, recovered clock, and retimed data waveforms from 2.5-Gb/s half-rate clock recovery simulation. (a) . . .0000010111111011010001111001011101011001001000010010010001001000 (c) . . .00111101101101111101000100101001 10. (d) 0000111100011001001001000100001111.

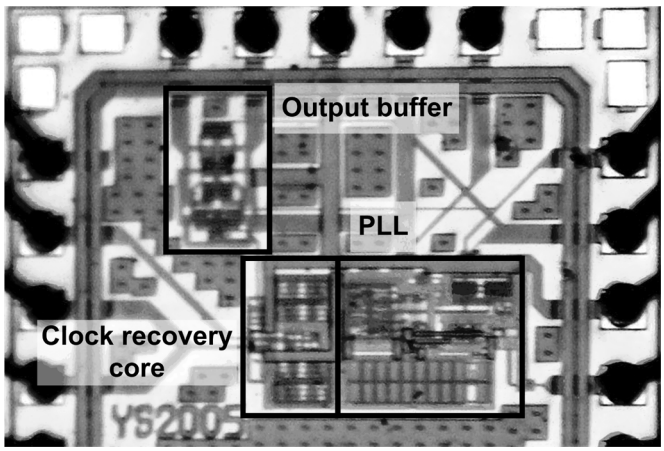

Fig. 11. Die photograph of the prototype chip.

250 μm, and the frequency biasing PLL requires 310 μm $\times$ 250 μm, including loop filter.

Figs. 12 and 13 show recovered clock waveforms and histograms of clock jitter from the 2^7-1 pseudorandom binary sequence (PRBS) pattern at 1.25 and 2.5 Gb/s, respectively. Measured clock jitters were around 100 ps peak-to-peak for both cases. Because the data source is virtually jitter free, observed jitters are entirely from the clock recovery circuit.

To verify instant phase alignment, intentional phase drift was introduced by a data sequence having long CIDs, and Fig. 14 describes how it affects the recovered clock. If the frequencies of gated oscillators in GOCRC are not equal to that of the frequency biasing PLL, the recovered clock edge drifts out of the center of data eye during the long CID interval. After that, GOCRC will bring back the clock edge to the center of data eye; therefore, an abrupt phase jump will be observed. Fig. 15 shows that instantaneous phase acquisition was successfully performed.

Frequency mismatch was calculated. Output clock frequency was measured with the spectrum analyzer for the input data

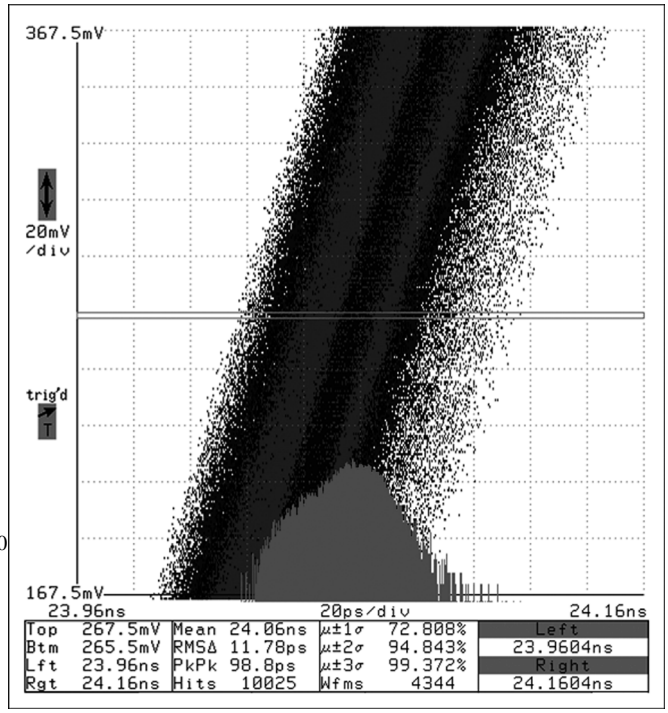

Fig. 12. Recovered clock from the 1.25-Gb/s 2^7-1 PRBS pattern.

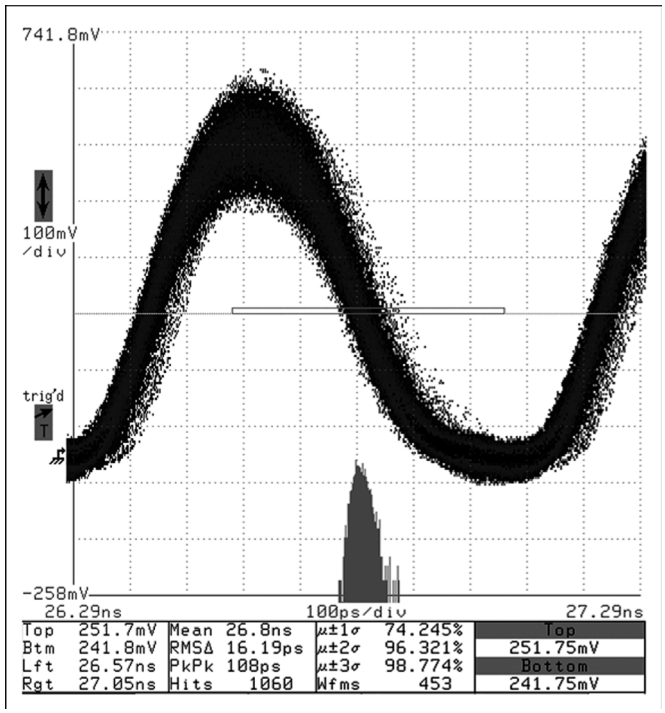

Fig. 13. Recovered clock from the 2.5-Gb/s 2^7-1 PRBS pattern.

pattern having all 1's. All 1's will make "Gated oscillator A" active. The same measurement was also performed with all-0 data pattern for "Gated oscillator B." The estimated frequency mismatch between gated oscillators A and B in clock recovery circuit was less than 2% over the entire operational frequency range.

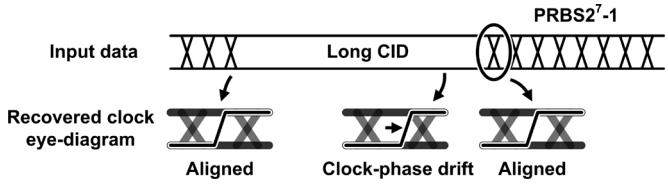

Fig. 14. Instantaneous phase acquisition after a long CID interval in case the clock-recovering gated oscillator pair leads to a frequency biasing PLL.

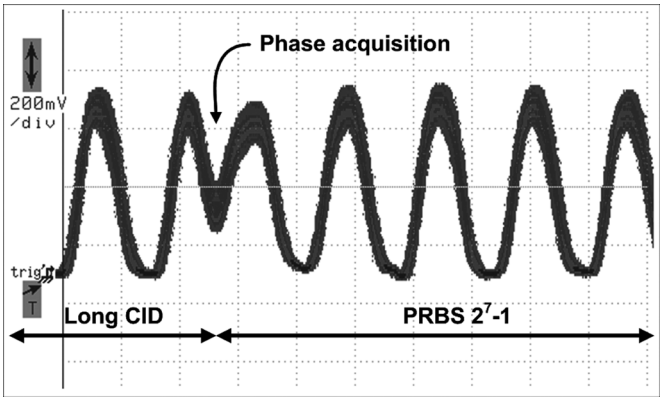

Fig. 15. Instantaneous phase acquisition.

VII. Conclusion

A novel structure for the dual bit-rate burst-mode clock recovery circuit was demonstrated. It can operate in half-rate clocking mode with the doubled operation speed as well as in full-rate clock recovery mode. Two operation modes can be easily selected by an external selection switch. The circuit was designed and laid out with the 0.18-μm CMOS technology, and a prototype chip was fabricated and tested.

Some PWD was observed in simulation, which was caused by the clock-phase drift due to frequency offset between oscillators in clock recovery circuit and frequency biasing PLL. This problem can be mitigated by using limited-CID coding scheme, e.g., 8b10b code, which limits the maximum run length of CID to 5 bits.

Estimated frequency mismatch between clock recovery gated oscillators is less than 2% over the entire operational frequency range, which agrees well with our previous paper and expectation. Careful design and layout will minimize the undesirable frequency mismatches.

For clock recovery measurements, the $2^7 - 1$ PRBS pattern, which has the maximum run length of 7 b, was used. Prototype chip successfully recovered full-rate and half-rate clock from each of the 1.25- and 2.5-Gb/s PRBS patterns. Table I sums up the measurement results.

TABLE I
Measurement Result Summary

Technology	0.18-μm CMOS
Nominal data-rate	1.25-Gb/s and 2.5-Gb/s (dual bit-rate)
Operational freq. range	1.1-Gb/s ~ 1.35Gb/s and 2.2Gb/s ~2.7Gb/s
Chip area	160-μm x 250-μm for core 310-μm x 250-μm for freq. biasing PLL
Max. tolerable CID	More than 7bits
Jitter generation	Around 100-ps p2p for 1.25-Gb/s and 2.5-Gb/s
Power supply	1.8V
Power consumption	60-mW for core, 50-mW for Output buffer

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