PAPER

A New 1.25-Gb/s Burst Mode Clock and Data Recovery Circuit Using Two Digital Phase Aligners and a Phase Interpolator

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SUMMARY We propose a new Clock and Data Recovery (CDR) circuit for burst-mode applications. It can recover clock signals after two data transitions and endure long sequence of consecutive identical digits. Two Digital Phase Aligners (DPAs), triggered by rising or falling edges of input data, recover clock signals, which are then combined by a phase interpolator. This configuration reduces the RMS jitters of the recovered clock by 30% and doubles the maximum run length compared to a previously reported DPA CDR. A prototype chip is demonstrated with 0.18-μm CMOS technology. Measurement results show that the chip operates without any bit error for 1.25-Gb/s $2^{31} - 1$ PRBS with 200-ppm frequency offset and recovers clock and data after two clock cycles.

key words: *burst-mode, clock and data recovery circuit, digital phase aligner, phase interpolator*

1. Introduction

Clock and Data Recovery (CDR) circuits should handle data packets with different phases in burst-mode applications such as Passive Optical Network (PON) and Local Area Network (LAN). For these applications, CDR circuits are required to have fast acquisition time and good immunity for long consecutive identical digits (CID). In Gigabit-capable PON (GPON) specification, for example, the preamble of 44 bits and the minimum CID immunity of 72 bits are suggested for 1244.16 Mb/s data rate [1].

Gated-Oscillator CDR circuits, which can be locked to the incoming burst data within a few bits of the preamble, have been proposed for burst-mode applications [2], [3]. However, they can not handle long CID because of the frequency mismatch between reference and gated clocks [2]. Over-sampling CDR circuits have been also proposed as a solution for burst-mode applications [4]. Although they can overcome above problems and are robust to noises and PVT variations with their digital nature, they require complex algorithms and large power consumption.

CDR circuits with Digital Phase Aligners (DPA CDR) have been introduced for switch applications [5], [6]. They have the all-digital structure along with simpler phase tracking algorithms than over-sampling CDR. The synchronous DPA CDR circuit proposed in [5] samples input data using multi-phase clocks and finds the best clock among them. Since the input data is sampled by clocks having different phases, however, a post-process is needed to re-align sampled data to one phase, increasing hardware complexity, power consumption, and internal clock latency. Another DPA CDR proposed by H.Y. Jung, B.C. Lee, and K.C. Park provides a simple solution by sampling multi-phase clocks with input data in order to eliminate the re-align process [6]. But it uses only the rising edge of input data in recovering clock, while the timing information of the falling edge is ignored.

We propose a new CDR structure using both rising and falling edges with two DPAs and a Phase Interpolator (PI), which can perform burst-mode CDR operation. Details of the proposed structure and its operation are given in Sect. 2. Section 3 shows measurement results of a prototype chip. Conclusions are given in Sect. 4.

2. Circuit Structure

Figure 1 shows the block diagram of previously reported Single DPA CDR (SDPA CDR) [6]. It consists of a DPA, a phase interpolator, a delay line, and a D-flip-flop. DPA receives data input and N reference clocks having equal spacing in phase. Among N reference clocks, DPA selects the clock that best matches the rising edges of input data. A delay line is inserted between data input and D-flip-flop in order to compensate DPA gate delay. The N-phase reference clock signals are generated by a Phase-Lock Loop (PLL) and a multi-phase generator (not shown in Fig. 1). Since the recovered clock is aligned only to the rising edge of input data, timing information of the falling edge is ignored. To overcome this drawback, we propose Double DPA CDR (DDPA CDR) using both edges of input data.

The structure of N-input DPA, which is used in proposed structure, is shown in Fig. 2. Note that the Ref. [6] does not specify detailed structure of DPA. To select the best clock signal, N reference clocks are sampled at rising edges of input data by N D-flip-flops, simultaneously. An example

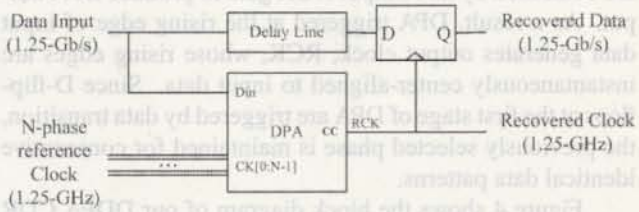

Fig. 1 Block diagram of SDPA CDR.

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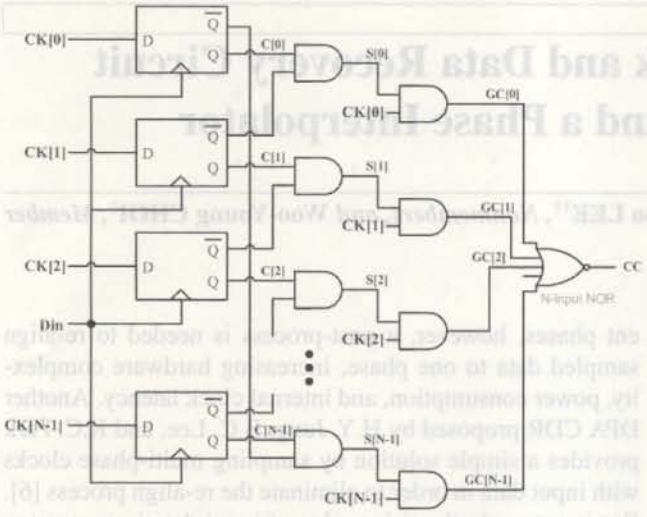

Fig. 2 Schematic of N-input DPA.

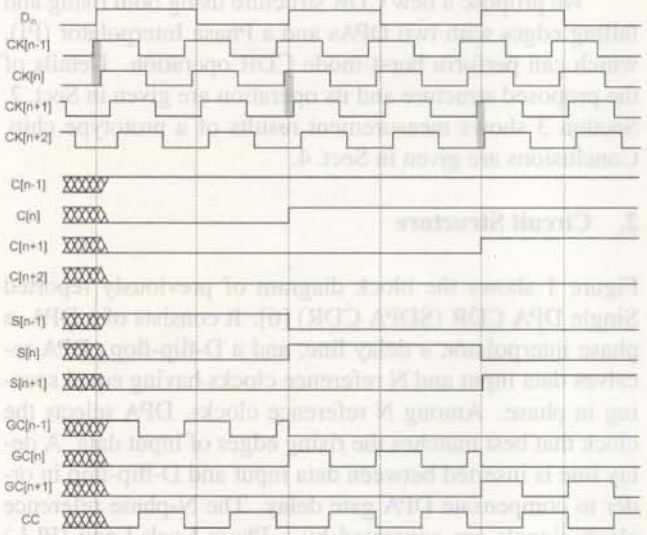

Fig. 3 Timing diagram of N-input DPA.

is shown in Fig. 3. Since the first rising edge of input data is located between rising edges of CK[n−1] and CK[n] in this example, C[n−1] is high but C[n], C[n+1] and C[n+2] are low. This enables only S[n−1] so that GC[n−1] has the gated clock. When the second rising edge of input data falls between rising edges of CK[n] and CK[n+1] due to jitters, S[n] goes to high instead of S[n−1] and GC[n] has the clock instead of GC[n−1]. The gated clocks GC[0] to GC[N−1] are combined by an N-input NOR gate to produce DPA output. As a result, DPA triggered at the rising edge of input data generates output clock, RCK, whose rising edges are instantaneously center-aligned to input data. Since D-flip-flops at the first stage of DPA are triggered by data transition, the previously selected phase is maintained for consecutive identical data patterns.

Figure 4 shows the block diagram of our DDPA CDR circuit using two DPAs (one positive and the other negative)

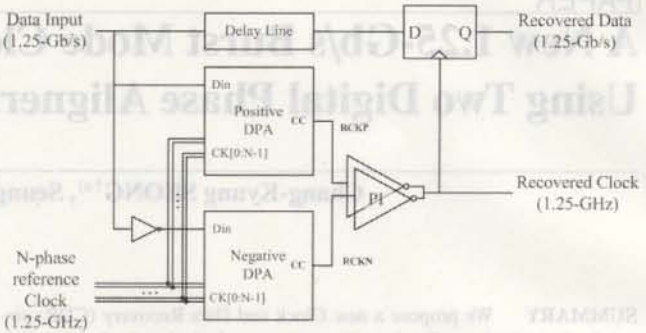

Fig. 4 Block diagram of DDPA CDR.

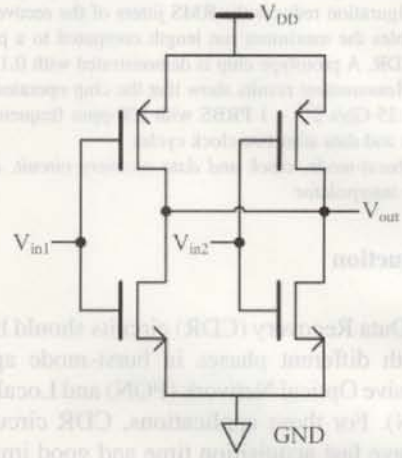

Fig. 5 Schematic of phase interpolator.

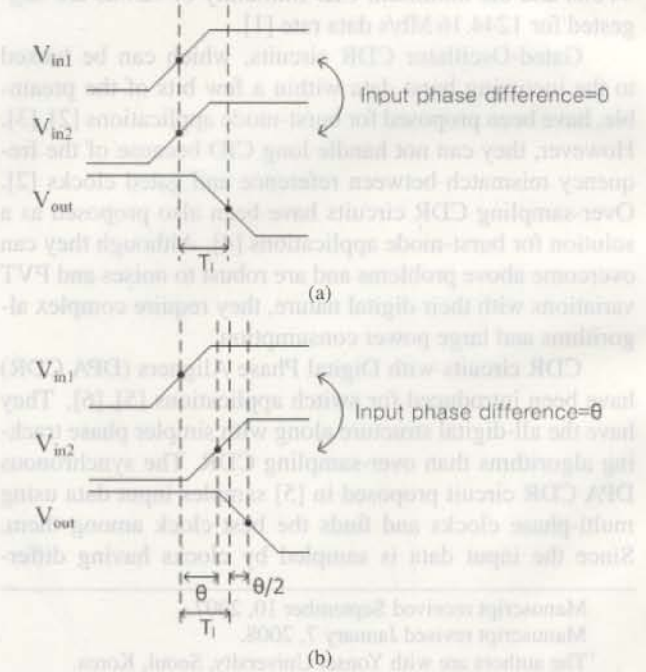

Fig. 6 Phase interpolation by phase interpolator: (a) results in only intrinsic delay T_i for input phase difference of 0 (b) results in intrinsic delay T_i and $\theta/2$ for input phase difference of θ.

and a PI. Positive DPA selects the clock that best matches the rising edges of input data, and negative DPA the falling edges. Selected clock signals are combined by a PI which produces the recovered clock having the average phase. The schematic of PI used in DDPA CDR is given in Fig. 5. A single-ended PI consists of two identical CMOS inverters. For two input signals having no phase difference, PI generates the inverted version of two identical input signals with intrinsic gate delay T_i as illustrated in Fig. 6(a). For two input signals having phase difference of θ, however, gate delay by PI increases as much as the half of input phase difference, i.e., $\theta/2$, as shown in Fig. 6(b). In order to verify the characteristic of output phase as function of input phase difference, HSPICE simulation was done for PI using 0.18-μm CMOS technology parameters and the results are shown in Fig. 7. The ideal output phase is shown as a dotted line in which the output phase is exactly the half of input phase difference without considering the intrinsic gate delay T_i. Although output phase deviates from the ideal line for larger input phase difference, the amount of error is not much having, for example, error of 3.61° for input phase difference of 90°.

Figure 8 shows a timing diagram of DDPA CDR with PI. The recovered clock RCK, which is merged from RCKP and RCKN by PI, has the average phase of the most recent phase values of RCKP and RCKN. As input data phases change from the rising to falling edges, two clocks from DPAs, RCKP and RCKN, may have different phases. For example, data edges numbered 1 and 2 (or 3 and 4, or 5 and 6) in Fig. 8 are positioned in different phase intervals. These make RCKP and RCKN have different phases and the average value is produced for RCK by PI. However, the same clocks are selected for the adjacent edges having the same phases as data edges numbered 2 and 3, and 4 and 5. Therefore, abrupt phase changes in RCK are reduced by the moving average. Also, this performs low-pass filtering on input jitters, removing high-frequency jitters.

Moreover, utilization of both edges in clock recovery reduces the phase drift during long CID. While SDPA CDR considers long 1's followed by long 0's as one piece of CID by ignoring the falling edge of input data, DDPA CDR considers them as two independent CIDs since it utilizes both edges. Therefore, DDPA CDR results in less phase drift than SDPA CDR for the same data patterns. This also means that DDPA CDR is more immune to long CID.

In order to compare performances, SDPA CDR and DDPA CDR structures are simulated in the behavioral level using CppSim, which is a time-step based behavioral simulator [7]. For implementation, we used 8-phase clocks with 45° phase steps. Input data having 0.375 UI (peak-to-peak) of eye closure due to uniformly distributed jitters and 200-ppm frequency offset are used. Note that the frequency offset specifications for most physical layer link standards are ±100-ppm. The recovered clock output jitters are compared in Fig. 9. The results show 0.375 UI peak-to-peak output jitters for both DPA CDR structures that are due to the limited quantization resolution of 8-clock phases. However, RMS jitters of DDPA CDR are smaller by about 30% (65.94 ps vs. 93.89 ps).

In Fig. 10, HSPICE simulation results for burst-mode data input show that the recovered clock appears after '10' pattern of input data and the rising edge of the clock is ready to sample the data. Since RCKP and RCKN start off at rising and falling edges of input data, respectively, PI begins

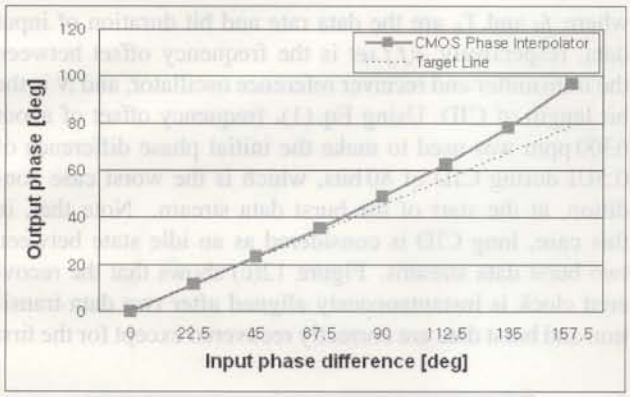

Fig. 7 Characteristic curve of phase interpolator.

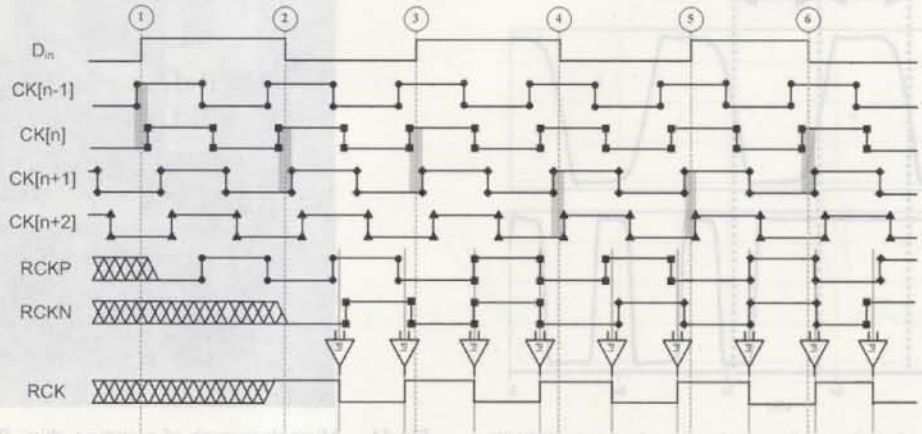

Fig. 8 Timing diagram of DDPA CDR.

to merge recovered clock signals after one rising and one falling edge. The acquisition time of DDPA CDR is two clock cycle for the preamble sequences starting with '10' pattern. With gate delays in DPAs and phase interpolator, the rising edge of the recovered clock is not center-aligned to data. Therefore, a delay line which consists of an inverter chain is inserted between input data node and D-flip-flop for data retiming.

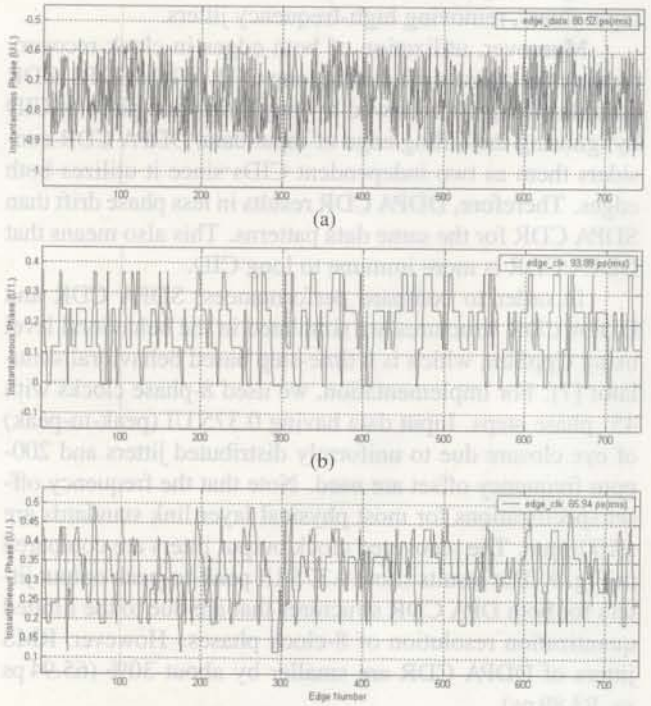

Fig. 9 Comparison of jitter performance for 0.375 $UI_{p\text{-}p}$ input jitter: (a) input data jitter (b) the output jitter of conventional circuit (c) the output jitter of proposed circuit.

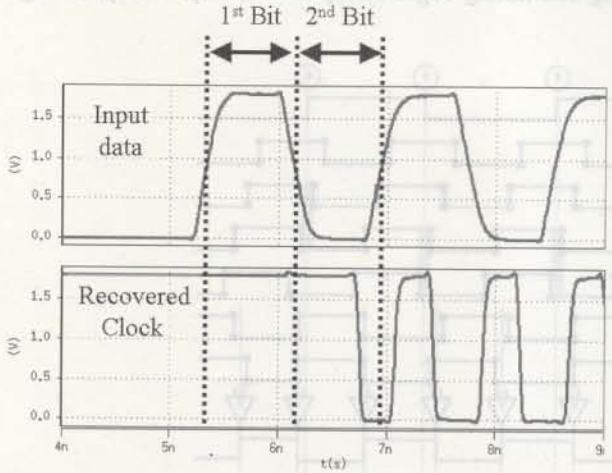

Fig. 10 Initial recovered clock waveform for burst-mode data in HSPICE simulation.

3. Measurement Results

The proposed DDPA CDR circuit was fabricated with 0.18-μm 1-poly and 6-metal CMOS process technology. The microphotograph of the prototype chip is shown in Fig. 11. The reference PLL was designed to have an external second-order loop filter to make the loop bandwidth approximately 1/100 of the external reference frequency, 156.25-MHz. The CDR core occupies $230 \times 310\,\mu m^2$ including 8-phase clock generator.

In order to verify the CDR performance, 80 bits of 0's were inserted in the middle of 1.25-Gb/s data stream as shown in Fig. 12(a). For frequency offset of 200 ppm between input data and the reference clock, the phase drift during 80 bits of 0's is not much and the CDR circuit performs successfully as shown in Fig. 12(b). In addition, a very large value of frequency offset was needed in order to verify the instantaneous acquisition ability with the initial out-of-phase condition for burst-mode data. The phase drift ϕ_{drift} during N bit-long CID due to frequency offset can be calculated by the following equation;

$$\phi_{drift}[UI] = \frac{\frac{1}{f_0} - \frac{1}{f_0(1+offset)}}{T_b} = \frac{offset}{1+offset}N, \qquad (1)$$

where f_0 and T_b are the data rate and bit duration of input data, respectively, $offset$ is the frequency offset between the transmitter and receiver reference oscillator, and N is the bit length of CID. Using Eq. (1), frequency offset of about 6300 ppm was used to make the initial phase difference of 0.5UI during CID of 80 bits, which is the worst case condition, at the start of the burst data stream. Note that, in this case, long CID is considered as an idle state between two burst data streams. Figure 12(c) shows that the recovered clock is instantaneously aligned after two data transition and burst data are correctly recovered except for the first

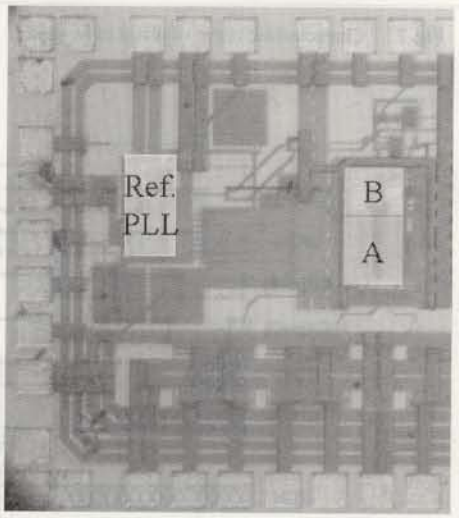

Fig. 11 Microphotograph of prototype chip: Part A and B are DDPA CDR core and 8-phase clock generator, respectively.

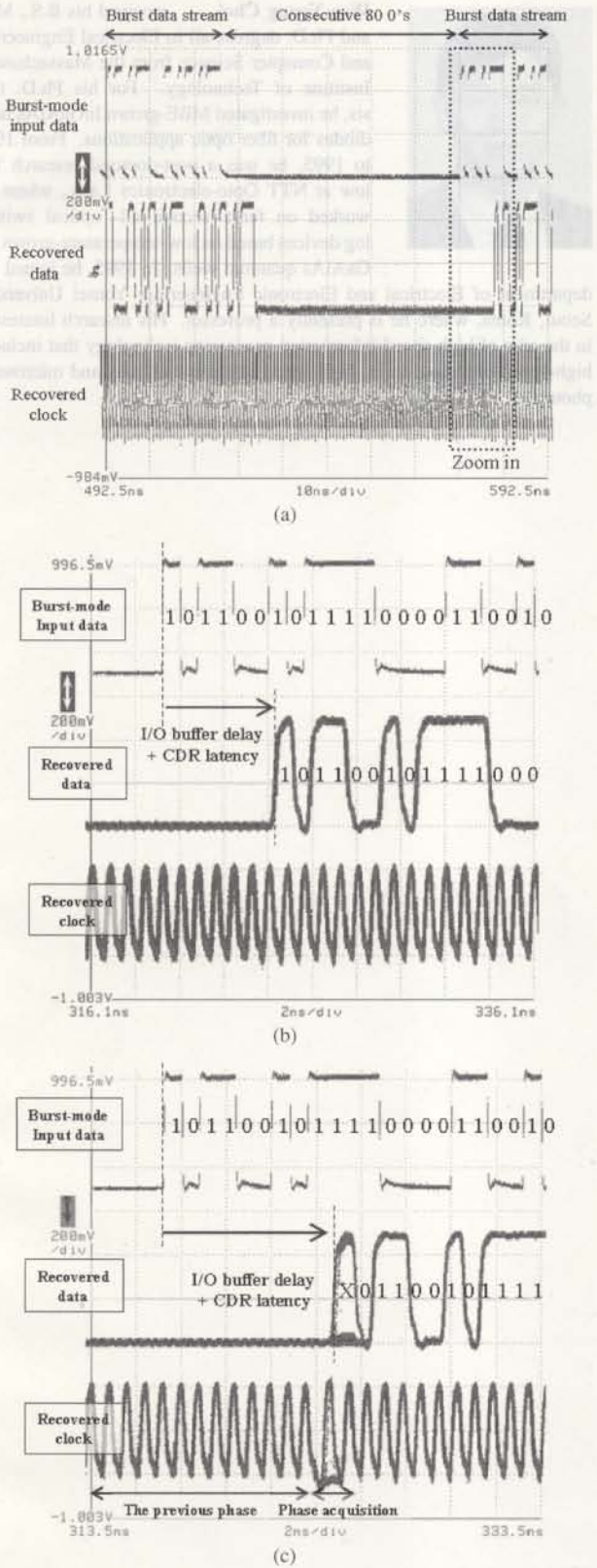

Fig. 12 Burst-mode operation of proposed CDR (a) Burst data stream after 80-bit long consecutive 0's (b) Zoomed-in waveform at the start of burst data stream for 200 ppm frequency offset (c) Zoomed-in waveform at the start of burst data stream for about 6300 ppm frequency offset (out-of-phase condition).

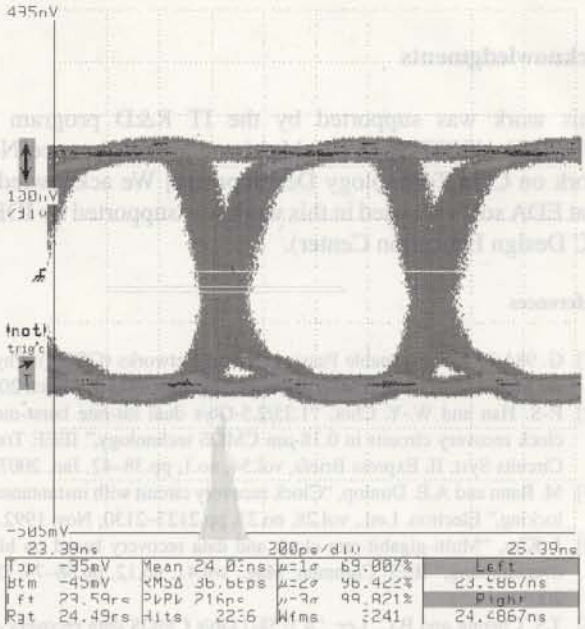

Fig. 13 Eye diagram of the recovered data for $2^{31} - 1$ PRBS pattern.

Table 1 Chip summary.

Parameter	Value
Process technology	0.18 μm 1-poly 6-metal CMOS
Supply voltage	2.2 V
Circuit area	$230 \times 310\,\mu m^2$
Power consumption	29 mW
Acquisition time	2 data transition
FrEq. offset tolerance	$> \pm 200$ ppm
Bit Error Rate	No error with $2^{31} - 1$ PRBS at 1.25-Gb/s

two bits.

Figure 13 shows the measured eye diagram of the recovered clock for 1.25-Gb/s $2^{31} - 1$ PRBS with 200 ppm frequency offset. The width and height of opening eye are 636 ps, or 0.795UI, and 400 mV, respectively. The prototype chip results in no bit error during measurement. The performance of the chip is summarized in Table 1.

4. Conclusion

A new DPA CDR circuit operating at 1.25-Gb/s is proposed and realized with 0.18-μm CMOS technology. The DDPA CDR has the fast acquisition ability and strong immunity to long CID, and it is suitable for burst-mode applications such as PON and multi-channel switches. Using a phase interpolator to merge two clock signals, each of which aligned to rising or falling edges of input data respectively, RMS jitter reduction of 30% and enhancement of CID immunity are achieved. It consumes only 29 mW and has a small chip area of $230 \times 310\,\mu m^2$ per channel. Experimental results show error free operation for 1.25-Gb/s $2^{31} - 1$ PRBS data having 200-ppm frequency offset and instantaneous phase acquisition after two data transition.

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