A 622-Mb/s Mixed-Mode BPSK Demodulator Using a Half-Rate Bang-Bang Phase Detector

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***Abstract*—A new mixed-mode binary phase shift keying (BPSK) demodulator is demonstrated using a half-rate bang-bang phase detector commonly used in clock and data recovery (CDR) applications. This demodulator can be used for new home networking applications using already installed CATV lines. A prototype chip realized by 0.18-μm CMOS process can demodulate 622-Mb/s data at 1.4-GHz carrier frequency. At this data rate, the demodulator core consumes 27.5 mW from a 1.8 V power supply while the core chip area is 210 $\times$ 150 μm^2. The transmission over 20-m CATV line using the prototype chip is successfully demonstrated.**

***Index Terms*—Binary phase shift keying, CATV, Costas-loop, demodulator, half-rate bang-bang phase detector, home networks, mixed-mode.**

I. Introduction

THERE are many A/V appliances at home such as DVD players, HDTV and satellite receivers. Establishing communication among these appliances is an important market demand. However, installing new lines for linking home appliances is not desirable and, consequently, approaches using either wireless channels or already-built-in wirelines are preferred. For the second approach, using cable TV (CATV) lines that are already installed in many houses can be an attractive solution.

Fig. 1(a) schematically shows such an approach. A switching hub and RF combiners are inside the wall with a CATV splitter. The switching hub connects a set-top box to many display terminals in several locations. In order to establish communication channels based on CATV lines, high-frequency carriers above 1 GHz must be used so that CATV signals ($\leq$ 700 MHz) are not disturbed by data streams as can be seen in Fig. 1(b). Modem chips that satisfy this requirement are not easily available.

Although such modulation techniques as QPSK and QAM are preferred since they utilize bandwidth more efficiently, we tried BPSK first because it is simpler and more suitable for the initial trial. There are several types of BPSK demodulators. In the analog approach, the carrier signal can be recovered by using a phase-locked loop (PLL) after the received signal is squared [1]. However, the phase error between the received and the recovered signals remains. Using Costas-loop [2] is a classical analog approach but, as the frequency becomes higher, design costs for filters and device matching increase. In the digital approach, several different architectures are possible depending on ADC configurations [3], but the maximum data rate is limited by the speed of ADCs. The digital interpolation scheme [4], [5], which is the most popular digital approach, needs GSamples/s ADCs to oversample hundreds of Mb/s data, but realization of such ADCs is not easy. In this paper, we report a new CMOS mixed-mode BPSK demodulator for 1.4 GHz carrier frequency that can handle 622 Mb/s for the above-mentioned application.

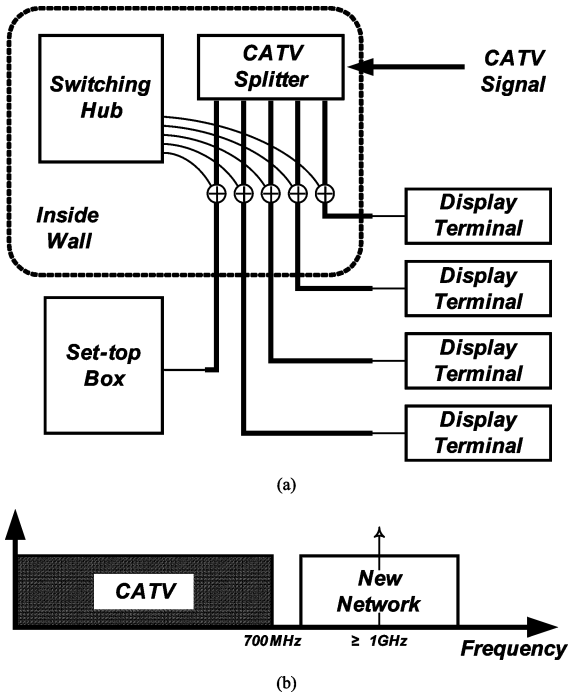

Fig. 1. CATV line network. (a) Block diagram. (b) Channel assignment.

This paper is organized as follows. Section II analyzes established BPSK demodulation schemes. Section III introduces the new mixed-mode demodulation scheme. Section IV describes the implementation of the prototype chip. Section V gives measurement results of the fabricated chip.

II. Established Demodulation Scheme

Fig. 2 is the block diagram of Costas-loop, the classic analog BPSK demodulator. Two sine waves with 90° phase difference are multiplied to the modulated signal. Assuming θ_e is the phase

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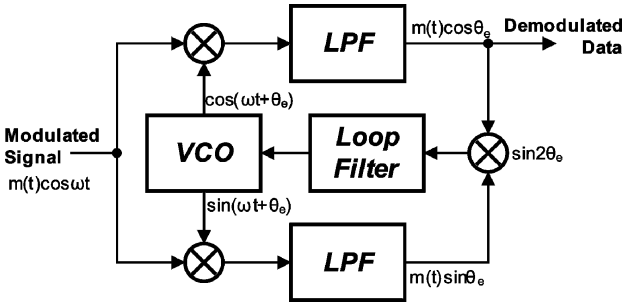

Fig. 2. Block diagram of Costas-loop.

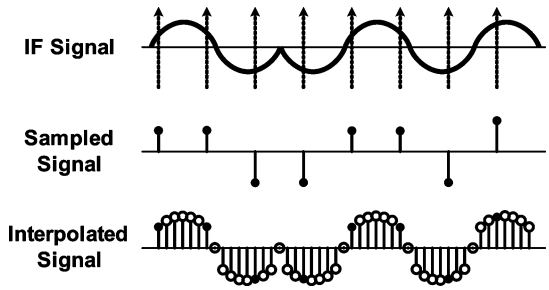

Fig. 3. Low-IF indirect conversion using digital interpolation.

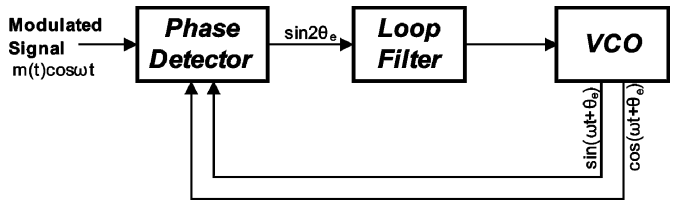

Fig. 4. Modified block diagram of Costas-loop.

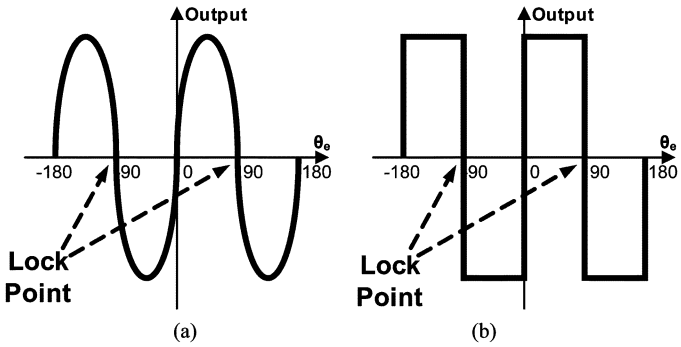

Fig. 5. Phase detection characteristic. (a) Costas-loop. (b) Half-rate bang-bang phase detector.

difference between the modulated signal and the voltage-controlled oscillator (VCO), two output signals are given as

$$m(t)\cos(\omega t)\cos(\omega t+\theta_e)=\frac{m(t)\{\cos\theta_e+\cos(2\omega t+\theta_e)\}}{2}$$
$$m(t)\cos(\omega t)\sin(\omega t+\theta_e)=\frac{m(t)\{\sin\theta_e+\sin(2\omega t+\theta_e)\}}{2}. \quad (1)$$

Low-pass filters (LPFs) remove high frequency terms having 2ω, so that only the terms having θ_e remain. The product of two LPF outputs results in terms having square of $m(t)$, which is always 1 since $m(t)$ is either 1 or -1. Consequently the output becomes $\sin 2\theta_e$. The phase difference, θ_e, can be eliminated by a feedback-loop and $m(t)$ is recovered.

For realization of Costas-loop for high frequency carrier applications, it is difficult to implement LPFs. By using simple *RC* filters, flatness of pass-band response and sharpness of cutoff band are poor. A large chip area is also needed due to capacitors. Although better flatness and sharpness can be achieved with other filter types, they usually require more chip areas. Another problem arises from the mismatch of two signal paths in the high frequency. This results in additional design costs.

In digital approach for BPSK demodulation, there are several variations depending on the ADC configuration, but ADC is usually located after the mixer. Fig. 3 shows an example of demodulation flow using the digital interpolation technique. After the mixer converts the RF signals to the IF domain, ADC samples them with a sampling clock. Then, signals between sampled data are produced by interpolation. The timing controller synchronizes interpolated signals in the digital domain and makes a decision. In this scheme, the minimum ADC sampling rate is twice of the data rate to satisfy the Nyquist condition. To demodulate higher order PSK signals, the ADC resolution has to be higher.

Several CMOS ADCs operating at GSamples/s have been reported in [6]–[8]. But they usually require large power consumption and chip area. Consequently, the ADC performance limits the maximum data rate in the digital approach.

III. Mixed-Mode Approach

The phase-tracking characteristic of Costas-loop can be represented by a block diagram shown in Fig. 4. Here, one phase detector block represents functions performed by three mixers and two LPFs in Fig. 2. In this block diagram, the phase detector (PD) takes modulated signals and a quadrature clock as input and produces $\sin 2\theta_e$ as output.

Then the phase detecting characteristics of Costas-loop can be represented by Fig. 5(a). Because BPSK signal changes its phase by 180°, this curve has two lock points separated by 180°. Similar PD characteristics can be realized with a half-rate bang-bang PD, commonly used for CDR applications, as shown in Fig. 5(b).

Fig. 6 shows how a half-rate bang-bang PD using a quadrature clock tracks BPSK signals. After passing through a hard limiter, input BPSK signals (MOD) become NRZ signals (NRZ). The dotted line, CLKI, is the tracking clock, and the solid line, CLKQ, is the sampling clock. The CLKI tracks transition edges of NRZ. If CLKI leads the modulated signal, the phase adjustment circuit makes its clock slower, and if it lags, faster. Consequently, a half-rate bang-bang PD can replace mixers and LPFs in Costas-loop.

After synchronization, edges of the sampling clock, CLKQ, are aligned to centers of NRZ as shown in Fig. 7. In the figure, arrows indicate sampling points of PD. Black arrows are rising edges and white arrows are falling edges of CLKQ. Then

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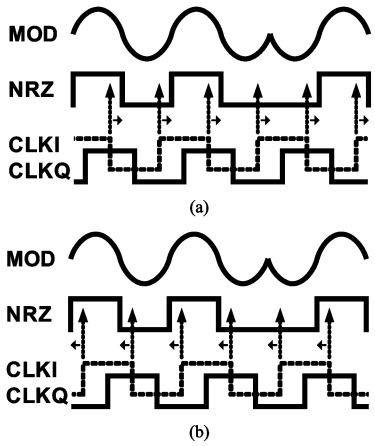

Fig. 6. BPSK signal tracking by half-rate bang-bang PD. (a) When clock leads. (b) Clock lags.

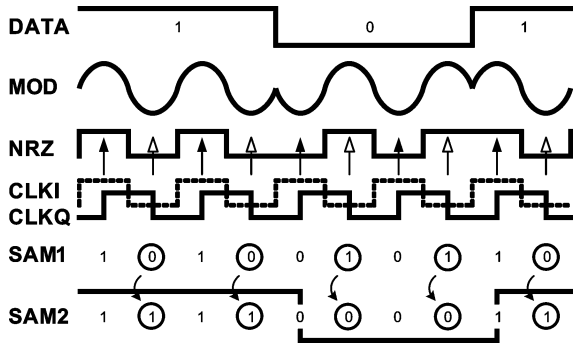

Fig. 7. Proposed demodulation scheme.

the bang-bang PD produces output sequence, SAM1, which consists of 10 and 01. The BPSK demodulation is done when decisions are made for high for 10 sequence, and low for 01 sequence. This can be easily realized by inverting samples at falling edges of CLKQ, which makes 10 sequence 11, and 01 sequence 00 (SAM2 in the figure). This BPSK demodulation scheme can use any type of CDR architectures using a half-rate PD.

When the carrier frequency is exactly the integer-multiple of the data rate, BPSK signal can be generated identically to NRZ signal. But it is impossible for a flexible data rate with a fixed carrier frequency. In the proposed scheme, data transition is recognized when the receiver clock synchronized to the carrier signals goes through the transition, not when the data go through the transition. When the carrier frequency is not exactly the integer-multiple of the data rate as shown in Fig. 8, data transitions occurring between receiver clock transitions are recognized at the next clock transition, causing the quantized timing error, maximum of which is given as the half of carrier period. This affects jitter performance directly. Sampling clock is aligned to carrier phase, and therefore, it slips as shown in figure. After an half beating period, the difference of data rate and carrier frequency, the transition will return because adjacent sampling clock is aligned again. Consequently, there occur slipping traces on eye diagram as shown. With a higher carrier frequency, this quantized timing error is reduced. Since the amount of jitter given in unit interval (UI) is proportional to the product of this quantization error and the data rate, the key parameter for jitter performance in our demodulator is (Carrier frequency)/(Data rate).

It is easy to extend the proposed scheme into demodulations of higher order PSKs. M-ary PSK modulation uses M phases to express M symbols. For example, BPSK uses 0° and 180° phases for 0 and 1 symbols, and QPSK uses 0°, 90°, 180°, and 270° for 00, 01, 11, and 10. Demodulator for M-ary PSK modulated signal should have PD which has M lock points to maintain locked state for input phases. Consequently, a 1/M-rate CDR circuit can synchronize its clocks to M-ary PSK signal. With the proposed scheme, CDR circuit locks its frequency to the carrier frequency not the data rate. Thus, 1/M rate CDR for data rate DR is capable of demodulating M-ary PSK signals with carrier frequency, DR/M. For example, 10-Gb/s half-rate CDR fabricated with 0.18 μm CMOS process reported in [12] can be applied to demodulate BPSK modulated signal with 5-GHz carrier. As the prototype BPSK demodulator chip shows maximum symbol rate of about half the carrier frequency, the maximum data rate will be above 2 Gb/s.

IV. Implementation

A. Phase Control Scheme

Among the several kinds of phase control schemes for CDR applications, the scheme of controlling VCO with PD output is the most basic one. For this, the loop bandwidth influences phase noises from input and power supply noises. The phase noise characteristics are very important for demodulator applications because phase noises can cause phase unlocking problems, resulting in data errors. For the optimal performance, the prototype chip employs the semi-digital dual-loop delay-locked loop (DLL) scheme [9], which separates loop bandwidth of PLL from input noises by using separate loops for clock generation and phase tracking. This phase control scheme is always stable because it is essentially DLL, type-I system. The frequency locking range of this scheme is limited by the operating frequency range of PLL. Fig. 9 shows a block diagram for the prototype chip. Since a half-rate bang-bang PD needs a quadrature clock, Phase-Interpolator2 and 4:2 MUX2 are added [10]. These additional blocks are also controlled by the same phase controller and use 90° delayed input clocks.

The phase controller shifts the phase by the minimum step to align tracking clock to input signal. The prototype chip has 6-bit resolution since it uses 4-bit phase interpolators and 4:2 MUXs with 2-bit select signal. The phase controller was implemented by auto placement and routing of standard CMOS logic cells. Because of the low speed of CMOS logic cells, the clock speed of the controller was pulled down to the quarter of the carrier frequency.

The phase interpolator, as shown in Fig. 10, was implemented by summing CLK1 and CLK2. It uses 15-bit thermometer code, equivalent to 4-bit binary code, as control signals. Each control signal turns on or off the current bias transistor to control weights of CLK1 and CLK2, resulting in phase shifts. Fig. 11 shows simulated output phases versus input codes. The dotted line in the figure shows the ideal output phase. The maximum

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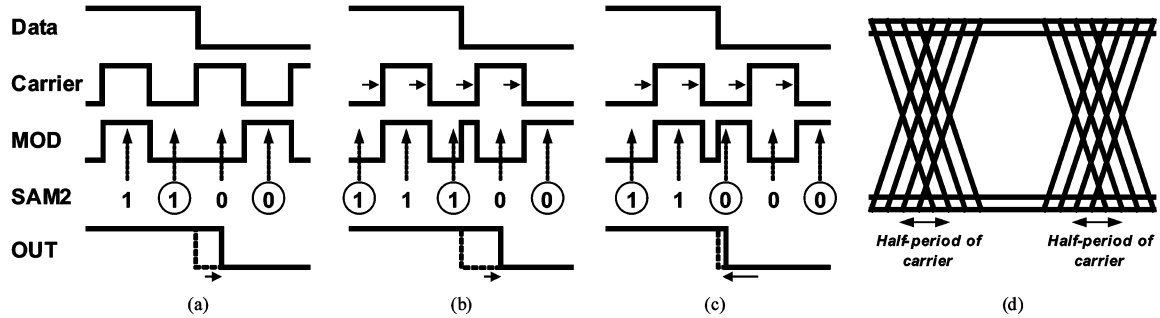

Fig. 8. Quantized timing error. (a) Aligned. (b) After 1/6 of beating period. (c) After 2/6 of beating period. (d) Eye-diagram.

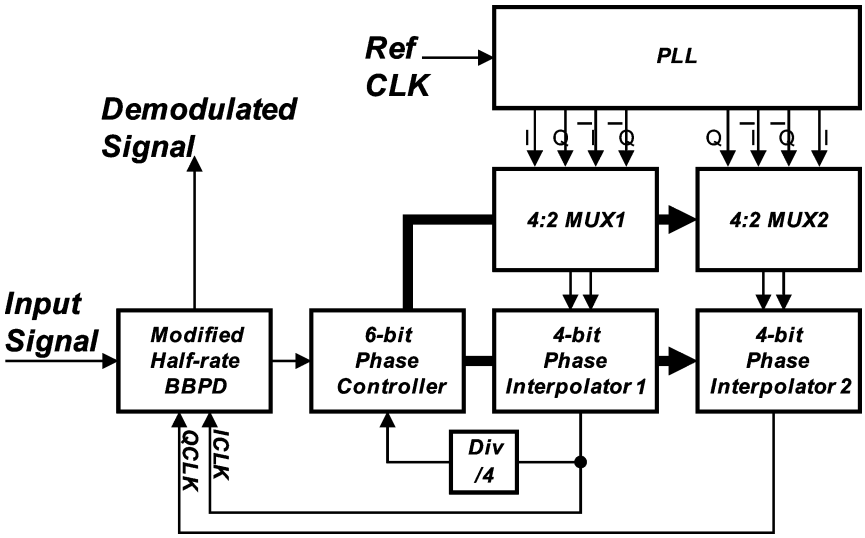

Fig. 9. Block diagram of the prototype chip.

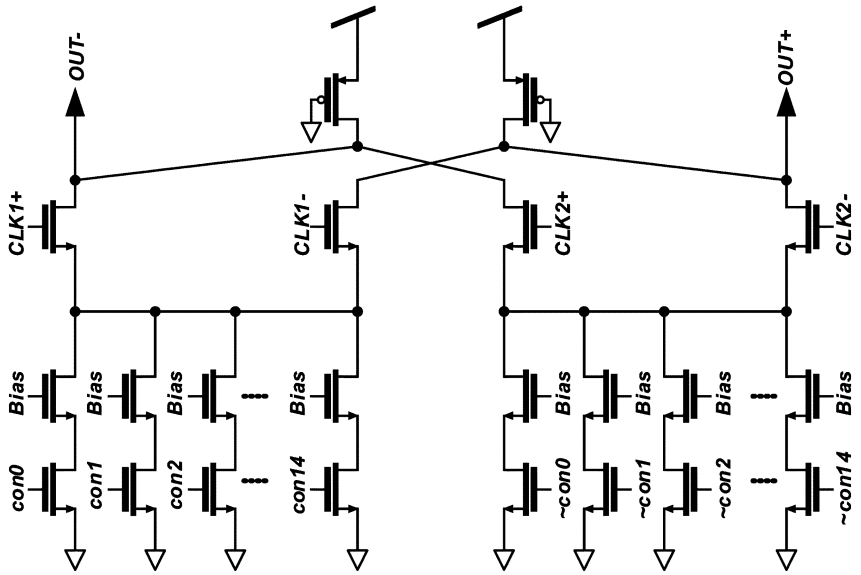

Fig. 10. 4-bit phase interpolator.

output phase error is 12.4° at code 12 and the maximum step is 12.1° at code 8.

B. Half-Rate Bang-Bang Phase Detector

Fig. 12 shows the structure of half-rate bang-bang PD used in the prototype chip. This is essentially same as PDs employed in [11], [12] except MUX4-5. Fig. 13 schematically shows the operation of the designed half-rate bang-bang PD. Two latches and one MUX constitute one double-edge-triggered flip-flop (DETFF), which samples input signals at rising and falling edges of clock. SI and SQ are data sampled by DETFF1 using CLKI and DETFF2 using CLKQ. DETFF3 samples SI using

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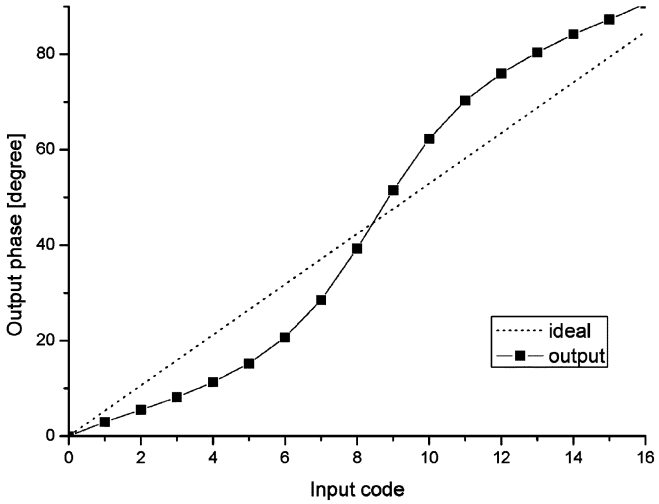

Fig. 11. Output phase versus input code.

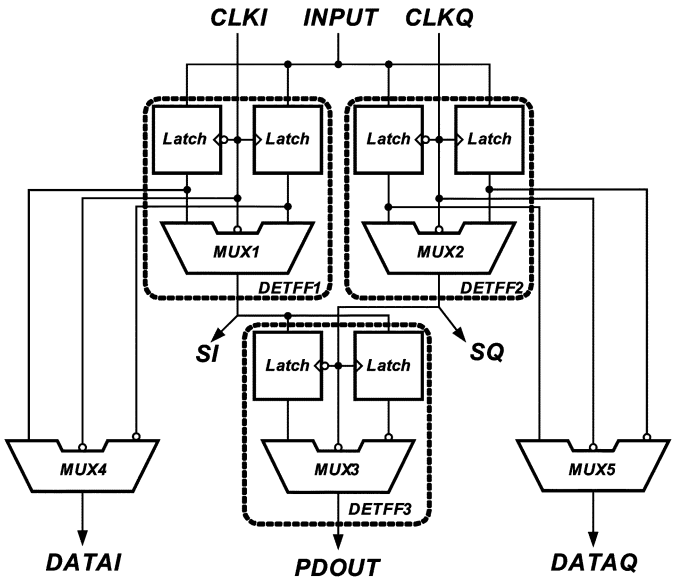

Fig. 12. Modified half-rate bang-bang PD.

SQ as a clock. DETFF3 inverts output at falling edges, shown by white arrows in the figure, since one input of MUX3 is inverted. Finally, PDOUT is 0 when clock leads and 1 when clock lags. After synchronization, MUX5 inverts samples at falling edges for demodulation. MUX4 is added as a dummy block to match delay.

Half-rate bang-bang PD is the block requiring the highest operation speed in the proposed scheme because this block must track modulated signals and produce sampled values in each carrier period. Consequently, this block is designed with current mode logic (CML) cells.

In order to verify that this PD is capable of detecting phase errors of BPSK modulated signal, simulation is performed for 622-Mb/s BPSK signals with 1.4-GHz carrier frequency. The characteristic is calculated by averaging differential output currents for 90 ns. Fig. 14 shows the simulated PD characteristics having two lock points within 360°.

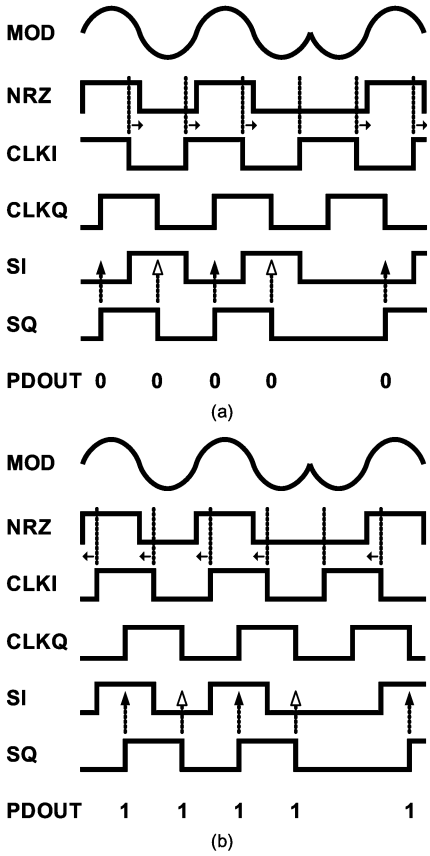

Fig. 13. Operation of half-rate bang-bang PD. (a) Clock lead. (b) Clock lag.

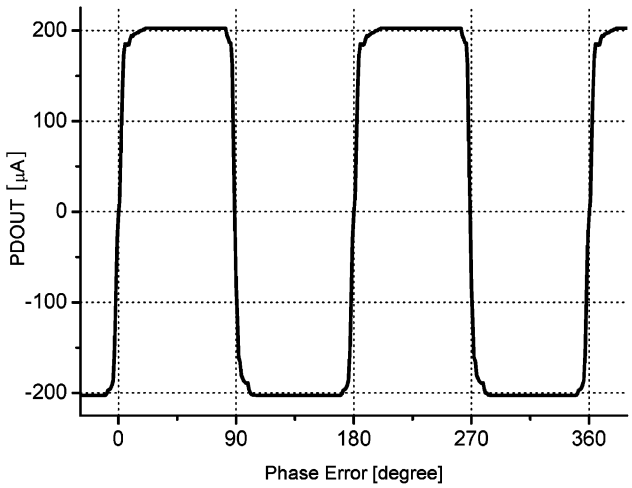

Fig. 14. Simulation of half-rate bang-bang PD @ data rate: 622 Mb/s, carrier frequency: 1.4 GHz.

C. Quadrature Clock Generator

The PLL should provide quadrature clocks for the demodulator to synthesize demodulator clocks. The prototype chip employs an LC oscillator for low phase noise performance. For quadrature clock generation, the phase interpolation technique [13] is used. Fig. 15 shows IQ generator which consists of 6 phase interpolators, PI1-6, and delay line. Input clock signal, CLK1, and the signal after delay line, CLK2, are given as

$$CLK1 = \cos\omega t$$
$$CLK2 = \cos(\omega t + \theta). \quad (2)$$

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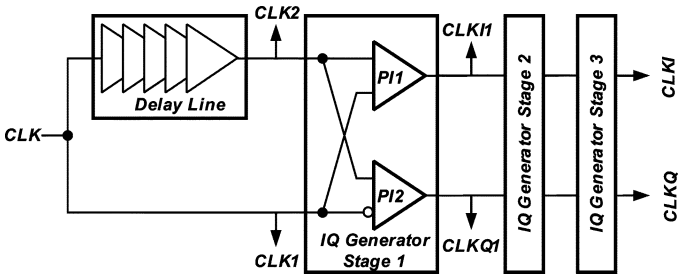

Fig. 15. Block diagram of IQ generator.

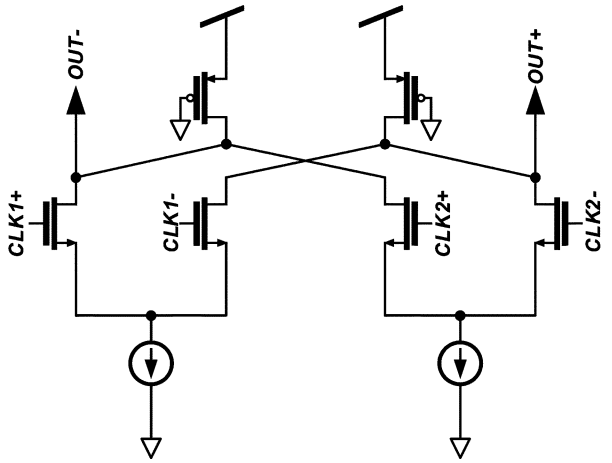

Fig. 16. Half-phase interpolator.

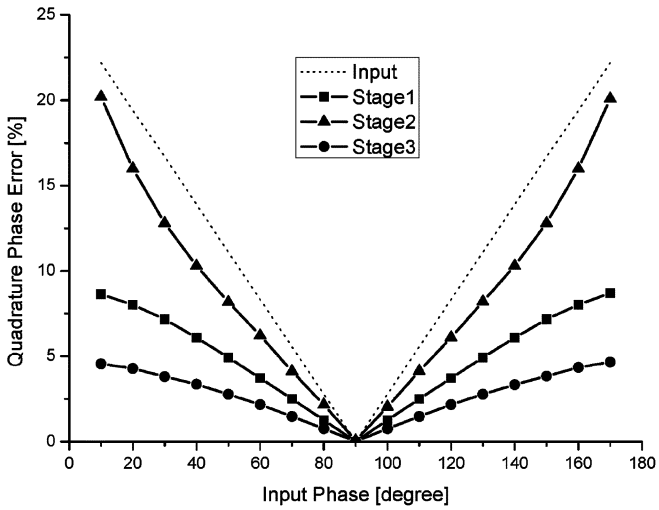

Fig. 17. Quadrature phase error versus input phase.

PI1 produces the mean phase of CLK1 and CLK2, and PI2 the mean phase of CLK1 and inverse of CLK2. Each of PI outputs, CLKI1 and CLKQ1, is given as

$$CLKI1 = \cos\left(\frac{\omega t + \theta}{2}\right)$$
$$CLKQ1 = \cos\left(\frac{\omega t + \theta}{2} + \frac{\pi}{2}\right). \quad (3)$$

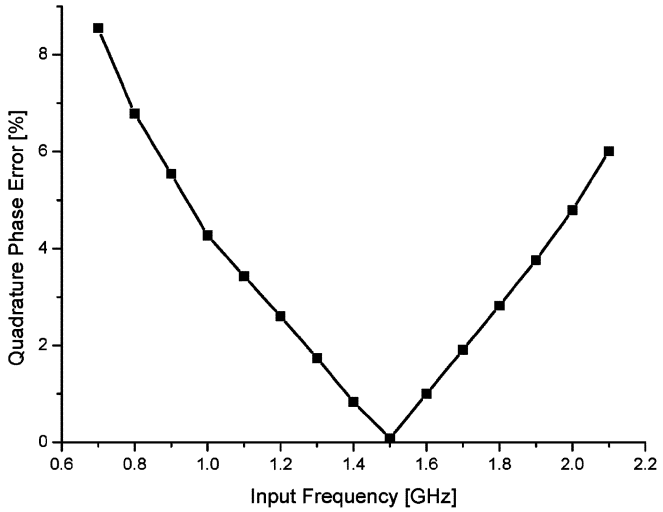

Fig. 18. Quadrature phase error versus input frequency.

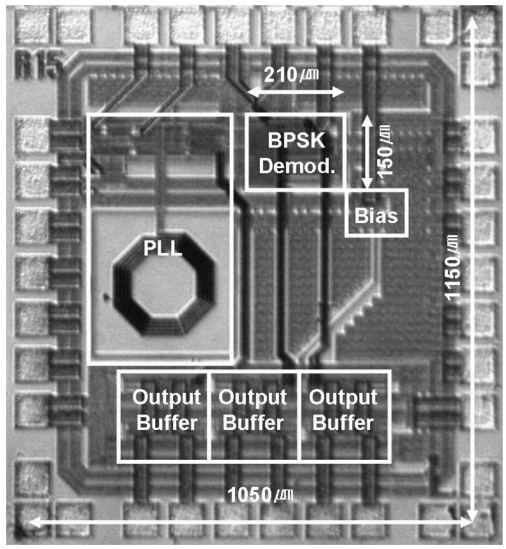

Fig. 19. Die photo of the fabricated chip.

They have $\pi/2$ of phase difference for any value of θ. In the circuit level, phase interpolators are implemented using a current sum as shown in Fig. 16 and, consequently, the range of input phase difference is limited. To resolve this limitation, two stages are attached. Fig. 17 shows the quadrature phase error, which is the phase error of output quadrature clocks normalized by 90°. In this figure, input phase represents the phase difference between CLK1 and CLK2. The first stage generates IQ phases with less than 10% errors for any length of delay line. The phase error after second stage is recovered as input, but slightly reduced because of non-ideality of the phase interpolator. Finally, the third stage generates IQ phases with less than 5% errors for any length of delay line.

Although this circuit generates IQ phases for any length of delay line, the result is best at 90° of input phase difference. Consequently, the length of delay line is chosen as close to 90° as possible with 5 CML buffers. Fig. 18 shows the quadrature phase error from the designed circuit at different operating frequencies. At 1.4 GHz, the error is less than 1%.

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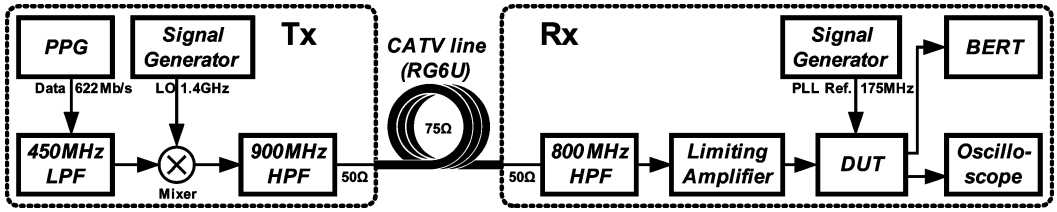

Fig. 20. Measurement setup.

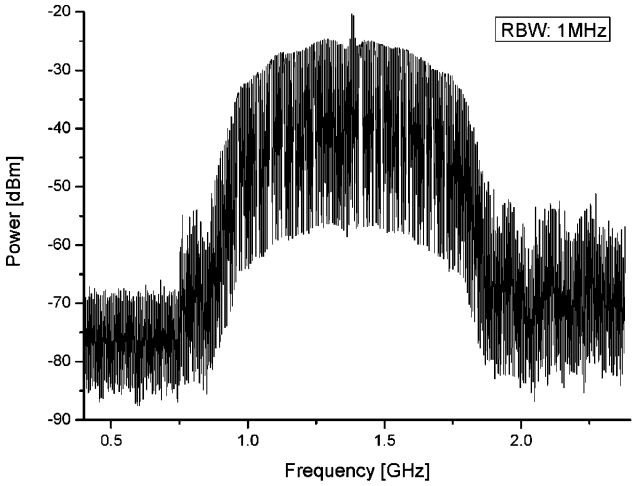

Fig. 21. Spectrum of Tx output.

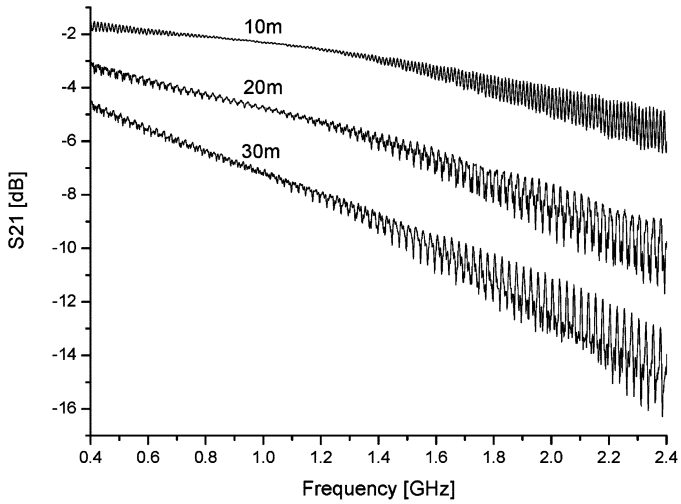

Fig. 22. S21-parameter of RG6U line for 10 m, 20 m, and 30 m.

TABLE I
PERFORMANCE OF FABRICATED CHIP

Process	TSMC 0.18μm RF
Maximum data rate (PRBS 2^7-1)	622 Mb/s
Carrier frequency	1.4GHz
Supply voltage	1.8 V
Area	Core: 210 □ 150 μm^2 Total: 1050 □ 1150 μm^2
Power consumption	Demodulator: 27.5mW PLL+IQ generator: 13.3mW 3 output buffers: 228.8mW Total: 269.6mW

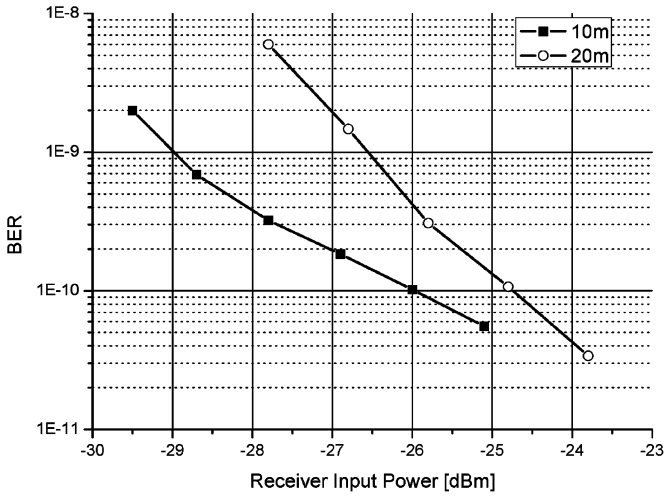

Fig. 23. BER versus Rx input power for 10-m and 20-m CATV line link.

V. MEASUREMENT

The prototype chip has been fabricated with 0.18 μm RF CMOS technology. Fig. 19 shows the die photo. Fig. 20 is the measurement setup used for verifying chip operation. The band-limited BPSK signals are produced by mixing 2^7-1 PRBS data with 1.4-GHz signals from a signal generator. A 900-MHz HPF is attached to reject any Tx signals in the CATV signal band. No actual CATV signals are used. Fig. 21 shows the spectrum of the transmitted signals. In the receiver, an 800-MHz HPF is used, which can filter out any CATV signals. A limiting amplifier is added, because a hard limiter helps mixed-mode operation. This amplifier has -40 dBm of minimum sensitivity and 50-dB gain.

At first, the performance of the demodulator is measured for the back-to-back link without any CATV line. The maximum error-free data rate is 622 Mb/s, which is about half of the carrier frequency (1.4 GHz). Table I summarizes the performance of the fabricated chip.

The link performance is also measured with RG6U line, which is commonly used for CATV applications. Fig. 22 shows measured S21-parameters for 10 m and 20 m cable. As can be seen, higher frequency signals experience more attenuation, which results in signal distortion especially for wide bandwidth signals. The fluctuation in S21 measurement is believed due to mismatch between 75-ohm CATV line and other 50-ohm components. From the spectrum measurement, it is estimated that transmitted BPSK signals experience about 0.2-dB/meter attenuation.

A variable attenuator is added between the transmitter HPF and CATV line for bit-error rate (BER) measurement. Fig. 23

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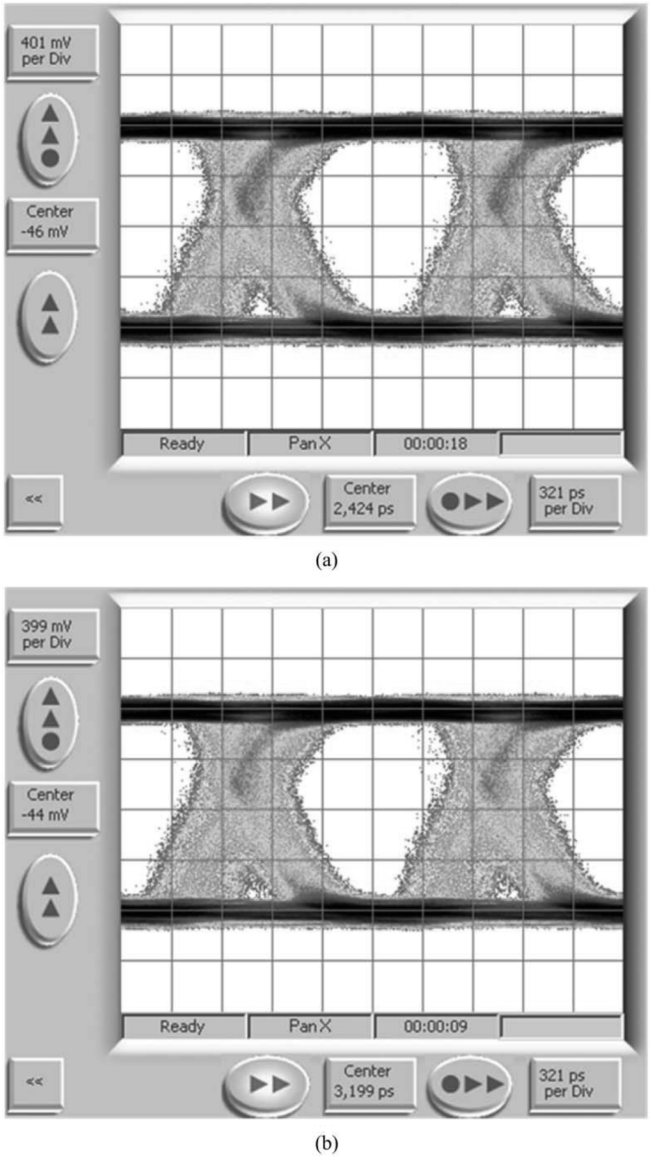

Fig. 24. Eye diagram @ 622 Mb/s. (a) Back-to-back link. (b) 20-m CATV line link.

shows measured BERs for 10 m and 20 m of RG6U line versus Rx input power. The longer cable has higher BER at the same receiver input power because the longer cable experiences more signal distortion. For less than 10^{-12} BER over 20 m, about -20 dBm of receiver input power is required.

With -0.6 dBm Tx power and -6.7 dBm Rx input power after 20-m line, no errors are detected for an hour, which corresponds to BER less than 4.35×10^{-13}. Fig. 24 shows eye diagrams in this condition for (a) back-to-back and (b) 20-m RG6U line. The figure shows a considerable amount of jitters even for the back-to-back case. This is mostly due to the quantized timing error from the frequency offset problem mentioned earlier.

VI. Conclusion

We demonstrated a new mixed-mode demodulating scheme which can handle a very high data rate, up to half of the carrier frequency. Experimental results show that the demodulator realized with 0.18 μm CMOS technology can demodulate BPSK signals up to 622 Mb/s with 1.4 GHz carrier frequency. It is expected that this demodulator finds useful applications for new home networking architecture based on CATV lines.

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