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6.25-Gb/s Optical Receiver Using A CMOS-Compatible Si Avalanche Photodetector

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An optical receiver using a CMOS-compatible avalanche photodetector (CMOS-APD) is demonstrated. The CMOS-APD is fabricated with 0.18 μm standard CMOS technology and the optical receiver is implemented by using the CMOS-APD and a transimpedance amplifier on a board. The optical receiver can detect 6.25-Gb/s data with the help of the series inductive peaking effect.

Keywords : Avalanche photodetector, CMOS, Optical interconnect, Optical receiver

OCIS codes : (040.5160) Photodetectors; (040.6040) Silicon; (060.0060) Fiber optics and optical communications; (060.4510) Optical communications

I. INTRODUCTION

For short-distance optical communications such as optical access networks and optical interconnects, CMOS compatible photodetectors (CMOS-PDs) have been widely investigated to enable cost-effective implementation of large-capacity data transmission systems [1-8]. CMOS technology provides not only low-cost and high-volume fabrication but also a single chip solution for optical receivers with well developed CMOS circuits. In addition, readily available low-cost vertical-cavity surface-emitting lasers (VCSELs) can be used with CMOS-PDs for 850-nm applications. CMOS technology, however, has inherent drawbacks of the low bandwidth-efficiency product due to low optical absorption coefficient of Si and high doping profiles not suitable for PD applications [1].

In order to improve the bandwidth-efficiency product of CMOS optical receivers, several approaches have been tried. By using a low-doped epitaxial layer [2] or silicon-on-insulator processes [3], high quantum efficiency or large bandwidth due to elimination of slow diffusion currents was achieved. However, these approaches require process modification or special substrates, resulting in additional fabrication costs. With a standard CMOS process, equalizer circuits for compensating low-speed PD were developed [4]. This scheme, though, requires knowledge in accurate photodetector responses and complicates the receiver circuit design. Spatially modulated PDs, in which slow diffusion currents are eliminated with differential signaling, were implemented. However, they still have problems of low responsivity and limited speed caused by a large area [5]. Recently, p+-p-n avalanche structure has been reported that provides high-speed and high-responsivity [6]. Based on this photodetector, a bandwidth enhancement technique was also devised by eliminating slow diffusion photocarriers [7]. Although this structure provides high-responsivity owing to a large depletion region formed by an N-well/P-substrate junction, relatively high dark currents can be generated. Furthermore, the advantage of high-responsivity can be sacrificed by applying body voltages applied for elimination of slow diffusion components. More severely, positive body voltages make it difficult to implement integrated optical receivers because the substrate potential of all the electronic circuits should be set to ground. We previously presented Si avalanche photodetectors which have large bandwidth and low dark currents by using P+/N-well junction with shallow trench isolation (STI) [8].

In this work, we demonstrate a high-speed optical receiver based on the CMOS-APD with a commercially available transimpedance amplifier (TIA). By using the series inductive peaking effect with bond wire [9], the bandwidth of the optical receiver is enhanced. Using the

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fabricated optical receiver, data transmission of 6.25 Gb/s is successfully performed with BER less than 10^{-12} at input optical power (P_{opt}) of -2 dBm.

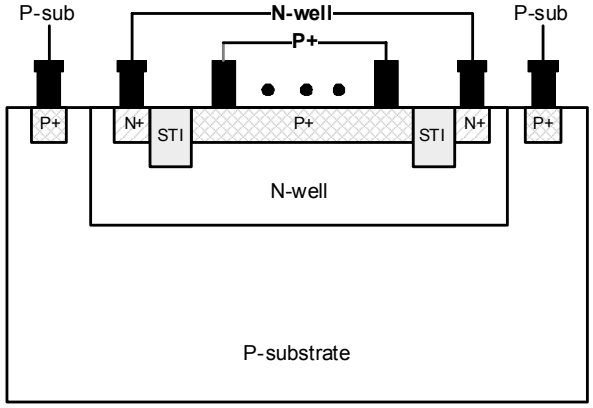
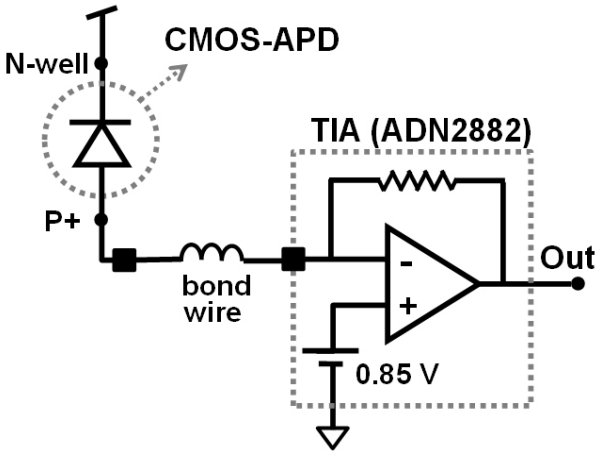
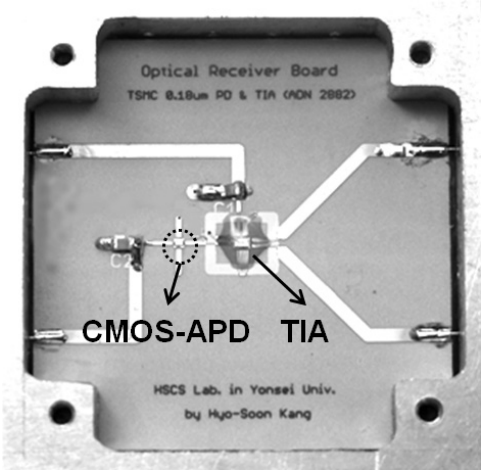


FIG. 1. Cross-sectional structure of the CMOS-APD. (STI: shallow trench isolation)



(a)



(b)

FIG. 2. (a) Schematic and (b) photograph of the optical receiver based on the CMOS-APD.

II. OPTICAL RECEIVER AND EXPERIMENTAL SETUP

Fig. 1 shows the cross-sectional structure of the fabricated CMOS-APD. The device was fabricated with 0.18 -μm standard CMOS technology without any process modification or special substrate. To eliminate slow diffusion currents in the substrate region, we only utilize PN junctions realized by P+ source/drain and N-well regions. The output signals are extracted from P+ contacts and multi-finger electrodes having 0.5 μm spacing. In the device, P+ region is bounded by shallow trench isolation (STI), whose material is SiO_2, to mitigate the edge breakdown effect in the avalanche regime. Because the dielectric strength of SiO_2 is about 30 times higher than the breakdown field of silicon, premature breakdown in the lateral edge of P+/N-well junction can be prevented. The active area of the P+ region is about 30×30 μm^2 and the salicide process is blocked for the optical window. Details of the CMOS-APD characteristics are given in [8].

Fig. 2 shows a schematic and a photograph of the fabricated optical receiver based on the CMOS-APD. The optical receiver is implemented on a board by connecting the P+ port of CMOS-APD to the input of the TIA chip (Analog Devices, ADN2882) with a chip-on-board (COB) technique which directly attaches semiconductor chips to a board with wire-bonding. In the optical receiver, the bond-wire inductances between the CMOS-APD and the TIA can enhance bandwidth owing to series inductive peaking effect [9]. The TIA gain and bandwidth used in the optical receiver is about 60 dB $\cdot\ \Omega$ and 3.5 GHz, respectively.

To characterize the fabricated CMOS-APD and optical receiver, modulated optical signals were generated using an 850-nm laser diode and a 20-GHz electro-optic modulator. The generated optical signals were injected to the CMOS-APD through a lensed-fiber. For the measurement of photodetection frequency response, a vector network analyzer (Agilent 8719ES) was used with prior calibration of cables and RF adaptors. For data transmission measurement, output signals of the optical receiver were amplified by a limiting amplifier to satisfy the dynamic range of Bit Error Rate (BER) measurement (BERTScope 12500A). The input optical power to the CMOS-APD was controlled by an optical attenuator at the input of the lensed-fiber.

III. EXPERIMENTAL RESULTS

Fig. 3 shows photodetection frequency responses of the CMOS-APD and the optical receiver. It is observed that the overall bandwidth of the optical receiver is enhanced by the series inductive peaking realized by

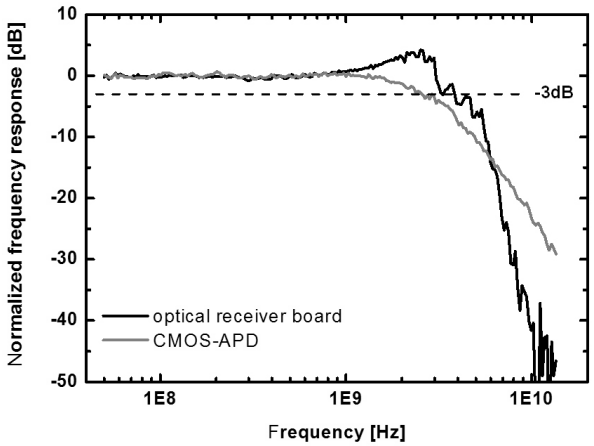


FIG. 3. Photodetection frequency response of the CMOS-APD and the optical receiver.

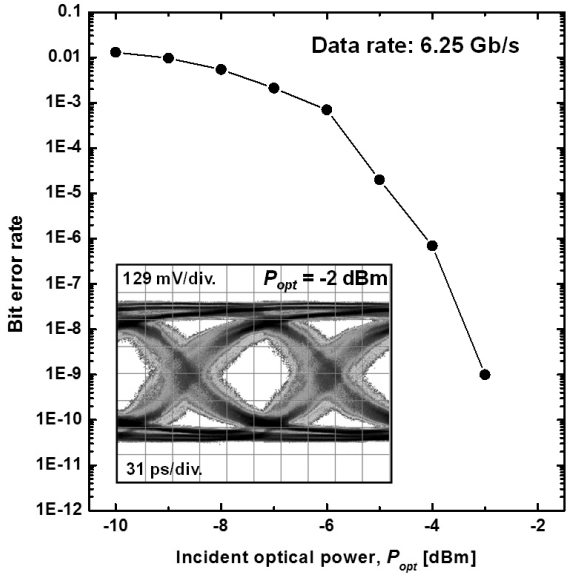


FIG. 4. Bit error rate as a function of incident optical power into the optical receiver at data rate of 6.25 Gb/s. At P_{opt} of -2 dBm, no error was detected for about 10 minutes. Inset: eye diagram at the incident optical power of -2 dBm.

bond-wire inductance. The fabricated optical receiver has bandwidth of about 4.4 GHz compared with 2.6 GHz for the CMOS-APD. Using the optical receiver, 6.25-Gb/s (2^7-1 PRBS) signal transmission was performed. Fig. 4 shows dependence of BER on incident optical power measured at the input of the lensed-fiber. Above the optical power of -2 dBm, error-free transmission (BER < 10^{-12}) of 6.25-Gb/s data was possible. Table 1 shows the comparison of published results with our work. The fabricated optical receiver can successfully transmitted the highest data rate of 6.25 Gb/s. However, to reduce sensitivity of optical receiver based on the CMOS-APD, further improvement of responsivity as well as careful design of an integrated optical receiver for optimized noise performance is required.

IV. CONCLUSION

We present an optical receiver using a CMOS-APD and a TIA on a board. The bandwidth of the optical receiver based on a CMOS-APD can be enhanced with the series inductive peaking effect of the bond wire. Using the optical receiver, 6.25-Gb/s data transmission is successfully performed.

ACKNOWLEDGMENT

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TABLE 1. Performance comparison of optical receivers based on CMOS-compatible photodetectors.

Year	2005	2005	2007	2008	2008
Reference	[5]	[4]	[6]	[7]	This work
Process	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
PD bandwidth	1.1 GHz	< 10MHz	1.6 GHz	2.8 GHz	2.6 GHz
Responsivity at bias voltage	0.02 A/W at 2V	N. A.	0.74 A/W at 14.3 V	N.A.	0.34 A/W at 10.4 V
Data rate	2 Gb/s	3 Gb/s	3.5 Gb/s	5 Gb/s	6.25 Gb/s
Sensitivity at BER	-8 dBm at 10^{-9}	-19 dBm at 10^{-11}	N. A.	N.A.	-2 dBm at 10^{-12}

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