High-Speed CMOS Integrated Optical Receiver With an Avalanche Photodetector

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***Abstract*—We present a high-speed monolithically integrated optical receiver fabricated with 0.13-μm standard complementary metal–oxide–semiconductor (CMOS) technology. The optical receiver consists of a CMOS-compatible avalanche photodetector (CMOS-APD) and a transimpedance amplifier (TIA). The CMOS-APD provides high responsivity as well as large bandwidth. Its bandwidth is further enhanced by the TIA having negative capacitance, which compensates undesired parasitic capacitance. With the CMOS integrated optical receiver, 4.25-Gb/s optical data are successfully transmitted with a bit-error rate less than 10^{-12} at the incident optical power of -5.5 dBm.**

***Index Terms*—Avalanche photodetectors (APDs), complementary metal–oxide–semiconductor (CMOS) integrated optical receiver, transimpedance amplifier (TIA).**

I. Introduction

DUE to such advantages of complementary metal–oxide–semiconductor (CMOS) technology as low fabrication cost and high volume manufacturability, all the electronic circuits for analog, digital, and radio-frequency (RF) applications have been widely developed on the CMOS platform. Since silicon photodetectors can be fabricated with CMOS technology for 850-nm optical communication applications, fully integrated CMOS optical receivers have been a target of active research efforts especially for low-cost optical communication systems [1]–[4].

Table I shows performance comparison of CMOS integrated optical receivers reported in recent publications. Various types of CMOS photodetectors based on spatially modulated light (SML) [1], lateral PIN [2], and N-well/P-substrate junction [3] have been used for these CMOS integrated optical receivers. Furthermore, photodetectors were monolithically integrated with CMOS circuits including amplifiers and equalizers, which compensate the photodetector frequency responses, greatly enhancing the overall receiver frequency responses [3], [4]. However, the reported performances are still inferior compared with those of receivers based on III–V photodetectors. This is because silicon photodetectors fabricated with standard CMOS technology suffer from low gain-bandwidth product due to narrow depletion regions and slow diffusion currents.

TABLE I
COMPARISON WITH THE PERFORMANCE OF INTEGRATED OPTICAL RECEIVER FABRICATED WITH STANDARD CMOS TECHNOLOGY

	[1]	[2]	[3]	[4]	This work
Process	0.18 μm	0.18 μm	0.18 μm	0.13 μm	0.13 μm
Data rate	2 Gb/s	2.5 Gb/s	3 Gb/s	4.5 Gb/s 4 Gb/s	4.25 Gb/s 3.125 Gb/s
Sensitivity	-8 dBm	-4.5 dBm	-19 dBm	-3.4 dBm -4 dBm	-5.5 dBm -8 dBm
BER (PRBS)	10^{-9} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-11} (2^{31}-1)	10^{-12} (2^{7}-1)	10^{-12} (2^{31}-1)
Receiver structure	SML +TIA+LA	Lateral PIN +TIA+LA	N-well/P-sub +TIA+EQ	SML+TIA +EQ+LA	APD+TIA

In order to solve these limitations, avalanche photodetectors (APDs) have been investigated that can be fabricated with standard CMOS technology [5]–[7] or with SiGe technology [8], [9]. Using the internal gain and RF-peaking effect in APDs, photodetector responsivity and frequency response can be greatly improved.

In this letter, we report an 850-nm integrated optical receiver having a CMOS-compatible avalanche photodetector (CMOS-APD) and a transimpedance amplifier (TIA). The receiver was fabricated with 0.13-μm standard CMOS foundry service. With the CMOS-APD, a high-responsivity and large-bandwidth photodetector is achieved. The optical receiver bandwidth is further enhanced by a negative capacitance in the TIA circuit. We successfully demonstrate data transmission up to 4.25 Gb/s using the fabricated CMOS integrated optical receiver.

II. CMOS Integrated Optical Receiver

Fig. 1(a) shows the architecture, and Fig. 1(b) the microphotograph of our CMOS-APD optical receiver. The chip size is 540×540 μm^2. The receiver has a CMOS-APD for optical-to-electrical signal conversion with internal gain, a TIA for current-to-voltage conversion with amplification, an offset cancellation network (OCN) for differential signaling, and an output buffer for driving 50-Ω load. The TIA and OCN consume about 21.6 mW with the supply voltage of 1.2 V.

The CMOS-APD is realized by vertical P^+/N-well junction surrounded by shallow trench isolation. Details of CMOS-APD structure and characteristics can be found in [5]. The shallow trench isolation surrounding P^+/N-well junction mitigates the premature edge breakdown in the avalanche regime. The active area for optical window is about 30×30 μm^2 and the salicide process is blocked between multifinger electrodes. Fig. 2 shows current–voltage (I–V) characteristics as a function of reverse bias voltage (V_R) with and without optical illumination ($P_{opt} = 0$ dBm). The CMOS-APD has low dark current less

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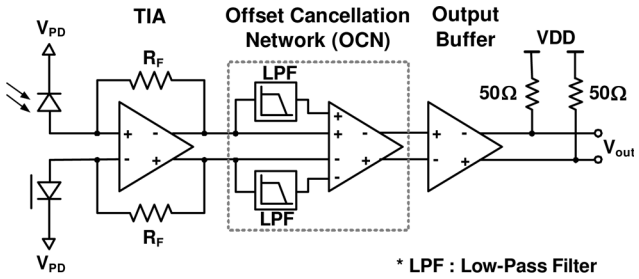
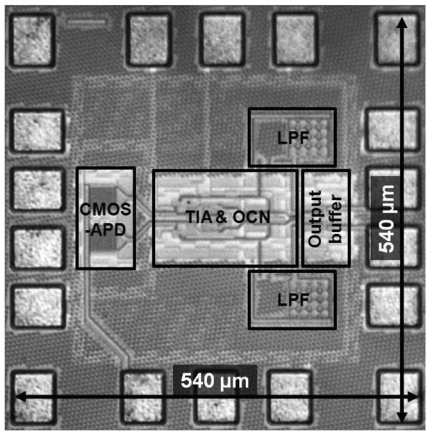


(a)



(b)

Fig. 1. (a) Architecture of the CMOS integrated optical receiver with integrated CMOS-APD. (b) Microphotograph of the fabricated CMOS integrated optical receiver.

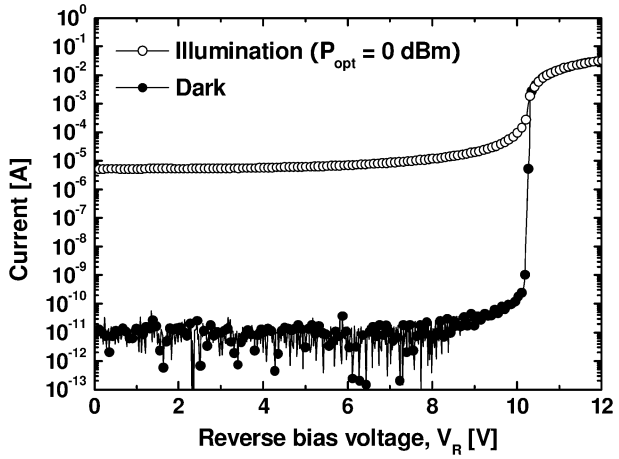


Fig. 2. I–V characteristics of the fabricated CMOS-APD as a function of the reverse bias voltage (V_R) under dark and illumination conditions. Incident optical power $(\mathrm{P_{opt}})$ is 0 dBm.

than a few nanoamperes before the avalanche breakdown occurs at about 10.3 V. The maximum responsivity and avalanche gain of CMOS-APD are about 0.4 A/W and 95, respectively.

Fig. 3 shows the schematic of the core amplifier in the TIA. To achieve high transimpedance gain and low input-referred noises, high feedback resistance is required. However, the high feedback resistance can reduce bandwidth of the optical receiver. For maintaining high feedback resistance ($R_F = 3\,\mathrm{k}\Omega$ in Fig. 1) without sacrificing 3-dB bandwidth of the TIA circuit, negative capacitance with a metal–oxide–metal (MIM) capacitor is

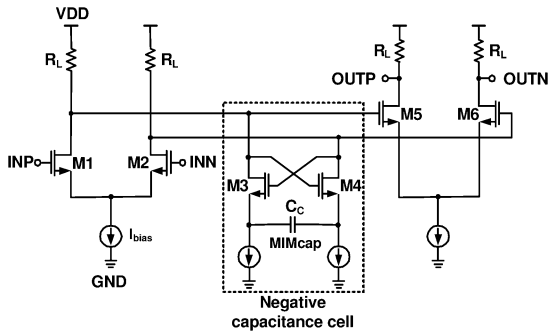


Fig. 3. Schematic of core amplifier in TIA including negative capacitance cell for enhancing 3-dB bandwidth ($C_c = 166$ fF).

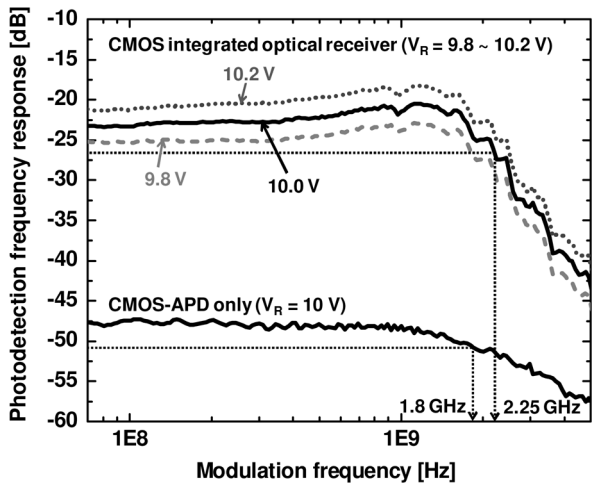


Fig. 4. Measured photodetection frequency responses of the CMOS integrated optical receiver ($V_R = 9.8$–10.2 V) and CMOS-APD only ($V_R = 10$ V). Incident optical power $(\mathrm{P_{opt}})$ is 0 dBm.

adopted as shown in Fig. 3. The capacitance (C_c) in the negative capacitance cell is set at 166 fF with consideration for its equivalent output impedance. The negative capacitance induces the RF-peaking effect, which enhances the optical receiver bandwidth. By using the root locus method, the TIA circuit was confirmed stable. Fig. 4 shows measured photodetection frequency responses of the CMOS-APD only as well as the CMOS integrated optical receiver when the reverse bias voltage of CMOS-APD increases from 9.8 to 10.2 V. Within this range of bias voltages, the CMOS integrated optical receiver response increases with the bias voltage due to increased avalanche gain of CMOS-APD. Fig. 4 also shows that the 3-dB bandwidth of receiver is enhanced to 2.25 GHz from 1.8 GHz for CMOS-APD alone. The measured transimpedance of 765 Ω corresponds well with the calculated result from the feedback resistance (R_F) used in the circuit considering the effect of output buffer and single-ended output connection.

III. Data Transmission Results

Using the fabricated CMOS integrated optical receiver, optical data transmission experiments were performed. The 850-nm optical signals were transmitted through 4-m-long multimode fiber and injected into the optical receiver using a

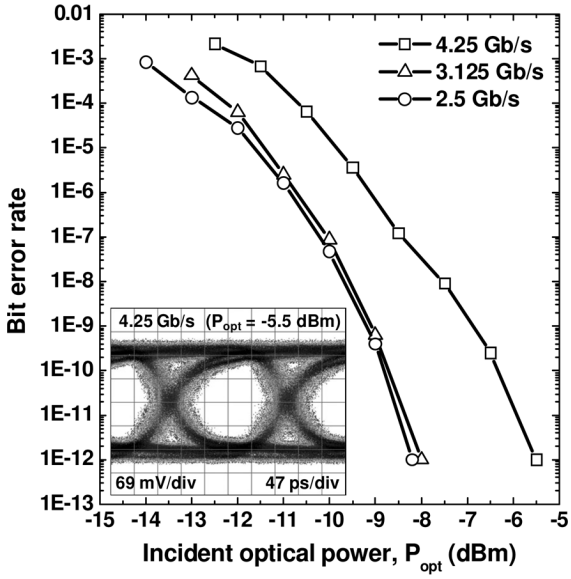


Fig. 5. BER as functions of incident optical power when 2.5-, 3.125-, and 4.25-Gb/s data are transmitted. The input data has PRBS $2^{31}-1$. Inset shows the eye diagram of 4.25-Gb/s data at output of the limiting amplifier. The incident optical power is -5.5 dBm.

lensed fiber. Fig. 5 shows measured bit-error rate (BER) of received data as functions of input optical power into the CMOS integrated optical receiver with three different data rates, 2.5, 3.125, and 4.25 Gb/s. The incident data had a pseudorandom bit sequence (PRBS) of $2^{31}-1$ and the CMOS-APD was biased at 10 V. The BER performance was experimentally found best at this bias voltage. At higher bias voltages, the response can be larger as can be seen from Fig. 4, but signal-to-noise ratio (SNR) degrades due to increased dark currents. In the experiment, a commercially available limiting amplifier operating at 4.25 Gb/s was used to satisfy the input dynamic range requirement for the BER tester (BERTScope 12500A). For the optical receiver, sensitivity of -8.2, -8, and -5.5 dBm were obtained for 10^{-12} BER with the data rate of 2.5, 3.125, and 4.25 Gb/s, respectively. From the observation that sensitivities for 2.5- and 3.125-Gb/s data are about the same, it can be determined that the receiver performance is limited by the receiver SNR at these data rates. For the higher data rate of 4.25 Gb/s, the performance is further limited by the receiver bandwidth. This limitation can be eliminated by adding equalization circuits in the receiver as have done in [3] and [4]. The inset of Fig. 5 shows the eye diagram at the output of the limiting amplifier when 4.25-Gb/s data were transmitted with the incident optical power of -5.5 dBm.

As can be seen in Table I, our CMOS-APD receiver shows better performance than other types of receivers having SML detector [1] or lateral PIN detector [2]. The sensitivity of our receiver is worse than that reported in [3] because N-well/P-substrate junction used for [3] absorbs more light than P^+/N-well junction used in our CMOS-APD, which with much better frequency response, is more suitable for high-speed optical receiver applications.

IV. Conclusion

A high-speed CMOS-APD integrated optical receiver is realized monolithically with 0.13-μm standard CMOS technology. A CMOS-APD and a TIA with negative capacitance are used which provide high-speed data transmission without any equalizer. Using the fabricated CMOS-APD integrated optical receiver, 4.25-Gb/s data are successfully transmitted at the input optical power of -5.5 dBm with BER less than 10^{-12}. These results show that CMOS-APD integrated optical receivers are promising for low-cost optical communication system applications.

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