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10 Gbps injection-locked CDR with a simple bit transition detector in 0.18 μm CMOS technology

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Abstract: A new and simple bit transition detection technique for non-return-to-zero (NRZ) signals is described. The bit transition detector uses MOSFET transistor's nonlinearity to extract return-to-zero (RZ) signals from NRZ signals. The resulting RZ signals can be used for injection-locking an oscillator, performing clock synchronization. A 10 Gbps injection-locked clock and data recovery (CDR) circuit is successfully demonstrated with the bit transition detector in 0.18 μm CMOS technology.

Keywords: CDR, injection-locking, clock recovery, clock and data recovery

Classification: Integrated circuits

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1 Introduction

There is a growing research interest for using an injection-locked oscillator

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(ILO) for synchronization circuits. [1, 2, 3, 4]. Since the phase response of an ILO is essentially equivalent to that of a first-order phase-locked loop (PLL) [1], ILOs can replace PLLs in synchronization circuits such as frequency dividers and clock recovery circuits. Furthermore, ILOs offer several advantages over traditional PLLs. First, they can operate at much higher frequency than PLLs due to their simple structure [2]. In particular, ILOs do not include flip-flop circuits, which often become the speed bottleneck in PLLs. Usually more than two flip-flops are required for a typical phase detector (PD) within a PLL. Second, ILOs do not need any loop filter capacitor, which usually occupies a much larger silicon area than the circuit core.

However, there are some disadvantages, too. The ILO free-running frequency must be close to the target frequency within the locking range. Otherwise, stable injection-locking cannot be achieved [3]. In addition, the injected signals must be periodic or includes harmonic tones of the target frequency in order to achieve injection locking. NRZ signals, the most commonly used signal format in high-speed signal interface applications, do not contain any spectral component at the bit rate frequency. Consequently, a bit transition detector, which converts NRZ signals into RZ signals that contain a strong spectral component at the bit rate frequency, must be used for realizing injection-locked clock recovery circuits.

2 Bit transition detector

The bit transition detector can be realized by either a time-domain or a nonlinear frequency-domain filter. The time-domain filter consists of a delay line and an XOR gate [2], and this is the bit transition detector that has been used for most injection-locked clock recovery circuits.

The nonlinear frequency-domain filter is realized by a differentiator followed by a rectifier performing harmonic generation [4]. This type of transition detector is less popular than the time-domain filter due to their difficulty in implementation. We propose a very simple version of frequency-domain bit transition detectors as shown in Fig. 1 (a).

A differential-pair signal can be defined using common mode voltage V_{COM} and time-varying component $V_{IN}(t)$:

$$\begin{cases} V_{IN+} = V_{COM} + V_{IN}(t) \\ V_{IN-} = V_{COM} - V_{IN}(t). \end{cases} \tag{1}$$

A typical MOSFET transistor has a square input-output relationship:

$$I_{DS} = \frac{KW}{L}(V_{GS} - V_T)^2, \tag{2}$$

where $K = \mu(\varepsilon_{ox}/t_{ox})$. Then, the output current $I_{OUT}(t)$ of the circuit in Fig. 1 (a) is:

$$I_{OUT}(t) = \frac{2KW}{L}\left[(V_{COM} - V_T)^2 + V_{IN}^2(t)\right]. \tag{3}$$

Eq. (3) shows that $I_{OUT}(t)$ consists of a DC part and a time-varying part, $2K(W/L){V_{IN}}^2(t)$. When the input signal switches its polarity, which

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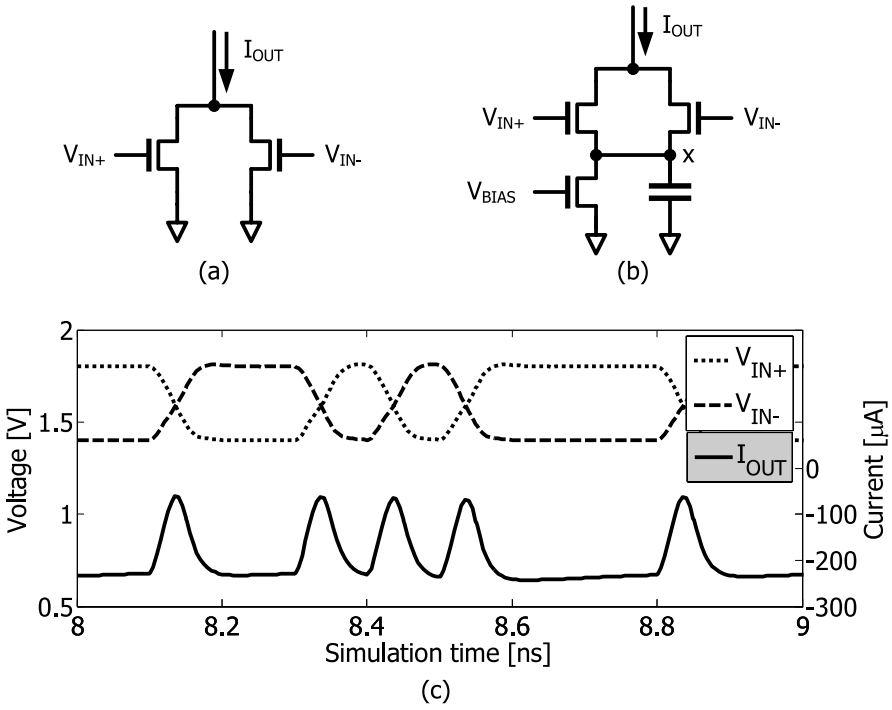

Fig. 1. Proposed bit transition detectors. (a) Basic structure of the bit transition detector. (b) Modified version for high common mode voltages. (c) Simulated waveforms of the proposed bit transition detector.

represents a bit transition, the time-varying part generates a current pulse in $I_{OUT}(t)$. The output pulse width is approximately the same as the slewing time of $V_{IN}(t)$. As a result, $I_{OUT}(t)$ becomes a RZ signal whose return-to-zero pulse represents the bit transition.

If the common mode voltage V_{COM} is so high that it is close to the power supply voltage such as in current-mode logic (CML) signaling, the proposed circuit in Fig. 1 (a) suffers from carrier velocity saturation [5] and it results in a linear I_{DS}-V_{GS} relationship. This will remove the time-varying part and make $I_{OUT}(t)$ have only a DC component.

To solve the high common mode voltage problem, the circuit in Fig. 1 (a) is modified into that shown in Fig. 1 (b). The gate-source voltage of the MOSFET pair can be effectively adjusted by adding a current-biasing MOS transistor. In this case a small capacitance should be added to avoid the source-degeneration effect. The capacitance provides a low-impedance path to the ground at the operation frequency, making node x a virtual AC ground for the NMOS pair. Fig. 1 (c) shows the HSPICE simulation results with 0.18 μm CMOS parameters for the circuit shown in Fig. 1 (b). The input data are 10 Gbps PRBS 2^7-1 NRZ data.

3 Clock and data recovery circuit

An injection-locked 10 Gbps CDR was designed using the proposed bit transition detector in a standard 0.18 μm CMOS technology. Fig. 2 (a) shows the

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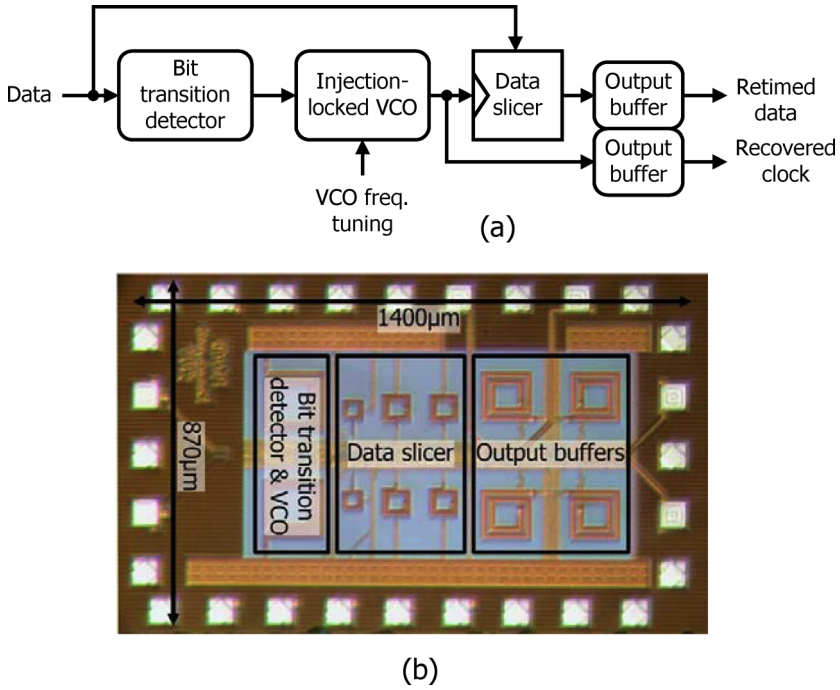

Fig. 2. (a) Schematic diagram of designed CDR. (b) Microphotograph of the fabricated CDR circuit.

schematic diagram and (b) the microphotograph of the designed circuit. An LC tank voltage controlled oscillator (VCO) is used as the injection-locking oscillator. Input data are sampled and retimed by the data slicer with the extracted clock signal. In order to make the data slicer as well as output buffers to handle very high frequency signals up to 10 GHz, the inductive-peaking technique with on-chip inductors are used [2]. The total chip area is pad-limited, and approximately 1400 μm by 870 μm. The designed chip is glued and bonded on the test PCB for measurement.

4 Measurement results

Fig. 3 (a) shows the measured eye-diagrams for 10 Gbsp 2^7-1 pseudo random

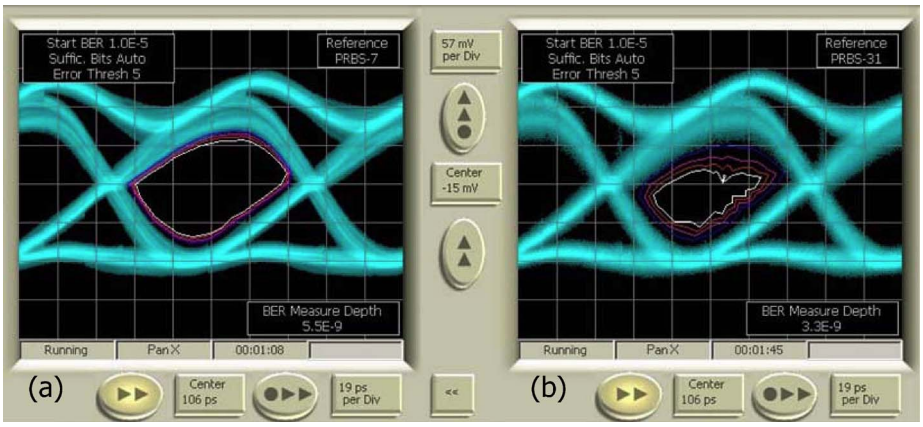

Fig. 3. Estimated BER contours overlapped on retimed data eye-diagrams. (a) With PRBS 2^7-1 patterns. (b) With PRBS 2^{31}-1 patterns.

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bit sequence (PRBS) input data and Fig. 3 (b) for 2^{31}-1. No bit error was detected over one-hour run for 2^{31}-1 PRBS input data. In the figure, BER contours for BER of 10^{-6}, 10^{-9}, 10^{-12} and 10^{-16} are also shown as overlapped contours. The innermost contours represent BER of 10^{-16}. With 1.8 V power supply, the measured power dissipation is only 10 mW for the CDR core, while the clock and data output buffers dissipates 80 mW. Table I summaries the measurement results and compare them previously reported injection-locked CDR circuits. We can achieve 10 Gbps operation with 0.18 μm CMOS technology and our CDR circuit consumes less power due to its simple structure.

Table I. Performance summary and comparison with other works.

	This work	Ref. [2]	Ref. [4]
Data rate	10Gbps	20Gbps	10.3Gbps
Process technology	0.18μm CMOS	90nm CMOS	45GHz–f_T SiGe
Chip area	1400μm x 870μm	800μm x 1200μm	730μm x 680μm
Power supply voltage	1.8V	1.5V	3.3V
Power consumption	90mW total, 10mW for CDR core only	175mW total	35mW for CDR core only
BER	No error detected over one hour run, estimated < 10^{-16} with 2^{31}–1 PRBS 500mV_{P-P} input)	< 10^{-12} for 2^9–1 PRBS, < 10^{-9} for 2^{31}–1 PRBS	< 10^{-12}

5 Conclusion

This paper presents a new and simple method for detecting bit transitions in NRZ signals and generating RZ signals suitable for injection locking. A 10 Gbps CDR circuit is realized with the bit transition detector in a standard 0.18 μm CMOS technology, and its operation is successfully demonstrated.

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