

A New Network Synchronizer Using Phase Adjustment and Feedforward Filtering Based on Low-Cost Crystal Oscillators

Chang-Kyung Seong, *Student Member, IEEE*, Seung-Woo Lee, and Woo-Young Choi, *Member, IEEE*

Abstract—A new network synchronizer using a two-way message exchange is proposed and implemented in a field-programmable gate array (FPGA). This synchronizer aligns its clock signal and time of day to that of the master node. For high-precision frequency control, a new phase adjustment method is employed, which efficiently provides high-frequency resolution and deterministic frequency control gain. In addition, a feedforward filter is used to reduce dithering of the time offset due to quantization errors in time-stamping. Even with a low-cost crystal oscillator, successful synchronization with root-mean-square (RMS) jitters of 0.1856 unit interval is achieved.

Index Terms—Filters, Global Positioning System (GPS), networks, phase control, synchronization.

I. INTRODUCTION

THE importance of time synchronization between remote network nodes has increased in real-time critical applications such as audio/video streaming, manufacturing automation, and mobile communication networks [1]–[3]. Although the GPS provides stable and accurate time synchronization, GPS receivers are still bulky and expensive. To achieve synchronization without many additional costs, approaches using the message exchange through legacy networks are interesting. Furthermore, it can be more attractive if low-cost crystal oscillators (XOs) can be used instead of temperature-compensated XOs or oven-controlled XOs.

Fig. 1 shows the two-way message exchange procedure between master and slave nodes described in Precision Time Protocol (PTP), or IEEE 1588, using the legacy Ethernet network [4]. This diagram has two independent time axes for master and slave nodes, respectively. Each axis shows time-of-day (ToD) values based on its own free-running oscillator. To synchronize the slave clock frequency and the ToD value to those of the master node, the slave node should measure the

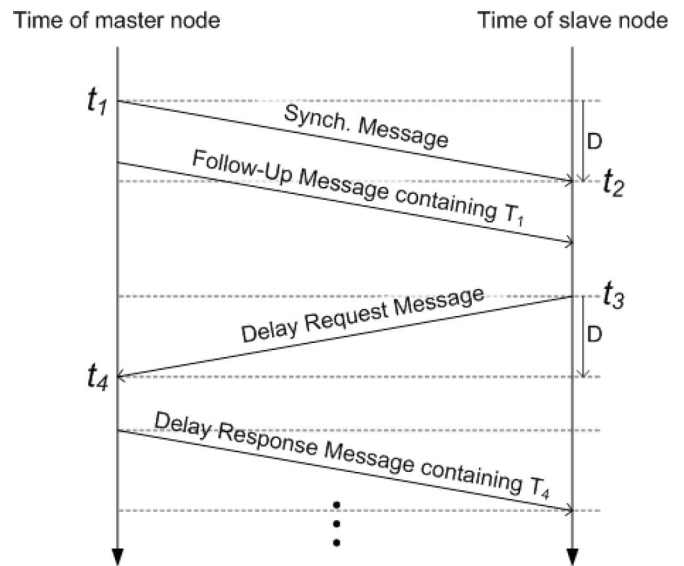


Fig. 1. One set of message exchanges between master and slave nodes to measure time offset and delay.

time offset and the propagation delay between two nodes. In PTP, one set of procedures consists of four messages. At the start of a set, the master node sends the *Synch Message* to the slave node. When the message arrives at the slave node after the delay time D , the slave node marks a time-stamp and stores the arrival time t_2 , which refers to its own ToD value. After a while, the *Follow-up Message* containing the departure time of the *Synch Message*, i.e., t_1 , is sent to the slave node. To separately calculate the delay time D and the time offset O , the slave node inversely sends the *Delay Request Message* to the master node at t_3 . When the master node detects this message, it stores the arrival time t_4 , which refers to the master's ToD value. By receiving t_4 contained in the *Delay Response Message* from the master node, the slave node is able to calculate O and D in the following manner:

$$O = \{(t_2 - t_1) - (t_4 - t_3)\} / 2 \quad (1)$$

$$D = \{(t_2 - t_1) + (t_4 - t_3)\} / 2. \quad (2)$$

Note that these equations are only valid when delays in both directions are symmetric.

In most previous works, only ToD values of the slave node have been considered as an object of synchronization [5]–[7]. However, this ToD synchronization has inherent performance

Manuscript received October 29, 2008; revised June 22, 2009; accepted July 4, 2009. Date of publication December 4, 2009; date of current version June 9, 2010. This work was supported by the IT R&D program of the Ministry of Knowledge Economy/Institute for Information Technology Advancement under Project 2009-S043-01 (Scalable Micro Flow Processing Technology Development). The Associate Editor coordinating the review process for this paper was Dr. Domenico Grimaldi.

C.-K. Seong and W.-Y. Choi are with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749 Korea (e-mail: wchoi@yonsei.ac.kr).

S.-W. Lee is with the Electronics and Telecommunications Research Institute, Daejeon 305-350, Korea.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TIM.2009.2028758

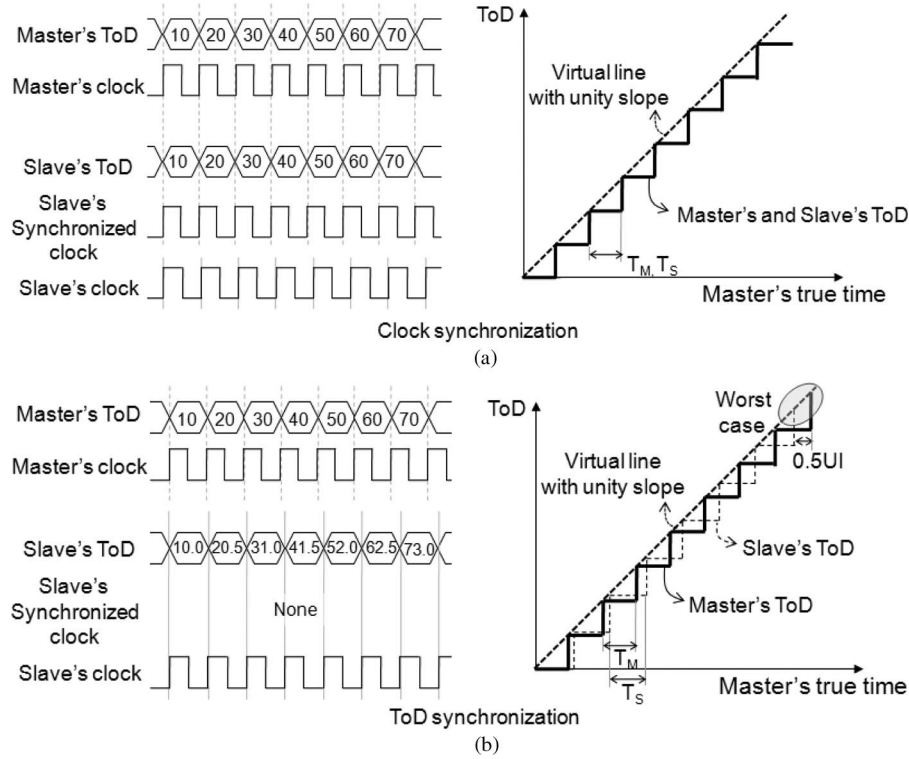


Fig. 2. Comparison of clock and ToD synchronization under successful synchronization: T_M and T_S are periods of master and slave clocks, respectively. (a) Clock synchronization. (b) ToD synchronization.

degradation compared with clock synchronization. In Fig. 2, the characteristics of the ToD and clock in the slave node are compared for ToD and clock synchronization techniques. In clock synchronization, the increasing step of the slave's ToD is fixed, and the ToD value always changes at the transition of the newly synchronized clock. If two nodes are successfully synchronized, they simultaneously have the same ToD values. On the other hand, in ToD synchronization, the slave's ToD value is arithmetically generated with a fractional part, and the ToD value changes at the transition of the slave's free-running clock without any correlation with the master clock. While ToD synchronization is simpler to implement than clock synchronization, two nodes that are only ToD synchronized may execute an assigned event with a timing error of 0.5 unit interval (UI) in the worst case.

We present a network synchronizer that achieves clock synchronization and considers the frequency drift d of low-cost XOs. In Section II, two major problems in clock synchronization are discussed. In Section III, the structure of our new synchronizer that can overcome these problems is presented. The synchronization algorithm, model, and analysis are also given in this section. A prototype system and its measurement results are described in Section IV. Finally, this paper is concluded in Section V.

II. PROBLEMS IN SYNCHRONIZATION

There are two major barriers to high-precision synchronization, namely, quantization effect in time-stamping and frequency resolution limit.

A. Quantization Effect in Time-Stamping

Time information, or ToD, is generated by a digital counter triggered by its own clock. With clock synchronization, the minimum step of the ToD is fixed to 1 UI of the clock. In reality, true departure and arrival times (t_1, t_2, t_3 , and t_4) in message exchanges are not generally integer multiples of UI. However, the measured time-stamp values are quantized to integer multiples of UI due to the nature of digital circuits. Since egress packets are time-stamped with the synchronous clock, the quantization error in departure time-stamps (t_1 and t_3) is constant. However, arrival time-stamps (t_2 and t_4) always encounter varying quantization errors due to time-stamping with the asynchronous clock. The true arrival time can be decomposed into two parts, i.e.,

$$t_k = [t_k] + e_k \quad (k = 2, 4) \quad (3)$$

where $[t_k]$ is the quantized time-stamp, and e_k is the quantization error. Since $[t_k]$ denotes rounding off of t_k to the nearest integer toward $-\infty$, $0 \leq e_k < 1$. The calculated time offset O' obtained from four time-stamps is also quantized and is different from the true time offset O , as shown in the following equation:

$$\begin{aligned} O' &= \{([t_2] - [t_1]) - ([t_4] - [t_3])\} / 2 \\ &= O - E \end{aligned} \quad (4)$$

where $E = (e_2 - e_4) / 2$. It can be shown that $-0.5 < E < 0.5$ because $0 \leq e_k < 1$.

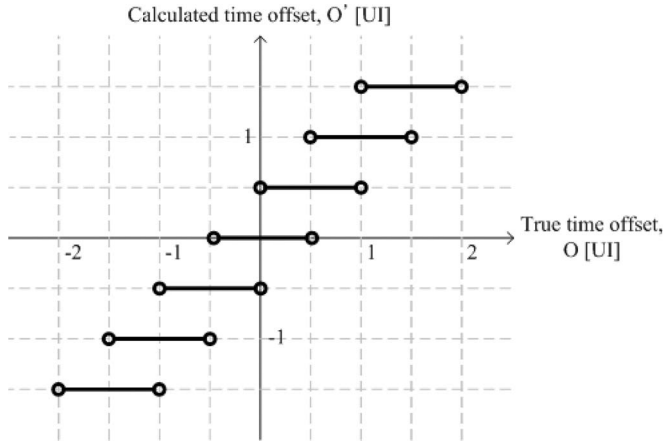


Fig. 3. Calculated time offset versus true time offset.

Fig. 3 plots the calculated time offset versus the true time offset. It is shown that one of two values of O' are mapped to one value of O depending on two variables, i.e., e_2 and e_4 . This uncertainty due to quantization degrades synchronization performance. Since O' under ± 0.5 UI is not detectable by a two-way message exchange, this range can be considered as a dead zone for detection. Without special techniques, the peak-to-peak time offset between two nodes cannot be less than 1 UI.

B. Frequency Resolution Limit

Analog voltage-controlled oscillators (VCOs) can generate continuous frequencies according to the applied control voltages. There have been several approaches to implement clock synchronizers based on analog VCOs [8], [9]. However, analog control is not suitable in network synchronization due to the relatively long update period. To use an analog VCO, the control voltage should be kept constant during every message exchange interval. It is very difficult to meet this constraint due to induced noises and leakage currents through shunt capacitors.

In digitally controlled clock synchronization systems, the controllable frequency step must be limited. Quantization errors due to the finite frequency step cause time error accumulation during every message exchange interval. The amount of time error accumulation is proportional to both the message exchange interval and the amount of the quantization error. As network systems demand longer message exchange intervals, a higher resolution frequency adjustment is required. The minimum frequency step should be small so that time error accumulation during a message exchange interval is less than the minimum detectable time offset [7], or

$$T \cdot \Delta f < 0.5 \tag{5}$$

where T is the normalized message exchange interval, Δf is the minimum frequency step, and the minimum detectable time offset is 0.5 UI, as can be seen in Fig. 3. In PTP, for instance, the default clock rate and the message exchange interval are 25 MHz and 2 s, respectively. These result in T of 5×10^7 UI, and the maximum allowed Δf should be less than 0.01 ppm. On the other hand, all nodes should be able to change

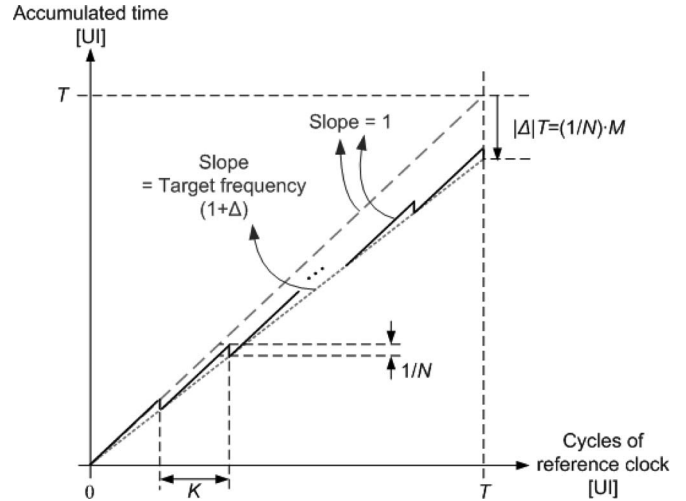


Fig. 4. Frequency control using phase adjustment.

their frequency rate up to ± 200 ppm because PTP allows the free-running frequency offset up to ± 100 ppm. In slave nodes, therefore, at least 15-bit digital codes are required to cover the frequency range from 0.01 to 200 ppm [7].

For digital clock frequency control, digitally controlled oscillators (DCOs) and digitally controlled XOs (DCXOs) have widely been used. Since it is difficult to make the resolution of DCO or DCXO more than 15 bits, $\Delta\Sigma$ digital-to-analog converters have been used to increase the effective frequency resolution [10], [11]. However, DCOs integrated on a silicon die suffer from fluctuation of free-running frequencies, poor phase noises, and process-voltage-temperature variation, yielding nondeterministic DCO gain and oscillation range. Although DCXOs have more stable oscillation frequencies and better phase noises compared with DCOs, they are expensive and have nondeterministic gain. To overcome these difficulties, we propose a new phase adjustment method using multiphase clock signals.

III. PROPOSED STRUCTURE

A. Phase Adjustment Method

We employ multiphase clocks that have the same frequency as the reference clock and are equally spaced in phases. Suppose that one of them can temporarily be selected as the slave clock. If the selected clock is periodically changed to the neighboring phase by one step, there will be periodic phase jumps forward or backward according to the direction of change. The slave clock newly generated by the phase jump has a different frequency from the reference clock. The amount of frequency difference is determined by the change period and the amount of phase jump, which depends on the number of phases N . Fig. 4 describes how to calculate the change period K to make the frequency offset Δ during T clock cycles with N phase clocks. The dashed gray line shows time accumulation versus the number of clock cycles of the reference clock, which naturally has unity slope. The dotted gray line is the desired behavior of the new slave clock with the target frequency offset or Δ . After T clock cycles, it is desired that two clocks have the

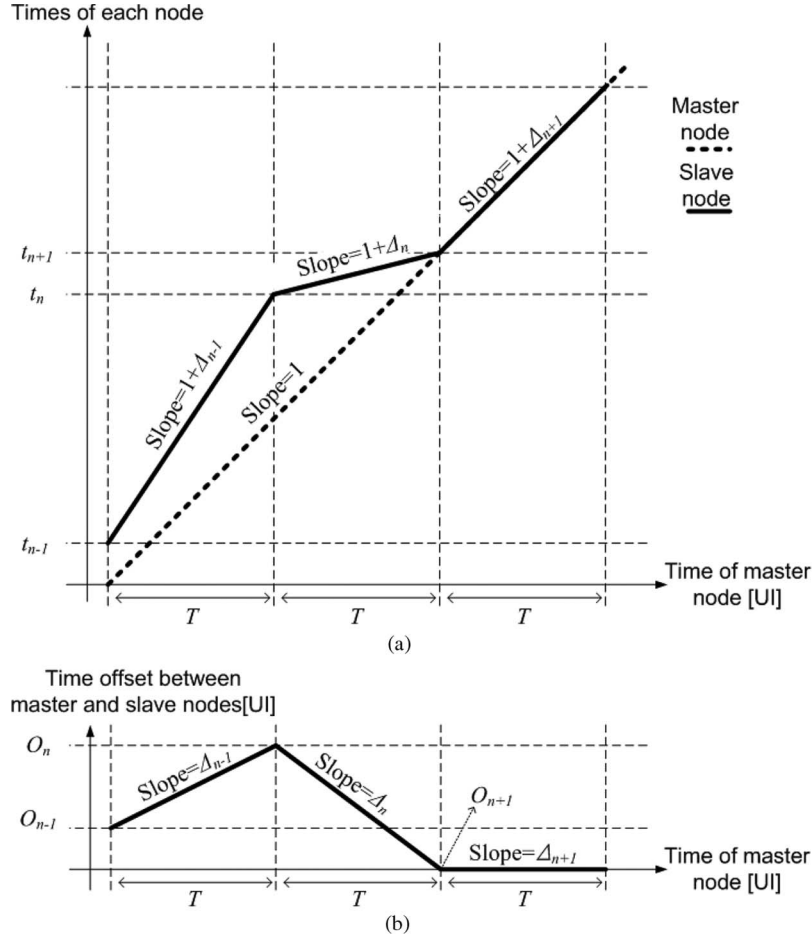


Fig. 5. Synchronization algorithm. (a) Time of the master node versus time of each node. (b) Time of the master node versus time offset between slave and master nodes.

difference of $|\Delta| \cdot T$ UI, and this should be equal to the total amount of phase shift $(1/N) \cdot M$, where M is the total number of phase changes, or

$$|\Delta| \cdot T = M/N. \quad (6)$$

Since the change period K is equal to T/M

$$K = 1/(|\Delta| \cdot N). \quad (7)$$

As shown in Fig. 4, there are periodic instantaneous phase jumps in this method. Since the timing issue is not critical in tens-of-megahertz operation, they do not matter if N is sufficiently large.

On the other hand, the proposed method provides almost infinite frequency resolution. By (6), the required amount of phase adjustment can arithmetically be calculated to achieve any target frequency offset. Note that the minimum achievable frequency offset is obtained when there is only one phase jump during the interval. By letting $M = 1$ in (6)

$$|\Delta_{\min}| = 1/N \cdot T \quad (8)$$

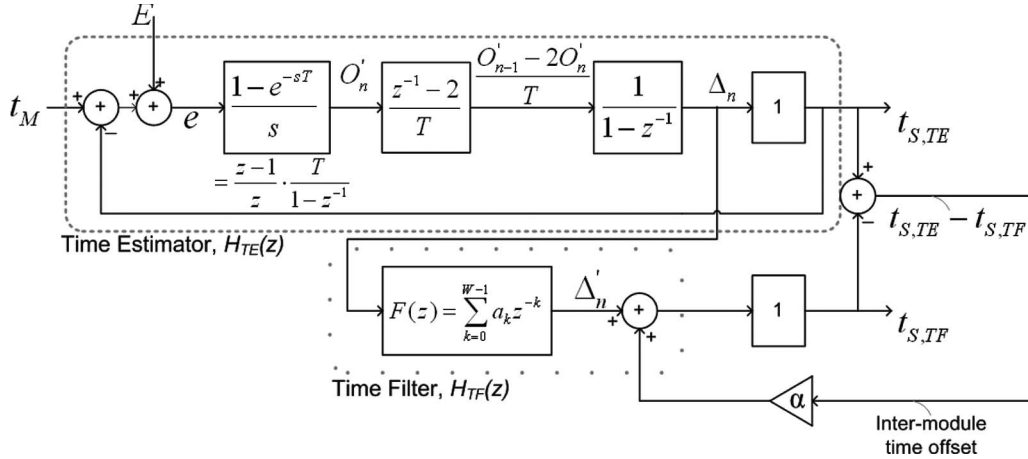
where Δ_{\min} is the minimum achievable frequency offset. In the default mode of PTP with a message exchange interval of 2 s at a 25-MHz operation ($T = 5 \times 10^7$), for example, the frequency

step up to 0.0025 ppm is controllable with $N = 8$. It is also remarkable that this method has deterministic control gain unlike DCOs and DCXOs because the frequency is determined by only deterministic values.

B. Synchronization Algorithm

Fig. 5(a) and (b) illustrates the simplified synchronization algorithm that is used in this paper. In Fig. 5(a), the horizontal and vertical axes represent the normalized ToD of the master and the normalized ToD of each node, respectively. Note that the slope represents the normalized clock frequency of each node. Therefore, the dashed line representing the master node time has unity slope. The segmented solid lines are the time accumulation of the slave node. The slave node adjusts its own clock frequency after every message exchange. Without perfect synchronization, the n th segment of the solid line has a slightly different slope with that of the master node due to the frequency offset Δ_n . Fig. 5(b) is a modified version of Fig. 5(a). Now, the vertical axis represents the time offset between slave and master nodes. By denoting the time offset at the n th message exchange by O_n , the rate of change for the time offset Δ_n can be expressed as

$$\Delta_n = (O_{n+1} - O_n)/T. \quad (9)$$


 Fig. 7. z -domain model of the proposed synchronizer.

filtered Δ_n , which is denoted by Δ'_n , has the same average but less fluctuation compared with Δ_n . As earlier mentioned, it is remarkable that the proposed phase adjustment method has deterministic gain. If there is a mismatch between two devices that generate the clock frequency in the TE and the TF, Δ_n and Δ'_n , which have the same average value, will produce different average frequencies in each module. In addition, the TF will fail synchronization to that of the master.

However, the clock of the TF only replicates the average frequency of the clock of the TE but is not aligned in time, even with feedforward filtering and deterministic gain in controlling frequency. There are three factors for misalignment, namely, the initial time offset, the roundoff error, and the frequency drift of the XO. First, since the TF have no information of the time offset, it maintains the initial time offset forever. Second, the roundoff error in Δ'_n makes the clock of the TF slightly drift. Third, the frequency drift of the XO directly effects on the time offset between the TF and the TE. To give time offset information to the TF, the IMTOD, which detects the time offset between the TE and the TF, is added. The intermodule time offset is multiplied by a scaling-down ratio α , and the result is added to Δ'_n . Finally, the sum of Δ'_n and the scaled intermodule time offset is fed into the PC in the TF and used for the calculation of the phase-shift period K_n in the same way as used in the TE module.

D. Model and Analysis

Fig. 7 is the z -domain model of the clock synchronizer. The error signal e , which is the difference between the slave's small-signal time $t_{S,TE}$ and the master's small-signal time t_M , is sampled at every T . E is the quantization error induced in time-stamping. By (12), the target frequency offset Δ_n accumulates $(O_{n-1} - 2O_n)/T$, and the slave's time is changed according to Δ_n . Excluding the effect of E , open- and closed-loop transfer functions are respectively obtained as follows:

$$G_{TE}(z) = (z^{-1} - 2)/(1 - z^{-1}) \quad (16)$$

$$H_{TE}(z) = t_{S,TE}/t_M = G_{TE}(z)/\{1 + G_{TE}(z)\} = 2 - z^{-1} \quad (17)$$

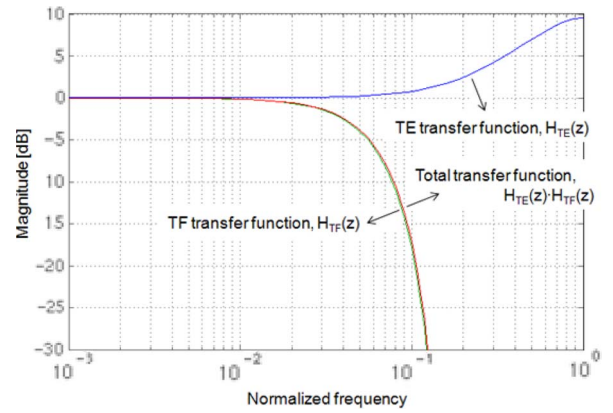


Fig. 8. Frequency response of the proposed synchronizer.

where $G_{TE}(z)$ is the open-loop transfer function of the TE, and $H_{TE}(z)$ is the closed-loop transfer function. Without considering the feedback path from the IMTOD for simple analysis, the transfer function of the TF, i.e., $H_{TF}(z)$, is the same as that of the FIR filter. Thus

$$H_{TF}(z) = t'_{S,TF}/t_{S,TE} = F(z) = \sum_{k=0}^{W-1} a_k z^{-k} \quad (18)$$

where $t'_{S,TF}$ is the small-signal time of the TF without the feedback path, $F(z)$ is the transfer function of the FIR filter, W is the number of taps, and a_k is the k th tap coefficient of the filter. Fig. 8 plots the frequency responses of the TE, the TF, and the entire system without the intermodule time offset feedback path, respectively. $H_{TE}(z)$ has all-pass characteristics with the lowest gain of 1 at dc and the highest gain of 3 at the sampling rate. The plotted $H_{TF}(z)$ is the frequency response of a 32-tap FIR filter with a normalized cutoff frequency of 0.028, which is used for the present prototype. By combining $H_{TE}(z)$ and $H_{TF}(z)$, the entire transfer function $t'_{S,TF}/t_M$ becomes very similar to $H_{TF}(z)$ having dc gain of 1 and low-pass characteristics. Therefore, the cascaded system attenuates high-frequency dithering of $t_{S,TE}$ but passes low-frequency deviation of t_M .

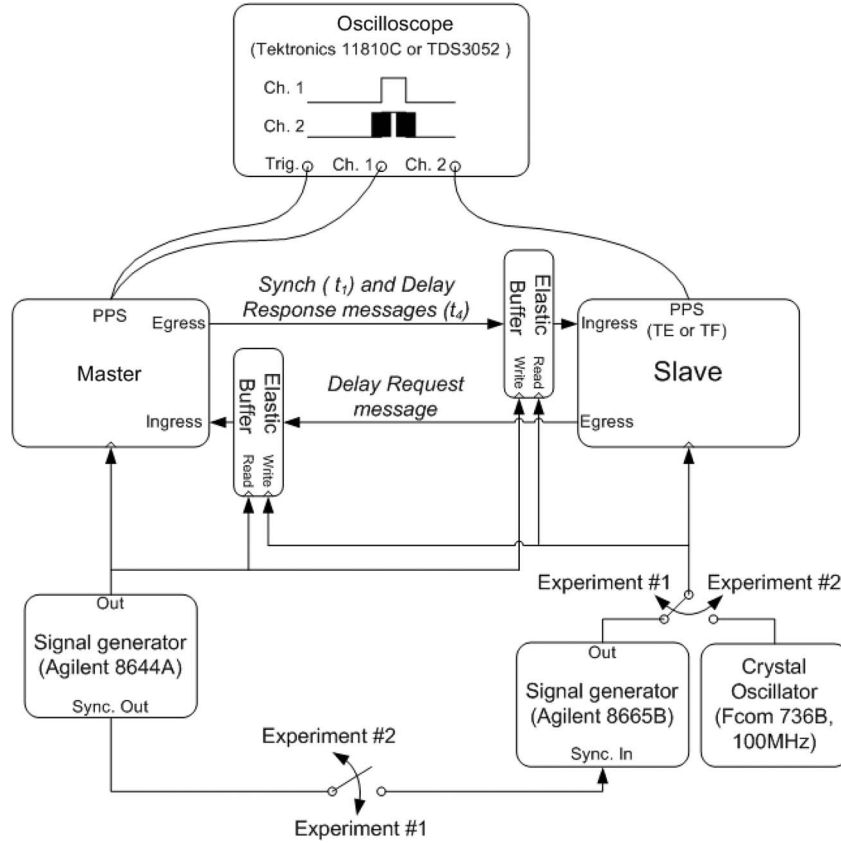


Fig. 9. Configuration of master and slave nodes and experimental setup.

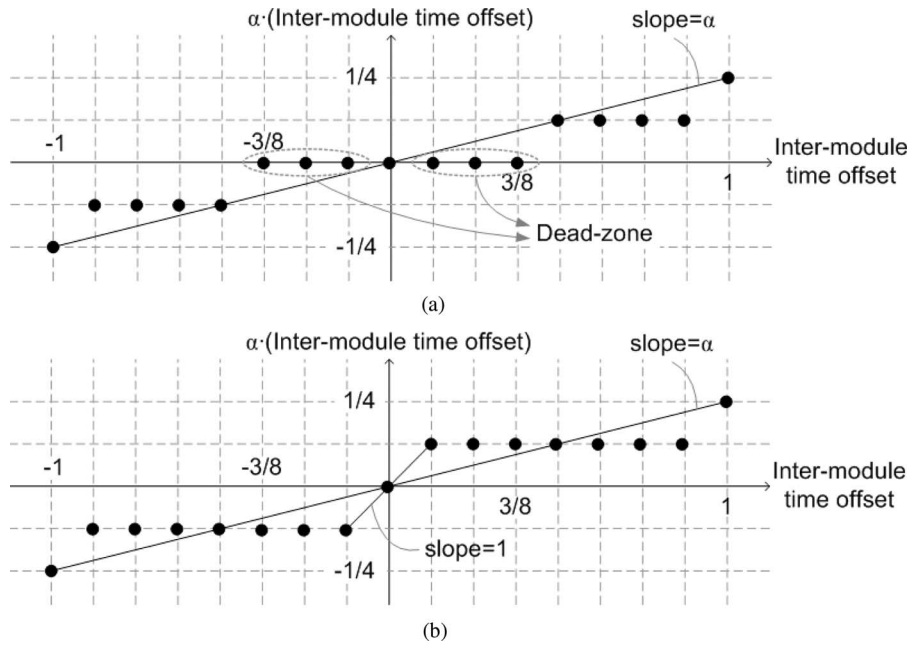


Fig. 10. Dead-zone elimination in scaling down the intermodule time offset when $\alpha = 1/4$. (a) Before compensation. (b) After compensation.

By considering the feedback path from the IMTOD, the following equations are sequentially derived:

$$t_{S,TF} = \alpha \cdot (t_{S,TE} - t_{S,TF}) + t'_{S,TF} \quad (19)$$

$$t_{S,TF} = \alpha/(1 + \alpha) \cdot t_{S,TE} + 1/(1 + \alpha)t'_{S,TF}. \quad (20)$$

Since $t'_{S,TF}$ is much smaller than $t_{S,TE}$ with a low enough cutoff frequency of the LPF, it can be ignored, and (20) becomes

$$t_{S,TF} = \alpha/(1 + \alpha) \cdot t_{S,TE}. \quad (21)$$

Equation (21) shows that there is a tradeoff between inherent jitter generation and tracking ability. To evaluate inherent jitter generation of the system, no external factors causing additional jitter should be assumed. In this case, the peak-to-peak dithering of $t_{S,TE}$ is fixed, as given in (15), and the peak-to-peak dithering of $t_{S,TF}$ monotonically decreases as α decreases by (21). Therefore, the smaller the α , the better the inherent jitter generation.

Considering the tracking ability of the system, on the other hand, the peak-to-peak dithering of $t_{S,TE}$ depends on external factors such as the oscillator drift and the packet delay variation. As α decreases, the gain from $t_{S,TE}$ to $t_{S,TF}$ also decreases in this case. Therefore, the smaller the α , the worse the tracking ability.

IV. IMPLEMENTATION AND MEASUREMENT

A. Implementation and Experimental Setup

Fig. 9 shows the configuration for the prototype system and the experimental setup. Both master and slave nodes are implemented with an FPGA. The master node comprises the ToD generator and the master message exchanger to handshake with the slave message exchanger in the slave node. The master message exchanger starts a set of message exchanges at every T and provides t_1 to the slave node with the *Synch Message* at every 2 s. In addition, it responds to the *Delay Request Message* from the slave and sends the *Delay Response Message* and t_4 .

When master and slave nodes are not initially synchronized, clock frequencies for each node are not equal. This can cause bit losses or duplications in two-way message exchanges due to timing slip between the transmitted bit and the sampling clock. In real network systems, there are clock and data recovery circuits and elastic buffers in physical layers of each node, and this problem does not occur. Because designing the physical layer is outside the scope of this paper, master and slave nodes are assumed to have initial bit synchronization. By inserting elastic buffers into each egress-to-ingress path and connecting write clock ports of master elastic buffers to the clock of the slave node, and vice versa, the problem of bit slip is eliminated.

The synchronizer operates with eight-phase 12.5-MHz clocks. To make eight-phase 12.5-MHz clocks, 100-MHz reference clocks are fed into each node. Agilent 8644B is used as a clock source for the master node. The master node also operates with a 12.5-MHz clock by dividing down the 100-MHz clock from the equipment. The reference clock of the slave node is fed by a low-cost 100-MHz XO (Fcom 736B). To compare the performance, a signal generator, namely, Agilent 8665B, is also used as a clock source. While the former is used for the case of a low-cost oscillator with frequency drift (Experiment 1 in Fig. 9), the latter is used for the case of fixed frequency offset (Experiment 2 in Fig. 9). Fixed frequency offset is obtained by externally synchronizing two signal generators.

The IMTOD detects the time offset using not only ToD values but also phase control codes of both modules. With eight-phase clocks, it calculates the time offset up to $1/8$ UI. Four values of α , such as 1, $1/2$, $1/4$, and $1/8$, are used because they can easily be implemented by the binary number bit

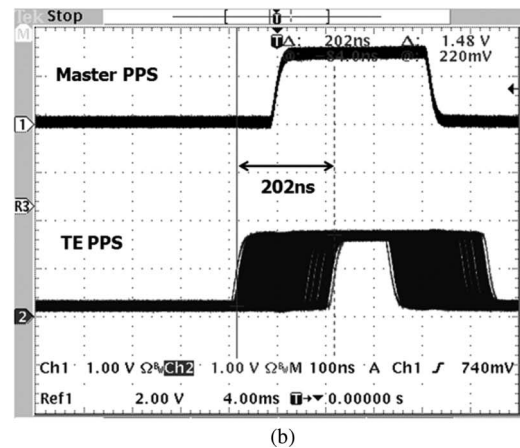
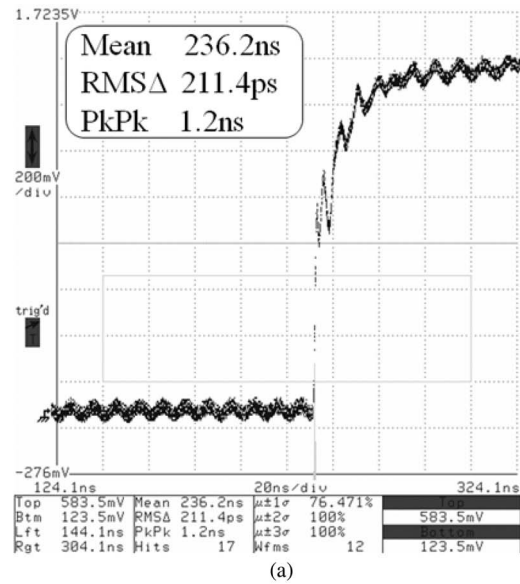


Fig. 11. Accumulated PPS waveforms. (a) Master's PPS. (b) TE's PPS.

shift. However, the roundoff error in scaling down becomes a problem. The case of scaling down to $1/4$ is shown as an example in Fig. 10. As shown in Fig. 10(a), the scaled value is zero when the input is within $\pm 3/8$, causing the dead zone in feeding back the intermodule time offset. To avoid this, the nonzero minimum output, or $1/8$, is mapped for the input in the dead zone, as shown in Fig. 10(b). As a result, the effective scaling-down ratio α_{eff} differs from α . Since the range of the dead zone becomes larger for smaller α , this effect gets severe as α decreases. Note that the effective scaling-down ratio for the minimum input is always unity.

The general method to evaluate synchronization systems is using pulses generated at every second, or pulses per second (PPS). Time separations of the slave node's PPS and the master node's PPS give time offset information, and their distribution provides the performance quality of synchronization systems. Although we have used pulses generated at every 2^{13} clocks instead of PPS due to the oscilloscope trigger problem, we use the word PPS for convenience in this paper. The PPS of master and slave nodes are fed into the oscilloscope for observation. Triggering the oscilloscope by the master's PPS, the relative position and distribution, or jitter, of the TE's and TF's PPS can be measured.

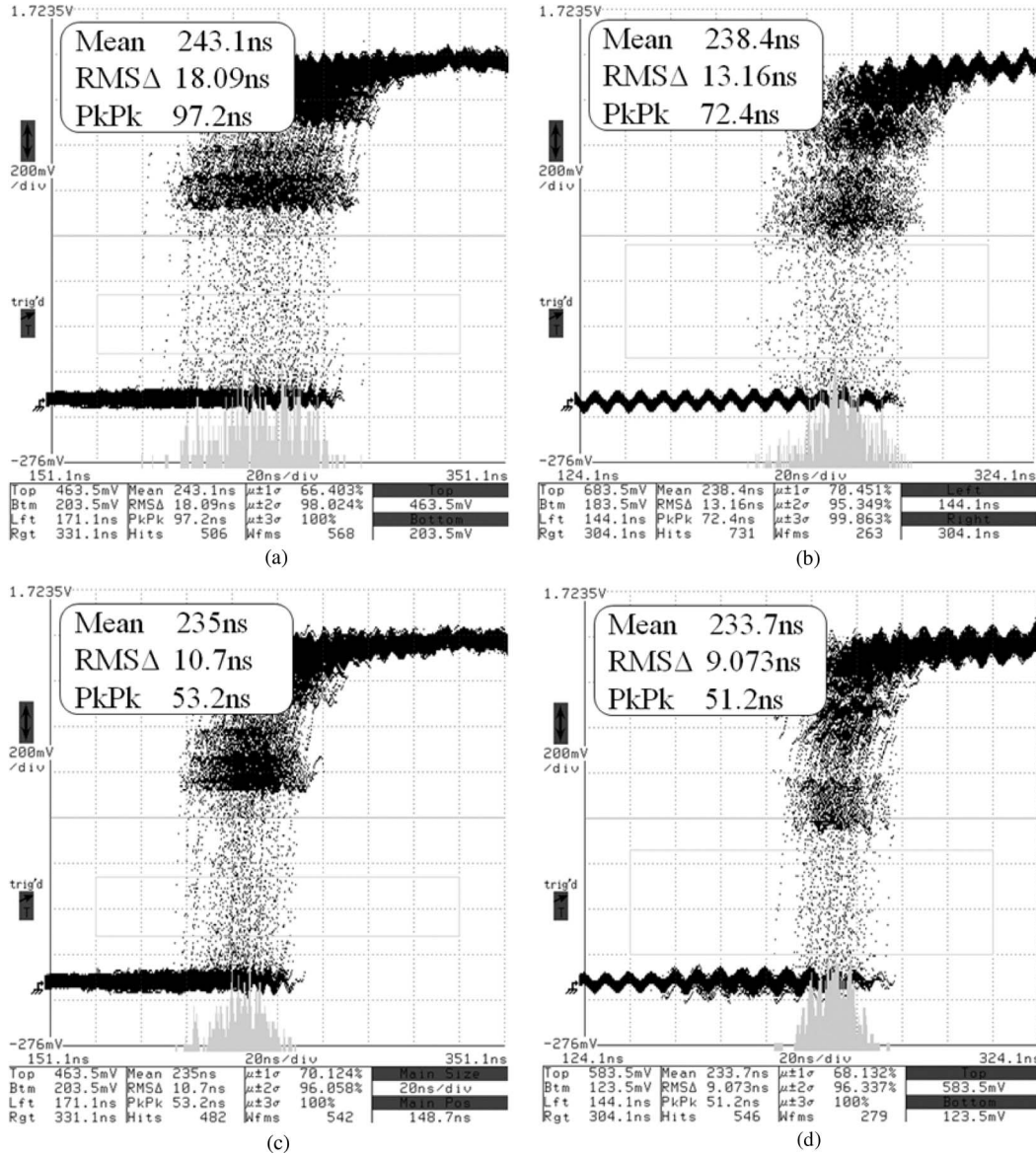


Fig. 12. Accumulated TF's PPS waveforms with fixed frequency offset for four cases of α . (a) $\alpha = 1$. (b) $\alpha = 1/2$. (c) $\alpha = 1/4$. (d) $\alpha = 1/8$.

B. Experimental Results

Fig. 11(a) and (b) shows the accumulated waveforms of the master's PPS and the TE's PPS, respectively. Since the accumulated master's PPS has the average of 236.2 ns in Fig. 11(a), this point is the average time that the TF's PPS should have. The accumulated TE's PPS has the peak-to-peak jitter of about 202 ns in Fig. 11(b).

Figs. 12 and 13 show the accumulated waveforms of the TF's PPS for four cases of α (1, 1/2, 1/4, and 1/8) in Experiments #1 and #2, respectively. In the case of Experiment #1, the frequency offset between two signal sources was fixed to +100 ppm.

Fig. 14 shows the dependence of peak-to-peak and RMS jitters of the TF's PPS on feedback gain α . The peak-to-peak jitters of the TF's PPS, i.e., $J_{S,TF,P-P}$, can approximately be calculated from (21), ignoring the effect of α_{eff} , i.e.,

$$J_{S,TF,P-P} \approx \alpha / (1 + \alpha) \cdot J_{S,TE,P-P} \quad (22)$$

where $J_{S,TE,P-P}$ is the peak-to-peak jitter of the TE's PPS. The solid line in Fig. 14 shows the normalized version of (22) in UI with the measured $J_{S,TE,P-P}$, or 202 ns. In addition, the measured $J_{S,TF,P-P}$ with fixed frequency offset versus four cases of α are plotted as rectangles in Fig. 14. It is shown that the TF's PPS has smaller peak-to-peak jitters as α decreases. The error between the calculated and measured values increases, however, as α decreases. This is because the error between α_{eff} and α gets larger as α decreases.

In Experiment #2, the RMS jitter is used for comparison since the peak-to-peak jitter is strongly affected by the instantaneous frequency drift of the free-running oscillator. The RMS jitter of the TF's PPS, i.e., $J_{S,TF,RMS}$, with the free-running XO versus four cases of α are plotted as circles in Fig. 14. As expected, a tradeoff between jitter generation and drift tracking ability is observed. It is shown that the best RMS jitter of 0.1856 UI is obtained when $\alpha = 1/4$. As α becomes smaller than 1/4, the RMS jitter

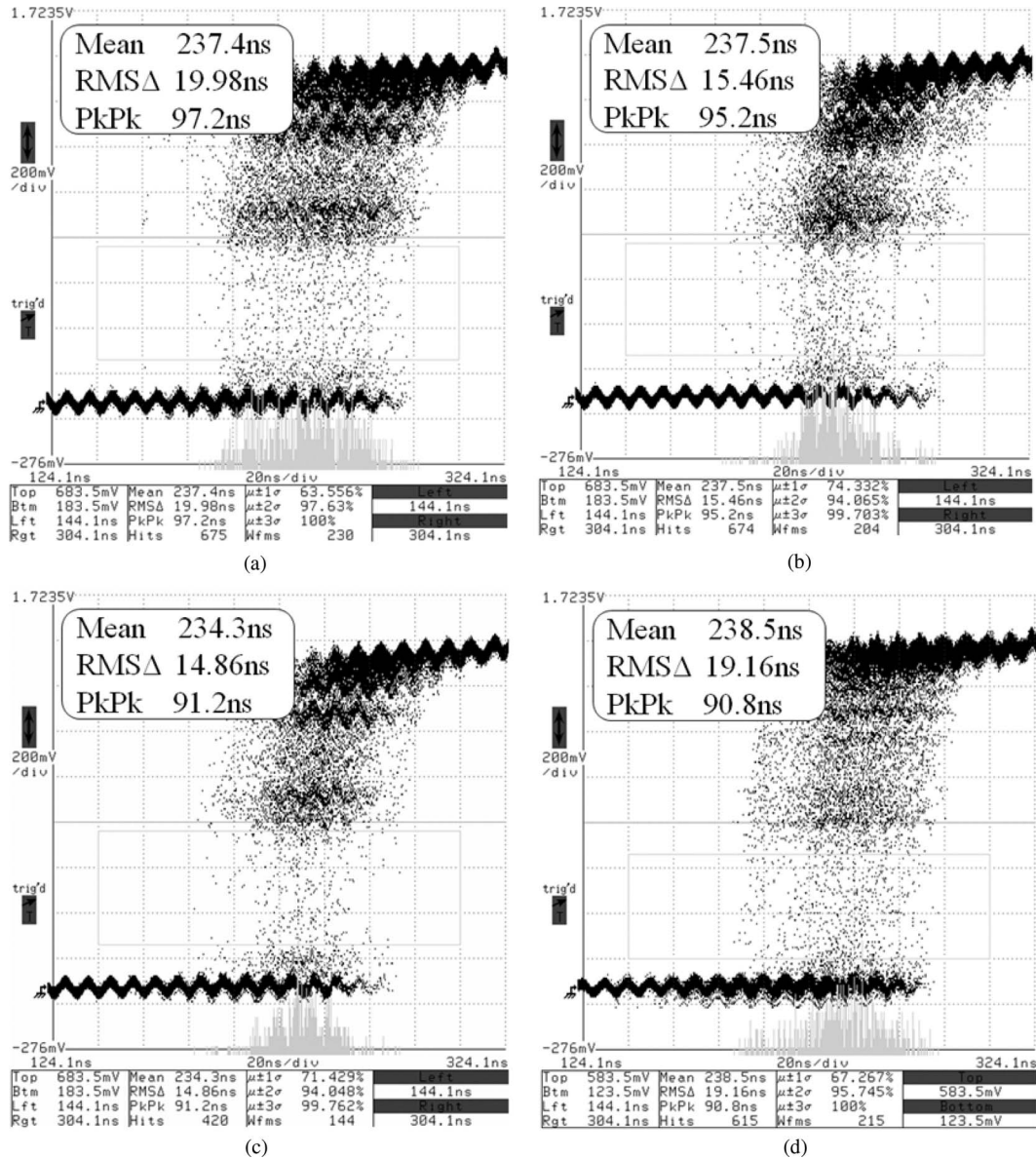


Fig. 13. Accumulated TF's PPS waveforms with frequency drift for four cases of α . (a) $\alpha = 1$. (b) $\alpha = 1/2$. (c) $\alpha = 1/4$. (d) $\alpha = 1/8$.

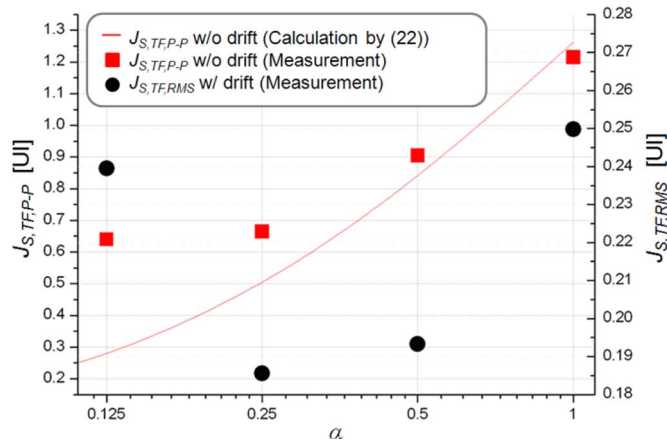


Fig. 14. Peak-to-peak and RMS jitters of the TF's PPS versus α .

increases because the TF cannot sufficiently track the frequency variation of the TE module due to the oscillator frequency drift.

In Figs. 11(a) and 13(c), the mean time error between the master's PPS and the TF's PPS at the best RMS jitter is 1.3 ns.

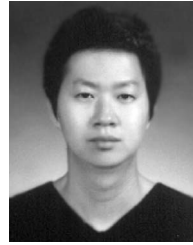
V. CONCLUSION

A new network synchronizer for clock synchronization with a low-cost XO has been presented. To overcome the frequency resolution limit in clock synchronization, the phase adjustment technique has been employed instead of direct frequency control. The synchronizer consists of TE and TF modules. Although the TE module tracks the frequency and time of the master node, its outputs suffer from dithering due to the quantization effect in time-stamping. To reduce it, the TF module takes feedforward low-pass filtering on the frequency output of the TE. The time offset between TE and TF modules are fed back with gain α into the TF to eliminate the time offset between outputs of the TF and the TE. The prototype system is implemented with an FPGA board, and its performance is evaluated under two conditions, namely, fixed

frequency offset and frequency drift. Without frequency drift between the master and the slave, smaller α shows better performance in PPS measurement. With frequency drift in a low-cost free-running XO, however, there exist certain conditions for the best result due to the tradeoff between jitter generation and drift tracking performance. Using an XO, the measured RMS jitter is 0.1856 UI with α of 1/4 with a message exchange interval of 2 s and eight-phase 12.5-MHz reference clocks.

REFERENCES

- [1] Draft Standard for Local and Metropolitan Area Networks, Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks, IEEE P802.1AS/D3.0, Jun. 24, 2008.
- [2] P. Ferrari, A. Flammini, D. Marioli, and A. Taroni, "IEEE 1588-based synchronization system for a displacement sensor network," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 2, pp. 254–260, Feb. 2008.
- [3] T. Cooklev, J. C. Eidson, and A. Pakdaman, "An implementation of IEEE 1588 over IEEE 802.11b for synchronization of wireless local area network nodes," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 5, pp. 1632–1639, Oct. 2007.
- [4] IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, IEEE Std. 1588-2008, Jul. 24, 2008.
- [5] P. Ferrari, A. Flammini, D. Marioli, and A. Taroni, "A distributed instrument for performance analysis of real-time Ethernet networks," *IEEE Trans. Ind. Informat.*, vol. 4, no. 1, pp. 16–25, Feb. 2008.
- [6] K. Schossmaier and D. Loy, "An ASIC supporting external clock synchronization for distributed real-time systems," in *Proc. 8th Euromicro Workshop Real-Time Syst.*, Jun. 1996, pp. 277–282.
- [7] J. C. Eidson, *Measurement, Control, and Communication Using IEEE 1588*. New York: Springer-Verlag, 2006, pp. 134–139.
- [8] K. Correll, N. Barendt, and M. Branicky, "Design considerations for software-only implementations of the IEEE 1588 Precision Time Protocol," in *Proc. Conf. IEEE-1588 Standard Precision Clock Synchronization Protocol Networked Meas. Control Syst.*, Winterthur, Switzerland, Oct. 2005.
- [9] P. Mueller, R. Luijten, and U. Bapst, "Hierarchical system synchronization and signaling for high-performance-low-latency interconnects," in *Proc. Conf. IEEE Electro/Inf. Technol.*, Lincoln, NE, May 22–25, 2005.
- [10] D.-H. Oh, D.-S. Kim, S. Kim, D.-K. Jeong, and W. Kim, "A 2.8-Gb/s all-digital CDR with a 10-bit monotonic DCO," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 222–223.
- [11] J. Lin, "A low-phase-noise 0.004-ppm/step DCXO with guaranteed monotonicity in the 90-nm CMOS process," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2726–2734, Dec. 2005.



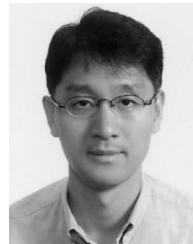
Chang-Kyung Seong (S'08) received the B.S. and M.S. degrees in electrical and electronic engineering in 2004 and 2006, respectively, from Yonsei University, Seoul, Korea, where he is currently working toward the Ph.D. degree.

His research interests are the design of synchronizer circuits for network synchronization and phase-locked loops, clock and data recovery, and adaptive equalizer circuits for high-speed I/O.



Seung-Woo Lee received the B.S., M.S., and Ph.D. degrees from Yonsei University, Seoul, Korea.

From 2002 to 2004, he was with the Analog IP Team, Hynix Semiconductor Inc. He joined the Electronics and Telecommunications Research Institute, Daejeon, Korea, in 2004 and is currently a Senior Member of Engineering Staff with the Next Generation Ethernet Team. His research interests are phase-locked loops, clock and data recovery, high-speed I/O, and network synchronization protocols.



Woo-Young Choi (M'92) received the B.S., M.S., and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, all in electrical engineering and computer science. For his Ph.D. thesis, he investigated MBE-grown InGaAlAs laser diodes for fiber-optic applications.

From 1994 to 1995, he was a Postdoctoral Research Fellow with NTT Optoelectronics Laboratories, where he worked on femtosecond all-optical switching devices based on low-temperature-grown InGaAlAs quantum wells. In 1995, he joined the

Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea, where he is currently a professor. His research interest is in the area of high-speed information processing technology, which includes high-speed optoelectronics, high-speed electronic circuits, and microwave photonics.