

BRIEF PAPER

Linear Analysis of Feedforward Ring Oscillators

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SUMMARY A linear model for feedforward ring oscillators (FROs) is developed and oscillator characteristics are analyzed using the model. The model allows prediction of multiple oscillation modes as well as the oscillation frequency of each mode. The prediction agrees well with SPICE simulation results.

key words: feedforward ring oscillator, ring oscillator, oscillator analysis

1. Introduction

Multiphase clocks are very useful for realizing high-speed data processing systems with low-speed circuit elements. Triggered in sequence by equally-spaced N-phase clock signals, multiphase systems can achieve N-times higher operating frequencies than single-phase clocked systems. For this reason, multiphase clocks are often used for such applications as high-speed analog-digital converters (ADCs) and clock and data recovery (CDR) circuits.

The ring oscillator (RO) structure is widely used for generating multiphase clocks. In feedforward ring oscillators (FROs) [1]–[7], feedforward signal paths are added between delay stages and can achieve much higher oscillation frequencies than conventional ROs without any feedforward paths [5], [6]. In addition, oscillation with an even number of single-ended delay stage [1], [3], [4], [7] can be achieved, which is not possible with conventional ROs. Although many different names have been used for FROs such as negative-skewed delay RO [1], coupled RO [3], and sub-feedback RO [7], we will use the name FRO in this paper.

FROs have been analyzed with several different methods. Well-defined models and equations are introduced in [2], [6], and the mechanism for the oscillation frequency enhancement characteristic of FRO is analyzed. However, these cannot predict oscillation modes. Consequently, oscillation frequency optimization based on these models is limited.

In this paper, a generalized linear FRO model is developed, which can cover a wide variety of FRO structures. The model allows prediction of multiple oscillation modes and oscillation frequencies. The accuracy of the model is verified with transistor-level simulation.

2. Analysis of FRO

A typical five-stage RO having an inverter as the delay stage is shown in Fig. 1(a). It has five output nodes and the signal at each node is represented by ck_1 through ck_5 . Figure 1(b) shows a five-stage FRO. The direct signal path from ck_i to ck_{i+1} is depicted in solid lines, and the feedforward signal path from ck_{i-1} to ck_{i+1} in dashed lines.

The unit delay stage can be defined as the simplest repeating circuit fragment as shown in Fig. 2(a) for RO and (b) for FRO. In Fig. 2(b), a normalized scaling factor α is used for the feedforward path inverter gain in a ratio to the direct path inverter gain.

A small-signal equivalent model for the unit delay stage of the conventional RO is shown in Fig. 3(a). The load capacitance C consists of input and output capacitances of the delay stage. The transfer function for the unit delay stage is given as

$$ck_{i+1} = H(f)ck_i = \frac{-g_m R}{1 + j2\pi fRC} ck_i \quad (1)$$

For this RO to achieve oscillation, its open-loop frequency response should reach unity. This condition can be expressed as

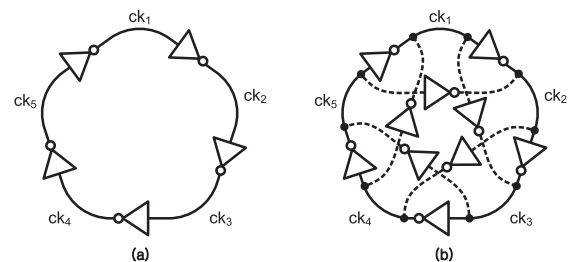


Fig. 1 Schematic diagram: (a) five-stage conventional RO (b) five-stage FRO.

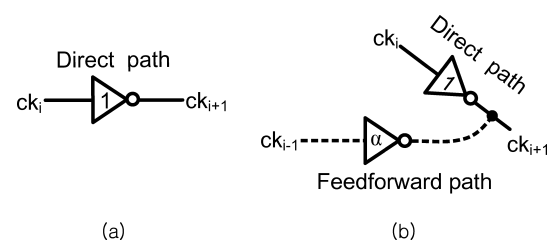


Fig. 2 Unit stage: (a) conventional RO (b) FRO.

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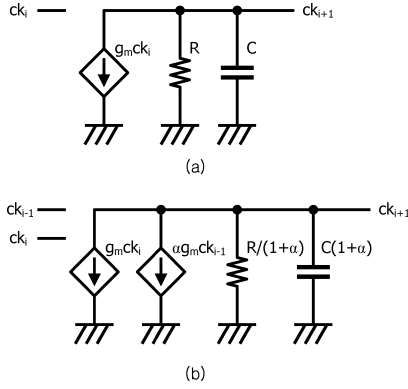


Fig. 3 A linear, small-signal equivalent circuit of the unit delay stage: (a) conventional RO (b) FRO.

$$\angle H(f_{osc}) = \frac{2\pi}{N}k = \theta_k \text{ for } k = 1, \dots, N-1 \quad (2)$$

and

$$|H(f_{osc})| = 1 \quad (3)$$

Where $\angle H(f_{osc})$ represents the phase response, and $|H(f_{osc})|$ the magnitude response, respectively, at the oscillation frequency f_{osc} .

The small-signal equivalent circuit for the FRO unit delay stage is shown in Fig. 3(b). The resistor in Fig. 3(b) represents two parallel resistors, R from the direct path and R/α from the feedforward path. The two parallel capacitors, C and αC , are also shown as a single capacitor, $C(1 + \alpha)$. The output signal ck_{i+1} can be expressed as the function of two input signals, ck_{i-1} and ck_i , as

$$ck_{i+1} = \frac{-g_m R}{(1 + \alpha)(1 + j2\pi f_{osc} RC)} (ck_i + \alpha ck_{i-1}) \quad (4)$$

In an oscillator in stable oscillation, any signals at two nodes have a constant phase relationship and, consequently, $\angle ck_i - \angle ck_{i-1} = \theta_k$ or $ck_{i-1}/ck_i = \exp(-j\theta_k)$. Note that this phase difference θ_k has the same meaning as θ_k given in (2).

The five-stage FRO in Fig. 1(b) has four phase values, $\theta_1, \dots, \theta_4$ for possible oscillation and they are graphically shown in Fig. 4.

Equation (4) can be rewritten with ck_{i-1} substituted by $ck_i \exp(-j\theta_k)$. Then ck_{i+1} can be expressed as a function of ck_i as

$$ck_{i+1} = G(\alpha)ck_i, \quad \text{where } G(\alpha) = \frac{-g_m R [1 + \alpha \exp(-j\theta_k)]}{(1 + \alpha)(1 + j2\pi f_{osc} RC)}. \quad (5)$$

The phase response of $G(\alpha)$ can be expressed as

$$\angle G(\alpha) = \pi + \beta - \gamma, \quad (6)$$

where β and γ represent the frequency-independent and frequency-dependent portion of the phase response, respectively, as given below:

$$\beta = \begin{cases} \tan^{-1}(Y/X), & \text{if } X > 0 \\ \tan^{-1}(Y/X) + \pi, & \text{if } X < 0 \end{cases},$$

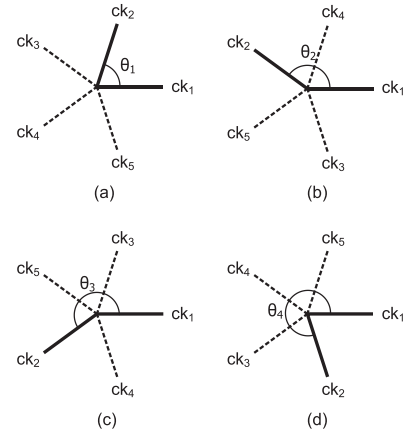


Fig. 4 Four phase values of five-stage FRO for possible oscillation; (a) $\theta_1 = 2\pi/5$. (b) $\theta_2 = 4\pi/5$. (c) $\theta_3 = 6\pi/5$. (d) $\theta_4 = 8\pi/5$.

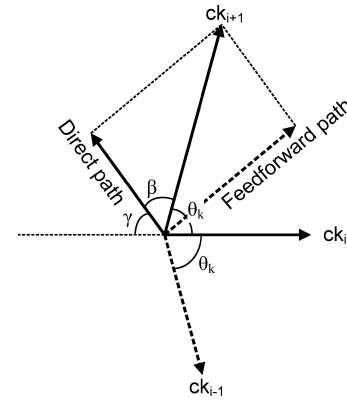


Fig. 5 Phase relationship between input and output signals of the unit stage.

$$\text{where } X = 1 + \alpha \cos \theta_k, \quad Y = -\alpha \sin \theta_k, \quad (7)$$

And,

$$\gamma = \tan^{-1}(2\pi f_{osc} RC). \quad (8)$$

In Fig. 5, the phase relationship between ck_{i-1} , ck_i and ck_{i+1} are depicted as vectors on a complex plane. Phase angle β is introduced by the feed-forwarded signal ck_{i-1} , which is lagging ck_i by θ_k . Since θ_k is constant in a specific oscillation mode, β is independent of the oscillation frequency and is determined solely by the feedforward strength α . To achieve oscillation in that mode, ck_i should be also lagging ck_{i+1} by θ_k or,

$$\pi + \beta - \gamma = \theta_k. \quad (9)$$

Using (8) and (9) we have

$$0 \leq \gamma \leq \pi/2, \quad \text{where } \gamma = \pi + \beta - \theta_k \quad (10)$$

The magnitude response of $G(\alpha)$ can be determined from (5), (7), (8) and (9).

$$|G(\alpha)| = \frac{g_m R}{(1 + \alpha)} \sqrt{\frac{X^2 + Y^2}{1 + \tan^2(\theta_k - \beta)}}$$

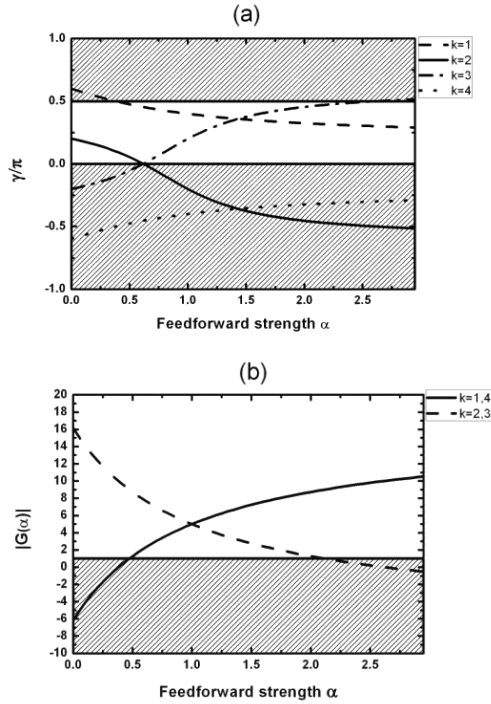


Fig. 6 Five-stage FRO characteristics: (a) Normalized frequency-dependent phase response γ and (b) Magnitude response $|G(\alpha)|$.

$$\begin{aligned}
 &= \frac{-g_m R}{(1 + \alpha)} \sqrt{X^2 + Y^2} (X \cos \theta_k + Y \sin \theta_k) \\
 &= \frac{-g_m R}{(1 + \alpha)} (\cos \theta_k + \alpha \cos 2\theta_k) \quad (11)
 \end{aligned}$$

Whether a given set of k and α can result in an oscillating FRO or not can be determined by checking first if γ given in (10) satisfies $0 \leq \gamma < \pi/2$ and $|G(\alpha)|$ in (11) is larger than one. The corresponding oscillation frequency f_{osc} can be calculated using (7), (8) and (9) as following:

$$\begin{aligned}
 f_{osc} &= \frac{\tan \gamma}{2\pi RC} = \frac{\tan(\beta - \theta_k)}{2\pi RC} = \frac{1}{2\pi RC} \left(\frac{(Y/X) - \tan \theta_k}{1 + (Y/X) \tan \theta_k} \right) \\
 &= \frac{-1}{2\pi RC} \left(\frac{\sin \theta_k + \alpha \sin 2\theta_k}{\cos \theta_k + \alpha \cos 2\theta_k} \right). \quad (12)
 \end{aligned}$$

3. Simulation Result of FRO

3.1 Dominant Mode Determination

The feedforward strength α is the key parameter for determining oscillation frequency, because α can change the dominant mode of FROs. α can be easily changed with transistor width. In order to predict the dominant mode of FROs, behaviors of FRO having $N=5$ are investigated with the above-described FRO model for $0 \leq \alpha < 3$.

Figures 6(a) and (b) show γ and $|G(\alpha)|$, respectively, for each k value in a five-stage FRO. It is assumed that the DC gain of the inverter used in the unit delay stage is 20, a typical value for a CMOS inverter. From the figure, the range of α can be determined for each k that satisfies the oscillation condition, $0 \leq \gamma/\pi < 0.5$ and $|G(\alpha)| > 1$. In the

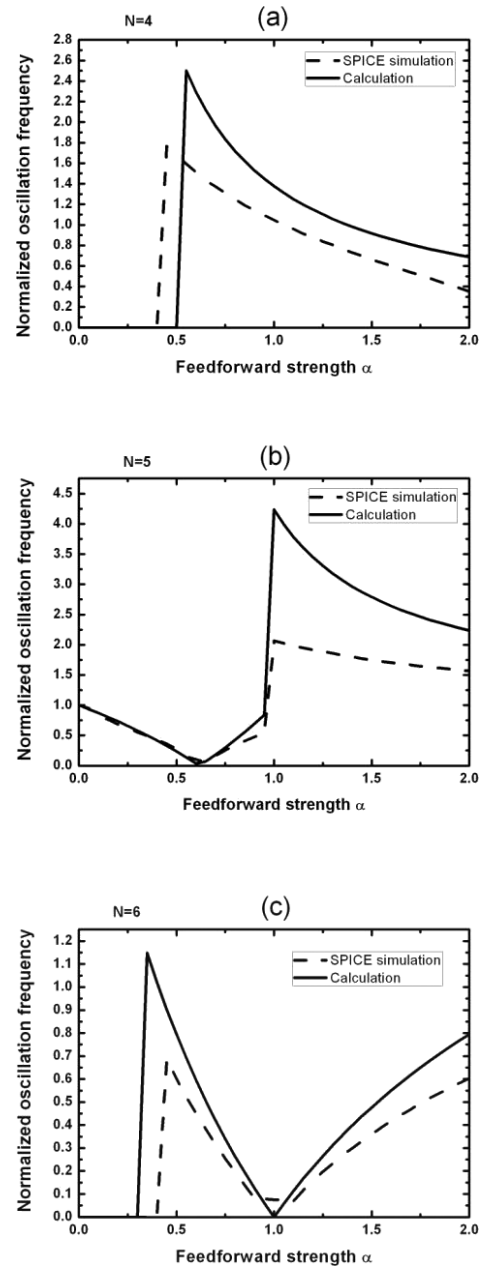


Fig. 7 Comparison between model-prediction and SPICE simulation results of various FRO. Oscillation frequencies are normalized with the value of five-stage FRO at $\alpha=0$.

figure, the shadowed regions represent those ranges where the oscillation condition cannot be satisfied. For example, for $0 \leq \alpha < 0.45$, only $k=2$ can satisfy the conditions. For $0.45 \leq \alpha < 0.6$, both $k=1$ and 2 can satisfy the conditions. If there are more than one oscillation modes at a give α , the one having the greatest $|G(\alpha)|$ becomes the dominant mode. Consequently, $k=2$ with the greater magnitude response is the dominant mode. For $0.6 \leq \alpha < 1$, $k=1$ and 3 both satisfy the oscillation conditions but $k=3$ is the dominant mode. Lastly, for $\alpha > 1$, $k=1$ and 3 both satisfy the conditions, but $k=1$ is the dominant mode.

The $k=1$ and 3 cases shown in Fig. 6 both satisfy the oscillation conditions and have the same magnitude response at $\alpha=1$. In this case, FRO oscillation modes compete with each other, and the one with the largest initial power-share wins following the “Winner-Takes-All” dynamics [8]. This implies that the dominant oscillation mode should have sufficient marginal magnitude gain to achieve stable oscillation.

3.2 Prediction vs. SPICE Simulation

In order to verify the accuracy of our model, behaviors of various FROs having $N=4, 5, 6$ are analyzed with our model, and compared with SPICE simulation results. Solid lines in Fig. 7 show the calculated oscillation frequencies for the dominant mode using Eq. (12) as α changes and dashed lines show SPICE-simulated oscillation frequencies. For easier comparison, oscillation frequencies in each figure are normalized with the oscillation frequency of five-stage FRO with $\alpha=0$.

It can be observed that the agreement is good except in the region where oscillation frequencies change abruptly. This is due to the fact that our FRO model is based on a small-signal model which assumes fixed bias conditions for each device. This assumption is appropriate when the FRO is in stable oscillation, however, it fails when a strong positive feedback pushes MOS transistors into the linear region. Such a strong positive feedback occurs in the region where the oscillation frequency changes abruptly due to the mode switching. However, overall dependence of oscillation frequencies on α shows a good agreement and, in particular, α values where the mode transition occurs are very well predicted by our model. In other words, we can reliably use our model to determine α for the mode having the desired oscillation frequency characteristics.

4. Conclusion

In this paper, a simple linear FRO model and design equa-

tions are developed. The model is verified with SPICE simulation. It is shown that our model can predict FRO behaviors accurately in all number of delay stages. This should be a very useful design guide for FRO circuits.

Acknowledgments

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References

- [1] S.J. Lee, B. Kim, and K. Lee, “A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme,” *IEEE J. Solid-State Circuits*, vol.32, no.2, pp.289–291, 1997.
- [2] S. Lizabeth and T.A. Kwasniewski, “A 1.25-GHz 0.35- μm monolithic CMOS PLL based on a multiphase ring oscillator,” *IEEE J. Solid-State Circuits*, vol.36, no.6, pp.910–916, 2001.
- [3] A. Rezaee and K. Martin, “A coupled two-stage ring oscillator,” *Proc. 44th IEEE 2001 Midwest Symposium on Circuits and Systems, 2001 (MWSCAS 2001)*, vol.2, 2001.
- [4] M. Grozing, B. Phillip, and M. Berroth, “CMOS ring oscillator with quadrature outputs and 100 MHz to 3.5 GHz tuning range,” *Proc. 29th European, Solid-State Circuits Conference, 2003 (ESS-CIRC’03)*, pp.679–682, 2003.
- [5] Y.A. Eken and J.P. Uyemura, “A 5.9-GHz voltage-controlled ring oscillator in 0.18 μm CMOS,” *IEEE J. Solid-State Circuits*, vol.39, no.1, pp.230–233, 2004.
- [6] H.Q. Liu, W.L. Goh, and L. Siek, “Design and frequency/phase-noise analysis of a 10-GHz CMOS ring oscillator with coarse and fine frequency tuning,” *Analog Integr. Circuits Signal Process.*, vol.48, pp.85–94, 2006.
- [7] S. Lizabeth, T. Kwasniewski, and K. Iniewski, “A quadrature output voltage controlled ring oscillator based on three-stage sub-feedback loops,” *Proc. 1999 IEEE International Symposium on Circuits and Systems 1999 (ISCAS’99)*, vol.2, pp.176–179, 1999.
- [8] K. Otsuka, “Winner-takes-all dynamics and antiphase states in modulated multimode lasers,” *Physical Rev. Lett.*, vol.67, pp.1090–1093, 1991.