A 10-Gb/s Adaptive Look-Ahead Decision Feedback Equalizer With an Eye-Opening Monitor

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***Abstract*—We demonstrate a novel adaptive look-ahead decision feedback equalizer (LADFE) that uses the measured eye diagram for equalization adaptation and verification. The eye diagram is obtained with a new type of eye-opening monitor (EOM), which measures the magnitude of the received signals having different data patterns and, using this, estimates intersymbol interference and determines the amount of adaptation needed for the LADFE. A 10-Gb/s adaptive two-tap LADFE with an EOM is fabricated in 90-nm CMOS technology. The eye diagrams for equalized signals are successfully obtained, and adaptation of the LADFE is achieved for PCB channels up to 40 cm. The LADFE core occupies $110 \times 95\ \mu m^2$ and consumes 11 mW at 1.2-V supply voltage.**

***Index Terms*—Adaptive equalizer, decision feedback equalizers (DFEs), eye-opening monitor (EOM), intersymbol interference (ISI).**

I. Introduction

As THE required data rate for wire-line interconnect systems becomes more demanding, the need for high-speed equalizers that can compensate high-frequency channel loss significantly increases. In particular, adaptive equalization is strongly desired so that equalizers can automatically compensate losses for unknown and/or time-varying channels [1]–[3].

Among various equalizer filters, decision feedback equalizers (DFEs) have been widely used in high-speed applications recently [4]–[6]. Sample-and-hold circuits for soft decision [4] and switched capacitors [6] have been used in DFEs so that marginal decision time can be extended. A current-integrating summer that eliminates systematic frequency-dependent loss inherent in conventional DFEs was proposed in [5]. DFEs provide good noise performance, but they require a very stringent timing margin at the first feedback path, and consequently, many high-speed DFEs employ the look-ahead structure [7], [8].

A look-ahead DFE (LADFE) has multiple decision paths with different tentative postcursors corresponding to several data patterns, from which the desired data are selected based on the past data pattern, as shown in Fig. 1. For example, a one-tap full-rate LADFE shown in Fig. 1 first produces two candidate signals y_1 and y_0 by applying DFE coefficients α_1 and $-\alpha_1$, respectively, to the received signal r. It decides y_1 for the desired equalized output if the previous data value is 1 or y_0 if it is 0. DFE coefficients can be preset for a known channel, or they can be adaptively determined for unknown channels with algorithms such as a least-mean-square algorithm [9].

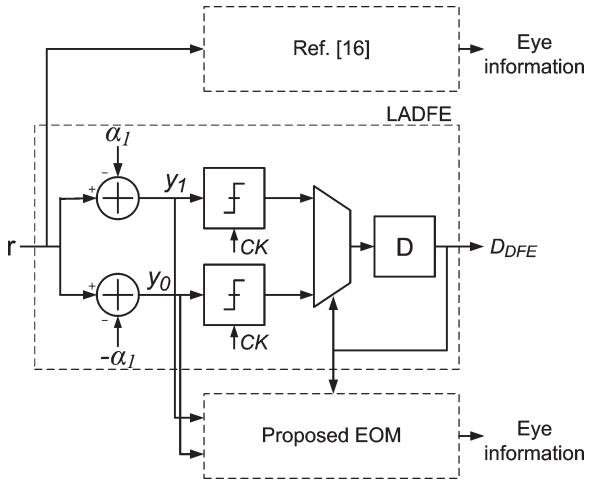

Fig. 1. Block diagram of a one-tap full-rate LADFE and comparison of the conventional and proposed EOMs.

In many applications, on-chip eye-opening monitors (EOMs) are used to verify the proper operation of equalizers and to estimate receiver bit-error rates (BERs) [10], [11]. There have been several reports for continuous-time linear equalizers (CTLEs) with EOMs, which directly monitor CTLE outputs [12]–[15]. However, such direct monitoring is not applicable to LADFEs because LADFEs produce sliced digital outputs, which always produce clean eye diagrams whether they contain errors or not. Consequently, an indirect technique based on BER estimation [10], [16] has been used for monitoring the operation of LADFEs.

In this brief, we demonstrate a new adaptive LADFE having the complete EOM capacity without any additional logic for a BER estimation. This brief differs from [2] in that our architecture is capable of producing an EOM, which is not possible in the earlier paper. In addition, our architecture utilizes the EOM, from which the level of intersymbol interference (ISI) can be directly measured from candidate signals and used for equalization adaption, whereas [2] applied sign-based zero-forcing algorithm on LADFE output for adaptation. Our new architecture obtains histograms of equalized waveforms with different data patterns using the EOM. By measuring the peak positions in histograms, the amount of ISI can be determined, as well as the DFE coefficients.

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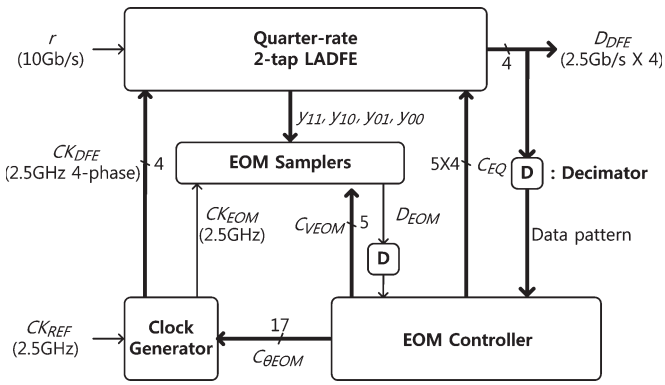

Fig. 2. Overall configuration of the prototype system.

II. Equalizer Structure

A. Overall Configuration

Fig. 2 shows the overall configuration for our equalizer. It consists of a LADFE, an EOM sampler, an EOM controller, a clock generator, and decimators. The LADFE receives 10-Gb/s signal r and compensates two postcursors with four 5-bit DFE codes C_{EQ} from the EOM controller, producing four candidate signals y_{11}, y_{10}, y_{01}, and y_{00}.

The EOM sampler scans these candidate signals two-dimensionally with $\mathrm{CK}_{\mathrm{EOM}}$, which is the EOM clock signal, and C_{VEOM}, which is the digital code for the EOM reference voltage. The vertical levels of the candidate signals are sensed by comparing these with the EOM reference voltage. In addition, $\mathrm{CK}_{\mathrm{EOM}}$ samples the results of comparison at the phase of $\mathrm{CK}_{\mathrm{EOM}}$ or θ_{EOM}. The EOM controller sequentially controls both C_{VEOM} and θ_{EOM} to scan one unit interval (UI) of the eye diagram. The scanned result D_{EOM} is transmitted to the EOM controller, which then combines D_{EOM} to produce an eye diagram.

Since our LADFE operates in the quarter rate to reduce the speed burden of sampling circuits, its output has four channels of data D_{DFE}. The clock generator provides four quarter-rate DFE clocks $\mathrm{CK}_{\mathrm{DFE}}$ to the LADFE by interpolating the reference clock $\mathrm{CK}_{\mathrm{REF}}$. An external clock source, which is frequency synchronized to the received signal, is used for $\mathrm{CK}_{\mathrm{REF}}$ in our chip instead of the recovered clock from input data since our prototype chip does not include a clock and data recovery circuit.

B. LADFE and EOM Circuits

The block diagram and the timing diagram for the quarter-rate two-tap LADFE are shown in Fig. 3. The LADFE equalizes the received signal r using four 5-bit DFE codes C_{EQ11}, C_{EQ10}, C_{EQ01} and C_{EQ00}. and four-phase clocks $\mathrm{CK}_{\mathrm{DFE,I+}}$, $\mathrm{CK}_{\mathrm{DFE,Q+}}$, $\mathrm{CK}_{\mathrm{DFE,I-}}$ and $\mathrm{CK}_{DFE,\mathrm{Q-}}$. Four 5-bit digital-to-analog converters changes DFE codes into analog voltages, V_{EQ11}, V_{EQ10}, V_{EQ01}, and V_{EQ00}. Postcursors are compensated using these coefficients, resulting in candidate signals, y_{00}, y_{01}, y_{10}, and y_{11}.

The LADFE samples and quantizes each of four candidate signals by four-phase clocks, generating 16 data samples. Then, 4 : 1 multiplexers (MUX) select the final output data according to the prior 2-bit-data pattern. As shown in the simplified timing

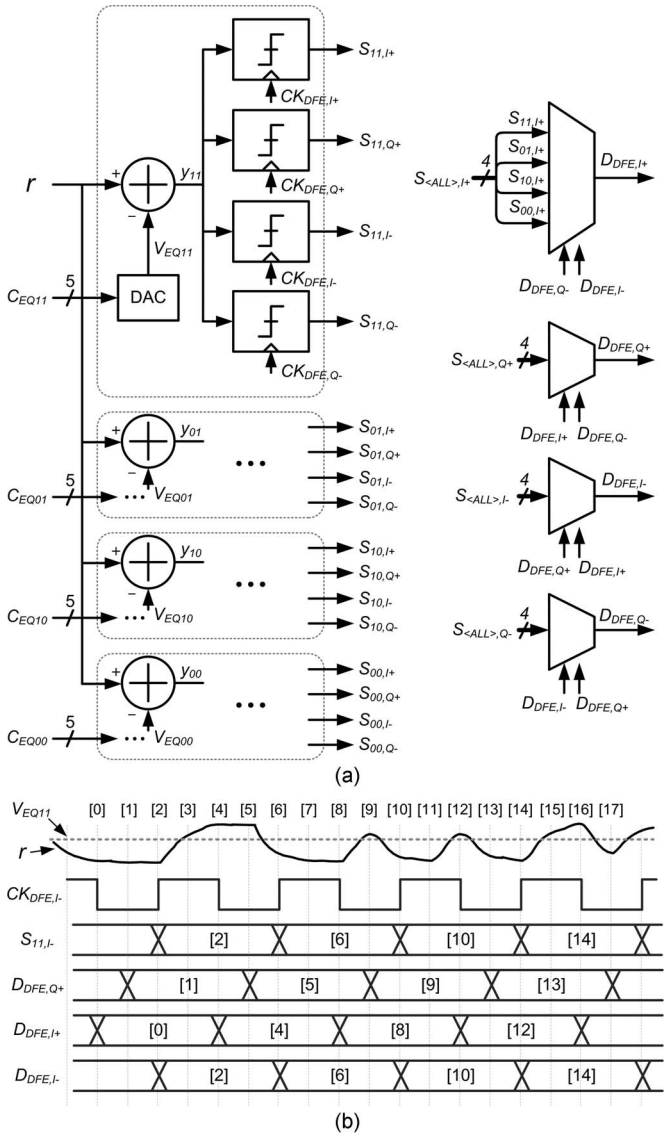

Fig. 3. Designed two-tap quarter-rate LADFE. (a) Block diagram. (b) Timing diagram.

diagram in Fig. 3(b), since $S_{11,\mathrm{I-}}$ are sampled at the phase of 180° by $\mathrm{CK}_{\mathrm{DFE,I-}}$, $D_{\mathrm{DFE,I-}}$ is determined by $D_{\mathrm{DFE,I+}}$ and $D_{\mathrm{DFE,Q+}}$, which are sampled at the phase of 0° and 90° by $\mathrm{CK}_{\mathrm{DFE,I+}}$ and $\mathrm{CK}_{\mathrm{DFE,Q+}}$, respectively.

Fig. 4 shows how an eye diagram is constructed with candidate signals in our LADFE. Segmented bold lines are the candidate signals that have the best bit-error probability, and thin lines that should be dropped out. The eye diagram of equalized signals can be realized with combined bold lines.

Fig. 5 shows a block diagram of the EOM sampler. Our EOM sampler uses one voltage V_{EOM} and one clock $\mathrm{CK}_{\mathrm{EOM}}$ to obtain the eye diagram for simplicity. To scan the candidate signals, the differences between all candidate signals and V_{EOM} are sampled at θ_{EOM}. Since the phase of $\mathrm{CK}_{\mathrm{EOM}}$ varies from -0.5 UI to $+0.5$ UI around that of $\mathrm{CK}_{\mathrm{DFE,I-}}$, eye monitoring is obtained around the sampling time of $\mathrm{CK}_{\mathrm{DFE,I-}}$. As in the LADFE, the MUX selects one valid data referring to prior 2 bits $D_{\mathrm{DFE,I+}}$ and $D_{\mathrm{DFE,Q+}}$ to monitor only the effective equalized signal.

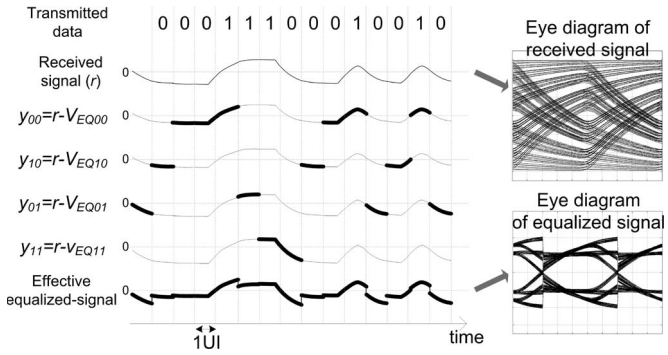

Fig. 4. Acquisition of eye diagram from candidate signals in the LADFE.

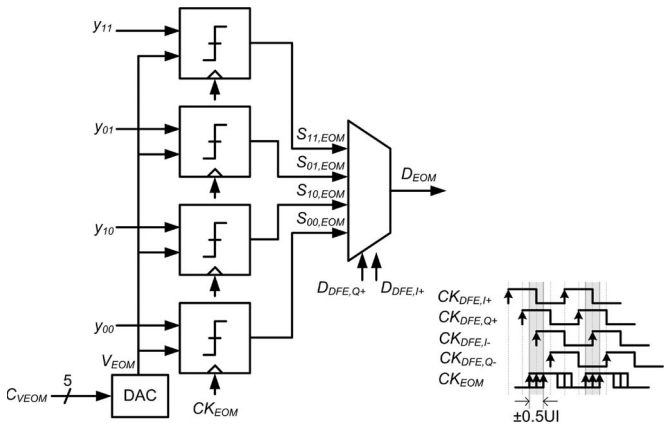

Fig. 5. Block diagram for the EOM sampler.

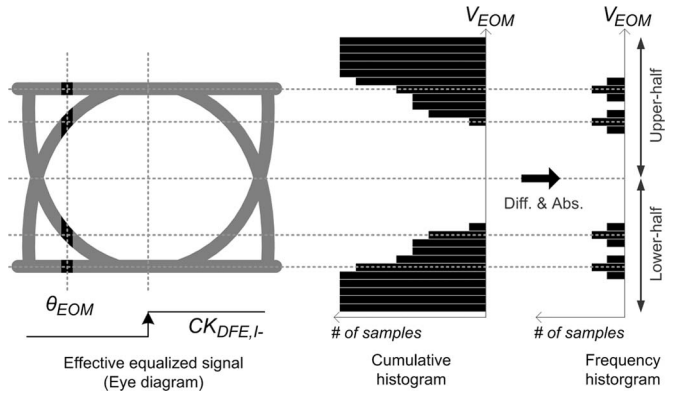

Fig. 6. Process to acquire histogram.

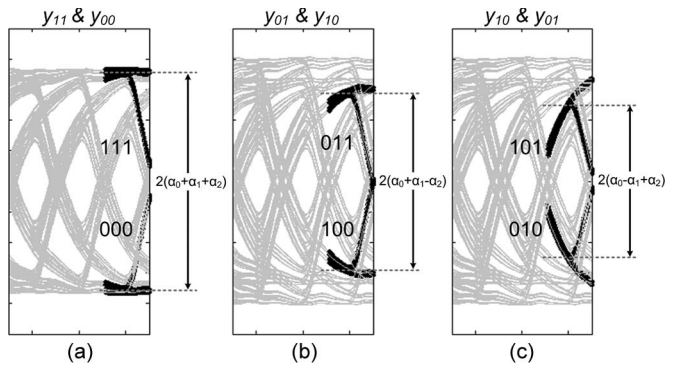

Fig. 7. ISI measurement using pattern-filtered eye diagrams.

C. Acquisition of the Histogram and the Adaptation Algorithm

The process to acquire a histogram is illustrated in Fig. 6, which is similar to that used in [15], although a synchronized clock is used in this brief instead of the asynchronous clock used in [15]. Suppose an effective equalized signal combined from candidate signals are as shown in Fig. 4. The EOM scans the candidate signals in a vertical direction with increasing $V_{\rm EOM}$ for discrete $\theta_{\rm EOM}$ in the range. At each $\theta_{\rm EOM}$, the EOM measures a full histogram by dividing the vertical range into the lower half and the upper half of $V_{\rm EOM}$. In the lower half of $V_{\rm EOM}$, the EOM monitors only the traces of symbol 0. It counts the number of 1 in $D_{\rm EOM}$ during N_S times only when the current symbol $D_{\rm DFE,I-}$ is 0. On the other hand, the number of 0 in $D_{\rm EOM}$ is counted for N_S times only when the current symbol $D_{\rm DFE,I-}$ is 1 for the upper half of $V_{\rm EOM}$. As a result, a cumulative histogram is obtained. The desired histogram can be obtained by differentiating the cumulative histogram and taking the absolute value. An eye diagram for the equalized signal can be obtained by measuring histogram values with $\theta_{\rm EOM}$ sweeping.

Since the EOM can make histograms of LADFE candidate signals, adaptation of LADFEs can be easily achieved using the zero-forcing algorithm with pattern-dependent filtering [2]. The EOM measures the amount of ISI by searching and comparing the signal levels for several data patterns. Fig. 7 shows three eye diagrams for different candidate signals with ISI. The lowest frequency component occurs when the data pattern is 111 or 000 for the case of two postcursors. If the mean value in the upper half of y_{11} is measured at the center of the eye, the channel response for the data pattern of 111 or $\alpha_0+\alpha_1+\alpha_2$ can be determined, where α_0 is the magnitude value of the main cursor and α_1 and α_2 are the magnitude values of the first and second *post*cursors, respectively. To perform this pattern filtering, the controller acquires the histogram only when the recent 3-bit pattern is 111 and then calculates the mean value of the upper level at the eye center. With the same process for the lower half of y_{00}, a differential magnitude of ISI or $2(\alpha_0+\alpha_1+\alpha_2)$ can be measured.

There are high-frequency components when data have transitions. Therefore, the EOM measures other two differential magnitude values of ISI, i.e., $2(\alpha_0+\alpha_1-\alpha_2)$ and $2(\alpha_0-\alpha_1+\alpha_2)$, and calculates each ISI component from them. Finally, it calculates DFE codes and applies them to the LADFE for adaptation.

Fig. 8 shows the schematic for the quarter of the LADFE with the EOM for a look-ahead path for the 11 pattern. An offset amplifier differentially subtracts the DFE coefficients $V_{\rm EQ11}$ and $V_{\rm EQ00}$ from the received signal $r_{+/-}$. Five branches, which consist of track-and-hold switches (T/H), clocked-sense amplifiers (CSA), and CMOS D-flipflops (DFFs) after the offset amplifier, sequentially make sampling and quantization. Each sampling element has its own clock provided from a clock tree in the clock generator. After T/H holds y_{11+} and y_{11-} at each sampling time, CSAs and DFFs make decisions on these and produce digital values. Since the sampling time is the moment when T/H begins its hold operation, it is important to match loading on all five clock signals for T/H. For this, dummy switches including two nMOS and pMOS transistors are added to $\rm CK_{EOM+,TH}$ and $\rm CK_{EOM-,TH}$.

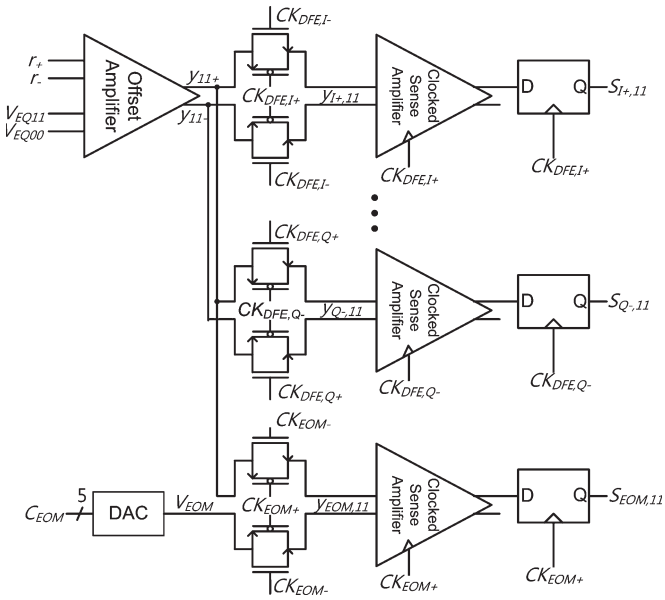

Fig. 8. Schematic of a quarter circuit of the sampling path in the LADFE with the EOM.

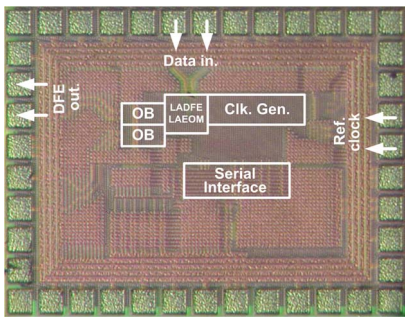

Fig. 9. Die photograph.

III. Experimental Results

A prototype chip is implemented in 90-nm CMOS technology. Fig. 9 is the photograph of the fabricated chip. The core size of the LADFE with the EOM is $110 \times 95\ \mu\text{m}^2$. For the present investigation, the EOM controller is realized in a field-programmable gate array to achieve flexibility in testing. However, this can be easily realized on chip as a synthesized digital circuit. The estimated gate count for the EOM controller is about 1500. For measurement, the die is directly mounted on a PCB and wire-bonded. The measurement setup is shown in Fig. 10.

A pattern generator transmits differential 10-Gb/s pseudo random bit sequence (PRBS) data to the chip directly or through 10-, 20-, 30-, or 40-cm FR4 PCB traces. A frequency-synchronized clock source provides a differential 2.5-GHz reference clock. One of four LADFE outputs is multiplexed and is fed back into a BER tester. The EOM controller produces eye diagrams by taking the EOM output and the data pattern from the chip. It then stores histograms for the eye diagram and delivers these to a computer, which displays the eye diagram.

Fig. 11 shows pattern-filtered eye diagrams for 10-Gb/s PRBS without any PCB channel. The horizontal and vertical axes are θ_{EOM} and C_{VEOM}, respectively. Since Fig. 11(a) is the eye diagram for patterns of 111 and 000, there is no transition

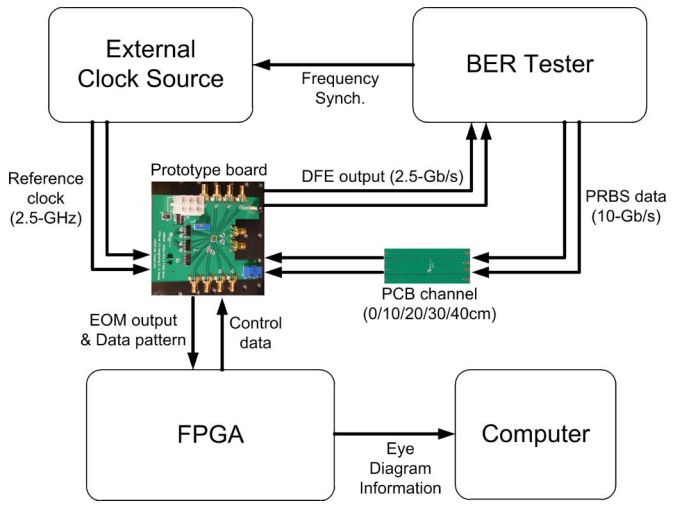

Fig. 10. Experimental setup.

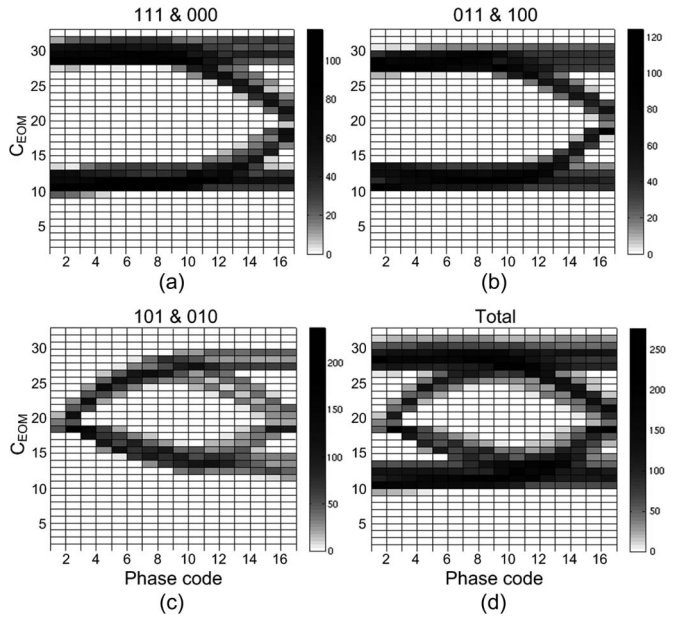

Fig. 11. Obtained eye diagrams by the EOM with pattern filtering.

from the previous bit; thus, the left side of the eye is opened. On the other hand, the eye diagram for patterns of 101 and 010 shown in Fig. 11(c) has crossings because there are always transitions from 0 to 1 or 1 to 0.

Acquired eye diagrams by the EOM and measured bathtub curves for 10-, 20-, 30-, and 40-cm PCB channels are shown in Fig. 12. The eye diagrams are obtained with all the tap weights initially set to their minimum values. Bathtub curves were measured by adjusting the position of the input data relative to the reference clock both before and after equalization. It is clear that the horizontal eye openings (HEOs) are greatly improved with our LADFE. The measured HEO is 0.2 UI at 10^{-12} BER with a 40-cm PCB channel.

Table I compares the performance of this brief with previously reported DFEs. Although the figure of merit for our LADFE is the highest, we would like to point out that other LADFEs do not include built-in adaptation capacity, which we believe is essential for many applications. In addition, ours is the only LADFE that can have a built-in EOM.

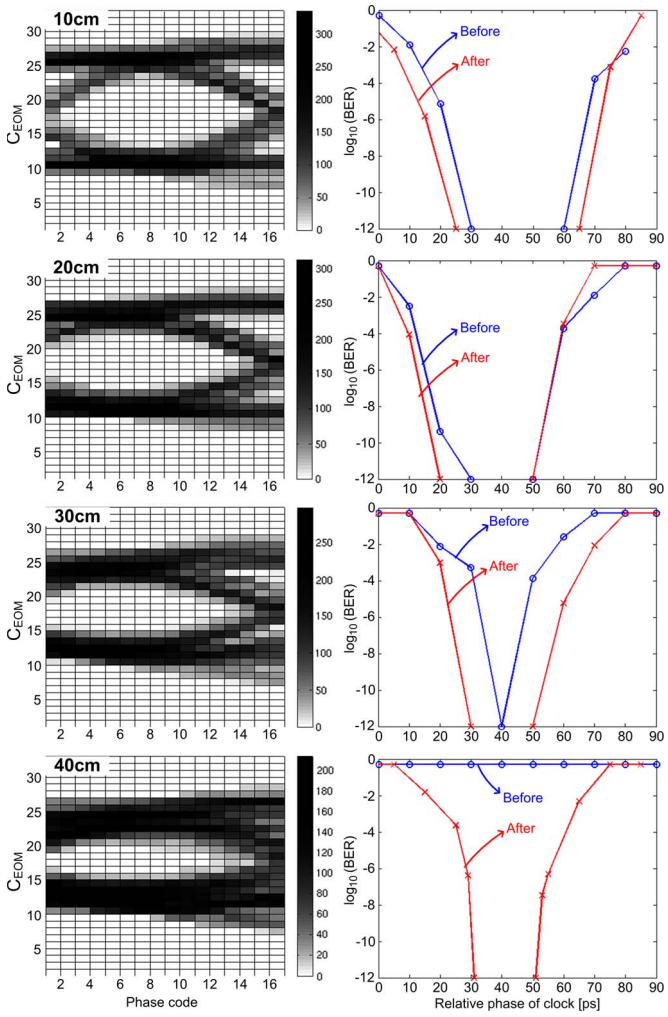

Fig. 12. (Left) Obtained eye diagrams by the proposed EOM after equalization and (right) bathtub curves before and after equalization for 10-, 20-, 30-, and 40-cm PCB traces.

TABLE I
PERFORMANCE COMPARISON WITH REPORTED CMOS LADFES

		[4]	[5]	[6]	This work
Technology		90nm	45nm	90nm	90nm
V_{DD}		1.0V	1.0V	1.0V	1.2V
Data rate		6Gb/s (PRBS31)	12Gb/s (PRBS7)	10Gb/s (PRBS31)	10Gb/s (PRBS7)
# of taps		2	5	1	2
Interleaving		4	2	4	4
Power consumption		2.88mW	11mW	6mW	11mW
Core area		4,410μm^2	10,510μm^2	3,650μm^2	10,450μm^2
Package		On-wafer	On-wafer	On-wafer	COB
Built-In Adaptation Capacity		No	No	No	Yes
EOM		No	No	No	Yes*
Performance	HEO (UI) @BER	N/A @10^{-12}	0.32 @10^{-8}	0.12 @10^{-9}	0.2 @10^{-12}
	Channel loss	6.2dB @3GHz	15dB @6GHz	6dB @5GHz	8.8dB @5GHz
	FOM[16] (pJ/bit/dB)	0.077	0.061	0.091	0.125

*EOM controller realized in FPGA

IV. CONCLUSION

A new LADFE architecture with EOM capability is demonstrated. By employing the look-ahead structure in EOM, an eye diagram can be obtained from candidate signals in the DFE. The EOM can measure the amounts of ISI induced by channels and determine DFE coefficients that are used for adaptive equalization. A prototype chip for a 10-Gb/s two-tap adaptive LADFE with an EOM is demonstrated in 90-nm CMOS technology with an external EOM controller. In experiments with PCB channels, our LADFE improves BER performance with automatic adaptation for channel lengths of 10-, 20-, 30-, and 40 cm. The LADFE and the EOM sampler occupy 110×95 μm^2 and consume 11 mW from 1.2-V supply voltage.

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