

# An 8-Gb/s Inductorless Adaptive Passive Equalizer in 0.18- $\mu\text{m}$ CMOS Technology

Joung-Wook Moon and Woo-Young Choi

**Abstract**—This paper presents an inductorless 8-Gb/s adaptive passive equalizer with low-power consumption and small chip area. The equalizer has a tunable RC filter which provides high-frequency gain boosting and a limiting amplifier that restores the signal level from the filter output. It also includes a feedback loop which automatically adjusts the filter gain for the optimal frequency response. The equalizer fabricated in 0.18- $\mu\text{m}$  CMOS technology can successfully equalize 8-Gb/s data transmitted through up to 50-cm FR4 PCB channels. It consumes 6.75 mW from 1.8-V supply voltage and occupies 0.021 mm<sup>2</sup> of chip area.

**Index Terms**—Adaptive equalizer, CMOS, inductorless, passive filter, power efficient

## I. INTRODUCTION

As data transmission speed for various electronic applications increases, inter-symbol interference (ISI) caused by frequency-dependant channel loss becomes more severe. In order to overcome this, various types of high-speed equalizers have been reported [1-3], [7-10]. In particular, equalizers having passive filters based on RLC components are attractive as their power consumption is much less than those with active filters [1-3]. Furthermore, an efficient scheme for filter frequency repose adaptation is required so that the equalizer can be used for various channel environments

even with unavoidable process-voltage-temperature (PVT) variations [3-5]. Especially, Shin *et al.* demonstrated an equalizer having a tunable passive filter whose frequency response is adaptively adjusted by comparing the low-frequency power with the total power [3]. However, their equalizer did not monolithically include a limiting amplifier, which plays a vital role for the passive adaptive equalizer by restoring the signal level attenuated by the passive filter.

In this paper, we report an inductorless low-power adaptive passive equalizer including a limiting amplifier and output driver realized in 0.18- $\mu\text{m}$  CMOS technology. Our equalizer has a very small power consumption of 6.75 mW and occupies only 0.021 mm<sup>2</sup> of chip area. It can successfully equalize up to 8-Gb/s data transmitted through from 20-cm to 50-cm FR4 PCB traces.

This paper is organized as follows. Section II presents the architecture of our equalizer as well as target channel characteristics of this work. Section III shows details of building blocks for the equalizer. Section IV presents the measurement results, and Section V gives the conclusion.

## II. SYSTEM DESIGN

### 1. System Architecture

Fig. 1 shows the simplified block diagram of our equalizer. A tunable passive filter performs channel equalization and a limiting amplifier restores the signal level. Equalization adaption is achieved by the self-power comparison method [4]. The power detector detects signal powers passed through low-pass filter (LPF) and high-pass filter (HPF), and the detected

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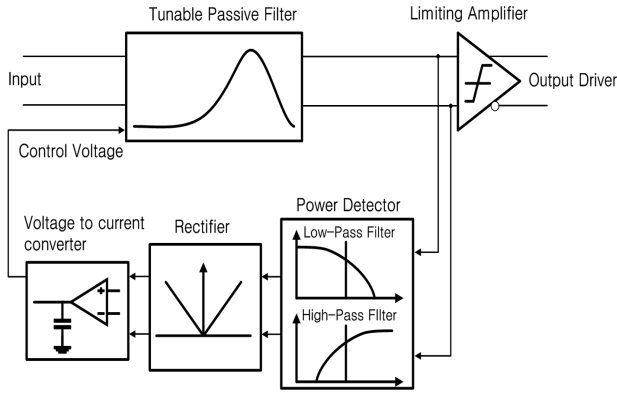


Fig. 1. Equalizer architecture.

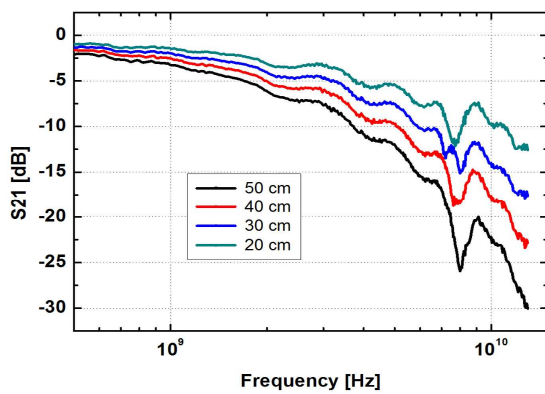


Fig. 2. Measured response for various channels.

powers go through a rectifier, output of which, after voltage-to-current (V/I) conversion, controls the filter characteristics for the optimal equalization. The goal of our research is realizing a small power-efficient passive filter for the adaptive equalizer application. The adaptive algorithm and the adaptive blocks in our equalizer are from Ref. [4].

2. Channel Characteristics

For optimal filter design, it is necessary to quantify the channel characteristics. Fig. 2 shows measured  $S_{21}$  characteristics of FR4 PCB channels having various lengths. From these, the required boosting gain for the target data rate can be determined. For example, 8-Gb/s data transmission, our design target, needs about 5-dB boosting at 4 GHz for 20-cm channel and 10-dB boosting for 50-cm channel as can be determined from Fig. 2.

III. BUILDING BLOCKS

1. Passive Filter

Most passive filters for high-speed equalizers use inductors because they effectively boost high frequency gain without attenuating DC gain. However, since on-chip inductors require a large chip area, we pursued our design without using any inductors for the goal of achieving as compact an equalizer as possible.

Fig. 3 shows the schematic of our inductorless tunable passive filter, where PMOS  $M_1$  is used as a variable resistance for controlling filter gain.

The filter transfer function is given as

$$A_v = \frac{s \left( R_M + \frac{R}{2} \right) + \frac{R_M}{2RC}}{s \left( R_M + \frac{R}{2} \right) + \frac{1}{C} \left( \frac{R}{2Z_L} + \frac{R_M}{Z_L} + \frac{R_M}{2R} + \frac{1}{2} \right)}, \quad (1)$$

where  $R_M$  is variable resistance of PMOS  $M_1$ , and  $Z_L$  is load impedance on output node due to the power detector and the limiting amplifier, which changes with the frequency. Fig. 4 shows the simulated frequency responses of  $Z_L$  as well as the passive filter with the control voltage changing from 0 to 0.8 V. For simulation, PMOS with 200- $\mu\text{m}$  width and 0.18- $\mu\text{m}$  length is used for  $M_1$  and  $R=80 \Omega$ ,  $C=680 \text{ fF}$ . The resulting filter characteristics provide the necessary gain range required for 8-Gb/s data transmission through up to 50-cm FR4 channel, satisfying our design target.

The measure  $S_{11}$  value for our passive filter is varying from -5.61 dB to -6.16 dB at 4 GHz by varying the control voltage from 0 V to 1.0 V when measured from

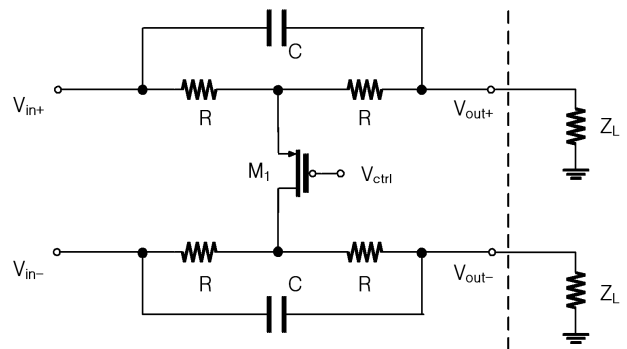
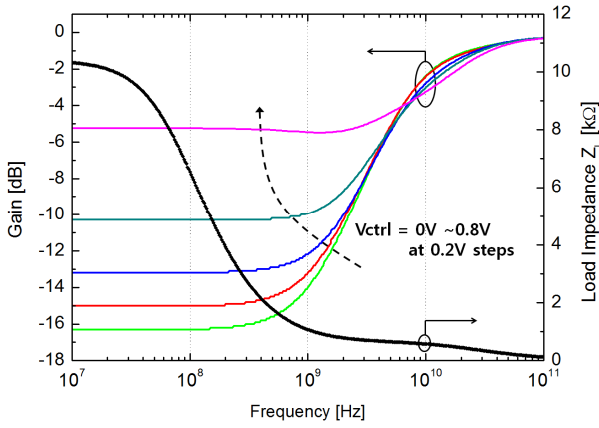


Fig. 3. Inductorless tunable passive filter.



**Fig. 4.** Simulated frequency responses of passive equalization filter and load impedance.

nominally 50 ohm FR4 channels. This is due to impedance mismatch caused by a large R value used in our filter.

**2. Power Detector**

Passive filters suffer from their small output swing. Consequently, we need a power detector with high sensitivity and reasonable output voltage swing while suppressed power consumption. Since the conventional common-source type differential pair does not provide enough output swing, we design the power detector with the current steering technique reported in [4].

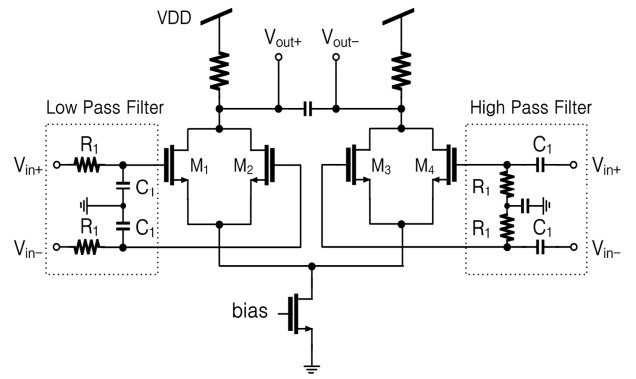
The power detector compares low and high frequency components of filter output using two different first-order RC filters. For normalized random binary data, the half power frequency can be derived as [4]

$$2\pi f_m = \frac{1}{R_1 C_1} = 2\pi \times 0.28 \times \frac{1}{T_b}, \quad (2)$$

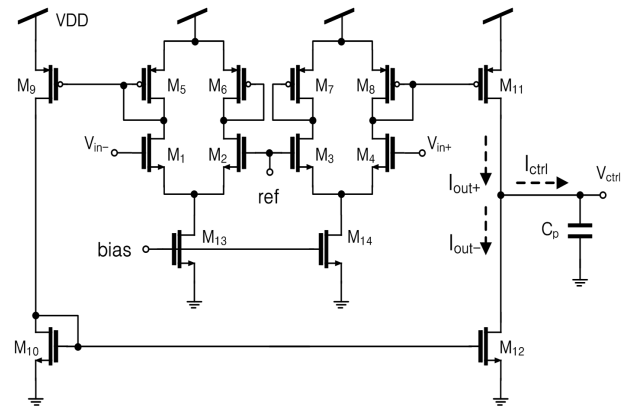
and

$$f_m = \frac{0.28}{T_b}, \quad (3)$$

where  $f_m$  is the frequency that splits the spectrum into equal powers, and  $T_b$  is the bit period of the data stream. From Eq. (2), we can determine the required  $R_1 C_1$  value is 71 ps for 8-Gb/s input data. The schematic for the power detector is shown in Fig. 5, which is based on two differential pairs with tied drains.



**Fig. 5.** Power detector.



**Fig. 6.** Voltage-current converter.

frequency components are produced by LPF and HPF, respectively, and their power difference are converted to the output voltage.

**3. V/I Converter**

An error amplifier based on two differential pairs is used as a voltage-current converter as shown in Fig. 6. Due to the current source  $M_{13}$  and  $M_{14}$  tie with a same bias voltage, the small input differential swing offer proportional to the output current.

$$I_{ctrl} = I_{out+} - I_{out-} = \alpha \cdot (V_{in+} - V_{in-}). \quad (4)$$

By charging and discharging the output dangling capacitor,  $C_p$ , the passive equalization filter obtains proper control voltage for the filter gain,  $V_{ctrl}$ .

**4. Limiting Amplifier and Output Driver**

It is essential for the limiting amplifier to boost up the

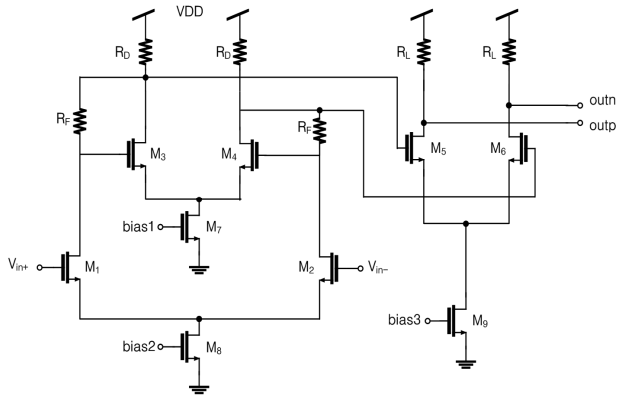


Fig. 7. Limiting amplifier and 1stage CML buffer.

signal attenuated by the passive filter. This is because passive equalizers realize equalization by selectively reducing low-frequency signals, which results in too small signal to be processed in the next block. A conventional differential Cherry-Hooper amplifier with a current source load is used for the limiting amplifier as shown in Fig. 7. In order to minimize power consumption and the size, we designed the limiting amplifier to have the minimum required gain of 8.5dB with effective bandwidth of 3.8 GHz.

To accomplish 50-Ω output termination, a four-stage current-mode logic (CML) output driver is implemented next to the limiting amplifier. It provides output swing up to 200 mV<sub>p-p</sub>.

IV. MEASUREMENT RESULTS

Fig. 8 shows the die photography of the equalizer fabricated in 0.18-μm CMOS technology. The chip area is about 115 μm by 190 μm. Measurement was done on a high-speed probe station. 2<sup>31</sup>-1 PRBS patterns from a pattern generator were delivered into from 20-cm to 50-cm long FR4 PCB traces. Their outputs were connected to the fabricated equalizer and the equalizer output was measured by an oscilloscope and a bit-error-rate (BER) tester.

Fig. 9(a), (b), (c), and (d) show the measured eye-diagrams before (left) and after (right) equalization for 20-cm, 30-cm, 40-cm, and 50-cm FR4 PCB trace at 8 Gb/s, respectively. The equalizer guarantees at least 100-mV of eye opening and successfully achieves the error-free condition (BER < 10<sup>-13</sup>) at all channel lengths.

We performed additional measurements in which

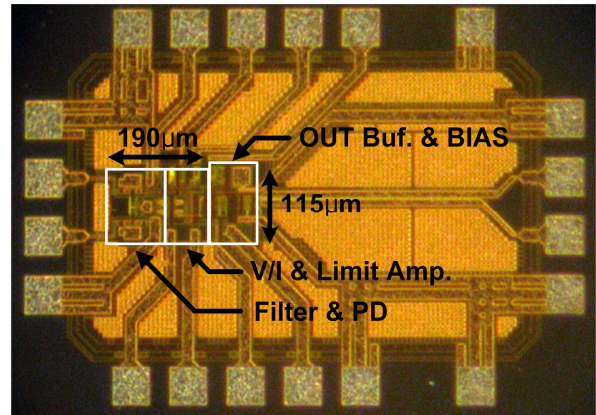


Fig. 8. Chip photography.

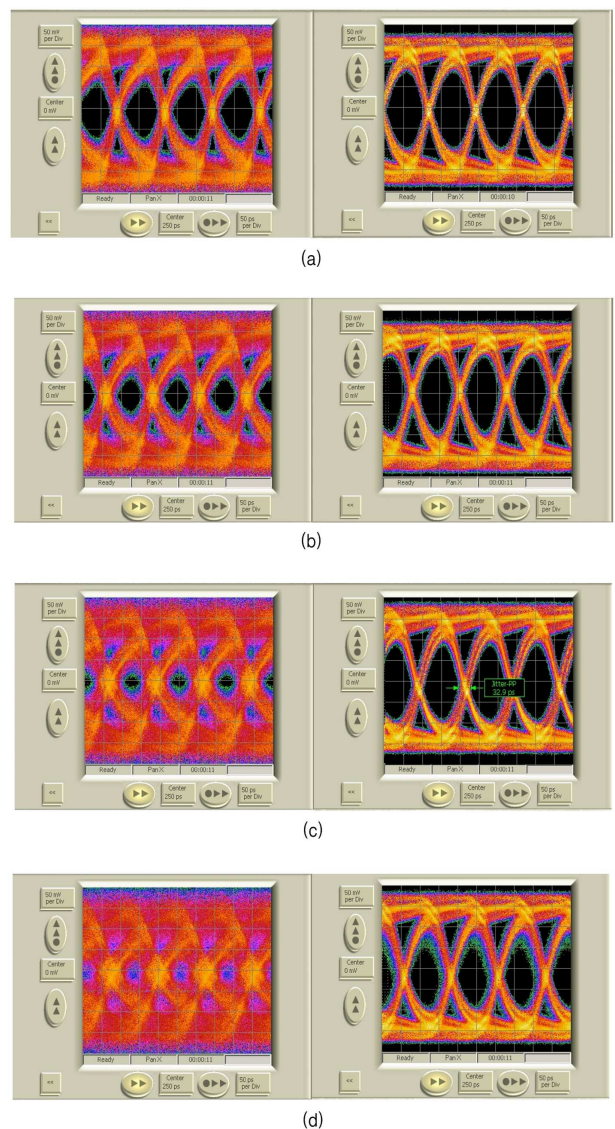


Fig. 9. Measured waveform before (left) and after (right) equalization at 8 Gb/s of (a) 20-cm FR4 PCB trace, (b) 30-cm FR4 PCB trace, (c) 40-cm FR4 PCB trace, (d) 50-cm FR4 PCB trace.

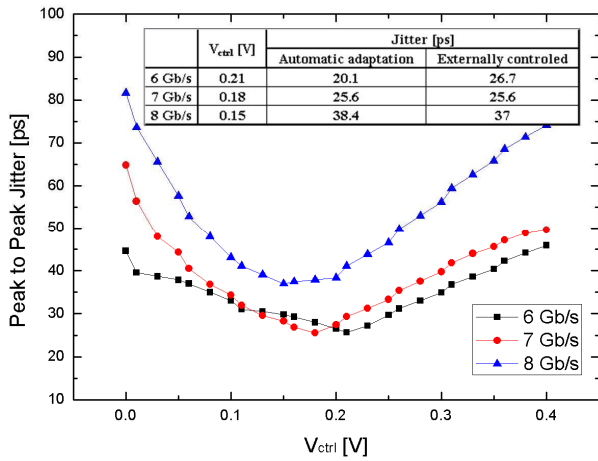


Fig. 10. Measured jitter vs. V<sub>ctrl</sub> at several data rates with 40-cm channel.

peak-to-peak jitter characteristics of equalized 6-Gb/s, 7-Gb/s, and 8-Gb/s PRBS data through 40 cm FR4 channel are measured with different filter control voltages that are externally provided. The results are shown in Fig. 10. The control voltages that produce the minimum jitter values are the values our equalizer should achieve automatically. This can be confirmed from the table shown inside the figure in which the minimum jitter values determined for each data rate in Fig. 10 are compared with the measured jitter values from the equalized data with the adaptive operation our equalizer without any external control. As can be seen in the table, the adaptive equalization achieves the minimum jitter value, confirming our adaptive equalizer functions properly. With the increasing data rates, the optimal control voltage becomes smaller, which provides higher boosting gain.

Excluding the output driver, the equalizer consumes 6.75 mW, of which the adaptation block consumes 4.5

mW and the limiting amplifier 2.25 mW from a 1.8-V supply voltage. In addition, the chip occupies only 0.021 mm<sup>2</sup> excluding the output drivers.

The measured performance is summarized in Table 1 with recently published equalizers. Our equalizer achieves very small power per rate of 0.84 mW/Gbps even though it is fabricated with the least advanced technology. The power consumption and the chip area for our design can be further reduced with more advanced technology.

Although the passive equalizer reported in [3] shows the best performance, it should be noted that it does not include a limiting amplifier which consume a fair amount of power and chip area.

### V. CONCLUSIONS

In this paper, a power-efficient equalizer having an inductorless RC passive filter and an adaptive feedback loop scheme is realized. The tunable passive filter shows a maximum gain boosting of 10 dB at 4 GHz without consuming any power consumption, and the feedback loop adaptively controls the filter characteristics for optimal equalization. The equalizer has 0.84 mW/Gbps of power efficiency and 0.021 mm<sup>2</sup> of die size in 0.18-μm CMOS technology.

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Table 1. Performance comparison

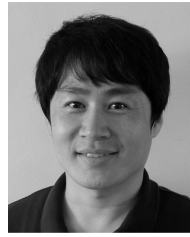
	[2]	[3]	[4]	[5]	[6]	This work
Technology	180-nm CMOS	90-nm CMOS	130-nm CMOS	130-nm CMOS	90-nm CMOS	180-nm CMOS
EQ. Type	Passive	Passive	Active	Passive	Active (*)	Passive
Data Rate	10 Gb/s	12 Gb/s	20 Gb/s	10 Gb/s	7 Gb/s	8 Gb/s
Boosting Gain	16.7 dB @ 5 GHz	13 dB @ 6 GHz	15~20 dB @10 GHz	20 dB @ 5 GHz	15 dB @ 3.5 GHz	10 dB @ 4 GHz
BER	10 <sup>-12</sup>	10 <sup>-10</sup>	10 <sup>-15</sup>	10 <sup>-15</sup>	10 <sup>-13</sup>	< 10 <sup>-13</sup>
Supply Voltage	1.8 V	1.0 V	1.5 V	1.2 V	1.0 V	1.8 V
Power Dissipation	34.2 mW	1 mW (**)	60 mW	25 mW	9.3 mW	6.75 mW
Power Efficiency	3.4 mW/Gbps	0.08 mW/Gbps	3 mW/Gbps	2.5 mW/Gbps	1.32 mW/Gbps	0.84 mW/Gbps
Area	0.110 mm <sup>2</sup>	0.034 mm <sup>2</sup> (**)	0.200 mm <sup>2</sup>	0.162 mm <sup>2</sup>	0.018 mm <sup>2</sup>	0.021 mm <sup>2</sup>

(\*) DFE equalizer without adaptation

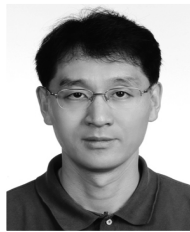
(\*\*) Power & Area without LA

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