Effects of Guard-Ring Structures on the Performance of Silicon Avalanche Photodetectors Fabricated With Standard CMOS Technology

Myung-Jae Lee, *Student Member, IEEE*, Holger Rücker, and Woo-Young Choi, *Member, IEEE*

***Abstract*—We investigate the effects of guard-ring (GR) structures on the performance of silicon avalanche photodetectors (APDs) fabricated with the standard complementary metal–oxide-semiconductor (CMOS) technology. Four types of CMOS-compatible APDs (CMOS-APDs) based on the p$^+$/n-well junction with different GR structures are fabricated, and their electric-field profiles are simulated and analyzed. Current characteristics, responsivity, avalanche gain, and photodetection bandwidth for CMOS-APDs are measured and compared. It is demonstrated that the GR realized with shallow trench isolation provides the best CMOS-APD performance.**

***Index Terms*—Avalanche photodetector (APD), avalanche photodiode, edge breakdown, guard ring, optical interconnect, shallow trench isolation (STI), silicon photonics, standard complementary metal–oxide-semiconductor (CMOS) technology.**

I. Introduction

RECENTLY, there have been growing interests in 850-nm optical communication and interconnect applications for optical access networks and high-speed data links [1], [2]. For these applications, cost-effective realization of optical components and transmission media is very important, and vertical-cavity surface-emitting lasers and multimode fibers are often used since they are cost effective and easy to employ [1], [3]. Photodetectors fabricated with the standard complementary metal-oxide-semiconductor (CMOS) technology are attractive as they can reduce the fabrication cost and provide the possibility of monolithic integration of photodetectors and electronic circuits [4]. Recently, their photodetection performance has been greatly enhanced with CMOS-compatible avalanche photodetectors (APDs) (CMOS-APDs) [5], [6].

APDs, however, can suffer from premature breakdown due to locally concentrated electric fields at the junction edges [7]–[9]. In order to achieve the best performance, CMOS-APDs should have a structure in which the high electric fields are uniformly spread over the planar junction. For this, guard-ring (GR) structures are often used. Although there are several GR structures available for CMOS-APDs, there have been no comparative studies on various GR structures.

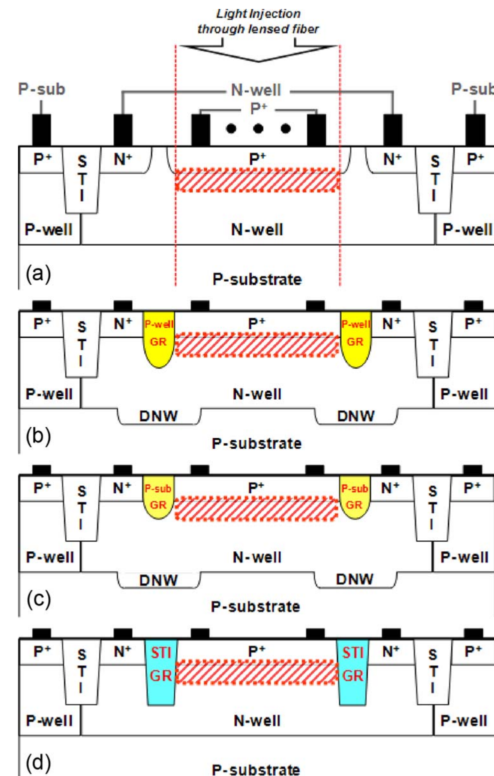

Fig. 1. Cross sections of CMOS-APDs. (a) Without GR, (b) with p-well GR, (c) with p-sub GR, and (d) with STI GR.

In this letter, we report the results of our investigation on the influence of various GR structures on CMOS-APD performances. Four types of CMOS-APDs based on the p$^+$/n-well junction having different types of GR structures were fabricated, and their electric-field profiles were analyzed with simulation. In addition, such performance parameters as current characteristics, responsivity, avalanche gain, and photodetection bandwidth were measured and analyzed to identify the optimal GR structure for the CMOS-APD.

II. Device Structures and Simulation Results

Fig. 1 shows the cross sections of four types of CMOS-APDs fabricated with 0.25-μm BiCMOS technology [10]. Although the technology offers both bipolar and CMOS devices, our

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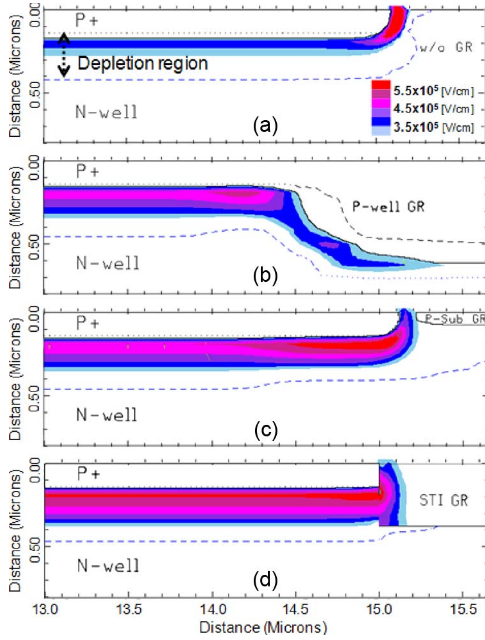

Fig. 2. Simulated electric-field profiles for CMOS-APDs. (a) Without GR, (b) with p-well GR, (c) with p-sub GR, and (d) with STI GR.

APDs are fabricated with CMOS processing steps only. Triple wells, including deep n-well (DNW), are available. All four types of CMOS-APDs are based on the p^+/n-well junction, which has been demonstrated to provide high photodetection bandwidth [5]. 10×10 μm^2 optical windows are formed by blocking the salicide process. No design rule is violated for realizing these CMOS-APDs.

The CMOS-APD shown in Fig. 1(a) has no GR. GRs between the CMOS-APD area and the n^+ contacting area can be formed by p-doped regions [Fig. 1(b) and (c)] or by shallow trench isolation (STI) [Fig. 1(d)]. In standard CMOS technology, p-type GRs can be formed by p-wells [Fig. 1(b)] or by p-substrate (p-sub) areas with blocked p-well and n-well [Fig. 1(c)]. DNW regions are utilized to isolate GRs from p-sub and to connect n-wells in the diode and contact regions. The width of the p-well and p-sub GRs is 1.5 μm according to the CMOS design rules. The width of STI GR is 0.7 μm.

We performed device simulation with MEDICI to investigate the influence of GRs on the electric-field profiles for CMOS-APDs in reverse bias. For the simulation, doping profiles for the 0.25-μm BiCMOS technology were provided by IHP [10]. The doping concentration of p-sub is about 10^{15} cm^{-3}. The p-well and n-well doping ranges from 10^{17} cm^{-3} in the space charge region to about 5×10^{17} cm^{-3} near the surface and at a depth of 0.7 μm. The p^+/n-well junction depth is about 0.2 μm. Fig. 2 shows the simulated electric-field profiles when CMOS-APDs are reverse biased about 0.1 V below their breakdown conditions. As shown in Fig. 2(a), without any GR, the electric fields are much stronger around the edge of the junction than at the planar junction. In APD applications, the uniform and high electric-field profile is desired so that large avalanche gain can be obtained in a large area before the avalanche breakdown occurs. With the field profile shown in Fig. 2(a), the avalanche breakdown occurs at the junction edge, preventing photogenerated carriers to experience sufficient avalanche gain.

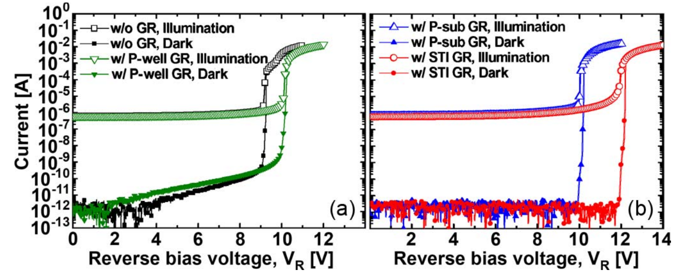

Fig. 3. Current–voltage characteristics of CMOS-APDs: (a) Without GR and with p-well GR, (b) with p-sub GR, and with STI GR.

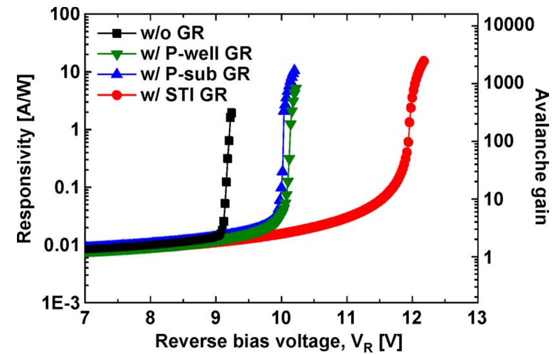

Fig. 4. Measured responsivity and avalanche gain for CMOS-APDs.

With GRs, this premature edge breakdown is alleviated, as shown in Fig. 2(b)–(d). The maximum electric field at the planar junction increases from 3.9×10^5 V/cm for the device without GR to about 5×10^5 V/cm with p-well or p-sub GR and 5.7×10^5 V/cm with STI GR.

III. Experimental Results and Discussions

For photodetection characterizations, an 850-nm laser diode was used as an optical source, and a circular lensed fiber with 10-μm spot diameter was used for injecting light into CMOS-APDs on wafer. For dc measurements, 0.1 mW of light measured at the lensed-fiber output was used. Fig. 3 shows the measured current–voltage characteristics of CMOS-APDs under illumination and dark conditions. Dark currents are below the detection limit of about 5 pA for CMOS-APDs with p-sub GR and STI GR [Fig. 3(b)]. CMOS-APDs without GR and with p-well GR show enhanced dark currents [Fig. 3(a)] due to tunneling at the edges of p^+ regions in n-well and n^+ regions in p-well, respectively. These currents disappear when p^+ and n^+ regions are surrounded by lightly doped p-sub or STI. All CMOS-APDs exhibit low dark currents below a few nanoamperes before avalanche breakdown. The avalanche breakdown voltage is defined as the voltage at which the dark current reaches 10 μA. Without GR, the avalanche breakdown voltage is about 9.25 V. However, the breakdown voltages increase to about 10.2 V for p-well and p-sub GRs and to 12.2 V for STI GR. This confirms the simulation results in which STI GR allows the highest electric field before breakdown, resulting in larger maximum gain, as shown in Fig. 4. The maximum gain is about 2500 with corresponding responsivity of about

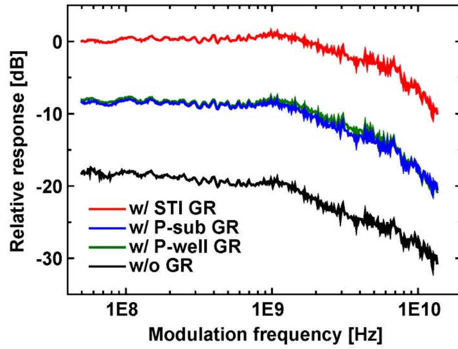

Fig. 5. Measured photodetection frequency responses of CMOS-APDs.

TABLE I
AVALANCHE GAIN: CALCULATION AND MEASUREMENT

	W [cm]	E_M [V/cm]	$\alpha_{eff}(E_M)$ [cm^{-1}]	M_{ratio}	$M_{ratio,DC}$*	$M_{ratio,AC}$**
w/o GR	0.29×10^{-4}	3.9×10^5	2×10^4	1	1	1
P-well GR	0.30×10^{-4}	5×10^5	5×10^4	2.86	3.13	3.16
P-sub GR	0.30×10^{-4}	5×10^5	5×10^4	2.86	3.13	3.16
STI GR	0.33×10^{-4}	5.7×10^5	5.5×10^4	7.71	7.88	7.94

*Determined from measured gain characteristics shown in Fig. 4.
**Determined from frequency responses shown in Fig. 5. (Factor of two correction made as Fig. 5 shows power measurement results.)

15.4 A/W for the device with STI GR, while it is about 300 with about 1.9-A/W responsivity for the device without GR.

Fig. 5 shows the normalized photodetection frequency responses of CMOS-APDs at the bias voltage of about 0.1 V below breakdown. For this measurement, an electro-optical modulator and a vector network analyzer were used with prior calibration of cables and RF adaptors. The average optical power injected into photodetectors was 1 mW, and the measured frequency range was from 50 MHz to 13.5 GHz. As shown in our previous works, slight peaking in the response is observed because of the inductive component produced in the avalanche regime [5], [11]. The photodetection bandwidths for all CMOS-APDs are similar because all four devices are based on the same junction structure. CMOS-APDs with p-well and p-sub GR structures have no appreciable difference in the photodetection frequency response and have about 10 dB higher response than the one without GR. The CMOS-APD with STI GR has about 18 dB higher response than the device without GR structures.

The avalanche gain M in an APD can be roughly estimated using $M = [1 - (1/2) \cdot W \cdot \alpha_{\text{eff}}(E_M)]^{-1}$ [12], where W is the depletion width, E_M is the maximum electric field, and $\alpha_{\text{eff}}(E_M)$ is the effective ionization rate at the maximum electric field. Using the aforementioned equation with W and E_M determined from the simulation and $\alpha_{\text{eff}}(E_M)$ from [9], the ratio of M between different types of CMOS-APDs can be estimated at the bias voltage of about 0.1 V below breakdown, as shown in Table I. For the structure without GR, the simulated value of E_M at the planar junction region is used for this estimation rather than at the corner of p^+ implantation where the electric field is higher. This is because the corner region is located outside the focused beam spot when light is injected through the lensed fiber and most photogenerated carriers are generated in the planar junction region. Here, we normalized M to its respective values for the CMOS-APDs without GR in order to cancel out uncertainties due to the used approximate expression for M. The obtained results agree well with the measurement results, as shown in Table I. The results show that different GR structures produce different electric-field magnitudes that the photogenerated carriers experience, which, in turn, influence the achievable avalanche gain. Clearly, STI provides the optimum GR structure with the largest avalanche gain in standard CMOS technology.

IV. CONCLUSION

We have investigated the effects of GR structures on the performance of CMOS-APDs. Four types of CMOS-APDs based on the p^+/n-well junction with different GR structures realized in standard CMOS technology are compared and analyzed. It is demonstrated that the device with STI GR can provide the largest electric field at the planar junction and consequently provides the maximum avalanche gain.

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