On-Chip Compensation of Ring VCO Oscillation Frequency Changes Due to Supply Noise and Process Variation

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***Abstract*—A novel circuit technique that stabilizes the oscillation frequency of a ring-type voltage-controlled oscillator (RVCO) is demonstrated. The technique uses on-chip bias-current and voltage-swing controllers, which compensate RVCO oscillation frequency changes caused by supply noise and process variation. A prototype phase-locked loop (PLL) having the RVCO with the compensation circuit is fabricated with 0.13-μm CMOS technology. At the operating frequency of 4 GHz, the measured PLL rms jitter improves from 20.11 to 5.78 ps with 4-MHz RVCO supply noise. Simulation results show that the oscillation frequency difference between FF and SS corner is reduced from 63% to 6% of the NN corner oscillation frequency.**

***Index Terms*—Phase-locked loop (PLL), process variation, supply voltage sensitivity, voltage-controlled oscillator (VCO).**

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used for on-chip clock generation for many electronic circuits and systems. For many of these applications, low-jitter clock signals are highly desirable. For this, it is essential to realize low-noise voltage-controlled oscillators (VCOs) because the VCO is the most noise-sensitive block in PLL.

Although LC VCOs can be used for low-jitter PLLs, they suffer from the limited tuning range and the large chip area. Ring VCOs (RVCOs), on the other hand, have many advantages such as easy integration, wide tuning range, and multiphase clock generation capability. Consequently, except for applications that require ultralow jitter performance, RVCOs are widely used. However, RVCOs suffer from poor phase-noise performance because their oscillation characteristics are sensitive to supply noise and process variation [1], [2].

To suppress RVCO frequency change with supply noise, voltage regulators are often used [3], [4]. However, they need large capacitance to maintain their feedback stability and large power transistors for low supply-voltage dropout. Moreover, reduced voltage swing with supply voltage scaling down in advanced technologies makes PLLs with a supply voltage regulator difficult to design. Consequently, other types of supply noise rejection techniques have been actively pursued. In [5] and [6], RVCO delay cells are modified for supply noise rejection. The resulting RVCO has good supply noise rejection performance, but its design complexity is high, and the resulting waveform is unfavorable [6]. AC coupling supply and control voltages with a capacitor can compensate supply noise [7], but this requires very careful design and layout. Digital calibration techniques are also used to compensate supply noise [8]–[10]. However, they require complex and large digital controllers.

This brief introduces a new circuit technique for reducing RVCO oscillation frequency changes that are due to supply noise and process variation. We have previously reported the results of our initial investigation in [11]. This brief is an extended version in which PLL measurement results are reported as well as simulated results for our technique against process variation.

II. Proposed Compensation Technique

The RVCO oscillation frequency with fully differential delay cells can be expressed as

$$f_{\rm osc} = \frac{I_{\rm bias}}{N \cdot C_{\rm tot} \cdot V_{\rm swing}} \tag{1}$$

where $I_{\rm bias}$ is the bias current for each delay cell, N is the number of delay cells, $C_{\rm tot}$ is load capacitance for a delay cell, and $V_{\rm swing}$ is RVCO voltage swing. Supply noise and process variation can affect $V_{\rm swing}$, $I_{\rm bias}$, and $C_{\rm tot}$. Their influence on RVCO oscillation frequency can be compensated if we first detect supply noise and process variation and change $V_{\rm swing}$, $I_{\rm bias}$, and $C_{\rm tot}$ in the right amount. Since $C_{\rm tot}$ is difficult to change and least affected by supply noise and process variation, we attempt to control $V_{\rm swing}$ and $I_{\rm bias}$ for our compensation technique.

Fig. 1 schematically shows the architecture of our RVCO made up of fully differential delay cells with bias-current and voltage-swing controllers. The controllers try to maintain a constant value for $I_{\rm bias}/V_{\rm swing}$ in order to stabilize RVCO oscillation frequency against supply noise and process variation. For this, we take a design approach in which the bias-current controller maintains $I_{\rm bias}$ as constant as possible but with unavoidable changes due to various nonideal factors, and the voltage-swing controller produces $V_{\rm swing}$ with which $I_{\rm bias}/V_{\rm swing}$ can be maintained constant.

Manuscript received July 20, 2011; revised October 11, 2011; accepted November 24, 2011. Date of publication January 27, 2012; date of current version February 23, 2012. This work was supported by the IT R&D program of MKE/KEIT [10034834]. This paper was recommended by Associate Editor H. C. Huat.

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Digital Object Identifier 10.1109/TCSII.2011.2180092

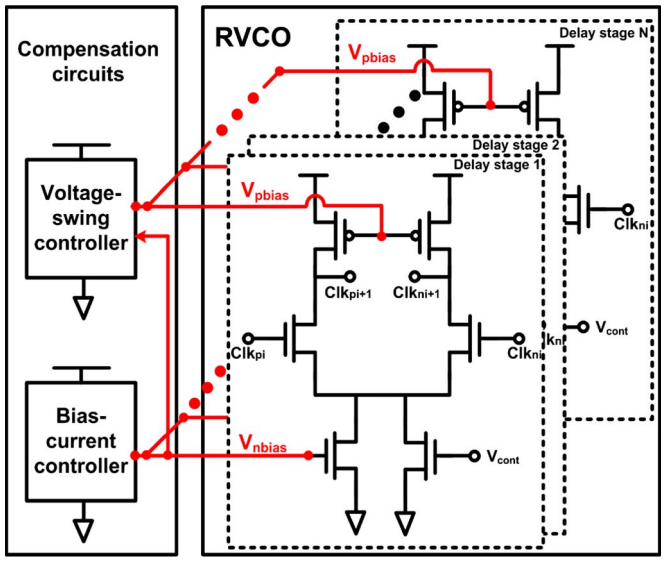

Fig. 1. Overall structure of the proposed RVCO.

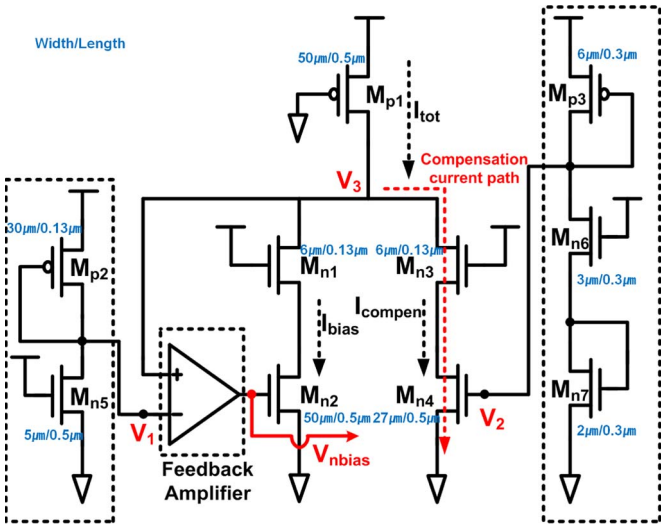

Fig. 2. Bias-current controller circuit topology.

A. Bias-Current Controller

Fig. 2 shows the schematic of the bias-current controller. It is composed of a feedback amplifier, a compensation current path, and two voltage generators—one for feedback amplifier reference voltage (V_1) and the other for compensation voltage (V_2). Because M_{n1} and M_{n2} are the replica of the delay cell, $I_{\rm bias}$ is copied as delay cell bias currents.

When the supply voltage increases, for example, $I_{\rm tot}$ increases because V_{sg} and V_{sd} of M_{p1} increase. At the same time, V_1 goes up because it is proportional to V_{DD}, as shown below

$$V_1 \approx (V_{DD} - |V_{\rm th}|) \quad \text{if} \quad C_{Mp2} \gg C_{Mn5} \tag{2}$$

where $C_i = k_i(W_i/L_i)$. With this, V_3 also goes up because the feedback amplifier controls $V_{n\rm bias}$ in order to maintain V_3 equal to V_1. This can reduce variation in $I_{\rm tot}$ caused by channel length modulation of M_{p1}. In addition, $I_{\rm compen}$ in the compensation

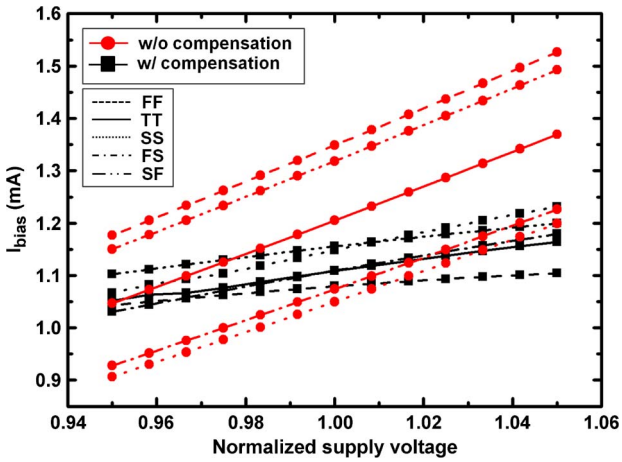

Fig. 3. Simulation results of bias-current variation due to supply noise (±5%) in each process variation.

current path goes up because V_2 is also proportional to V_{DD}, as shown below

$$V_2 = \left\{1 - \sqrt{\frac{C_{Mn7}}{C_{Mp3}}}\left(\sqrt{\frac{C_{Mn6}}{C_{Mn6}+C_{Mn7}}}\right)\right\} V_{DD} - \left\{1 - \sqrt{\frac{C_{Mn7}}{C_{Mp3}}} - \sqrt{\frac{C_{Mn7}}{C_{Mp3}}}\left(\sqrt{\frac{C_{Mn6}-C_{Mn7}}{C_{Mn6}+C_{Mn7}}}\right)\right\} V_{\rm th} \tag{3}$$

since $I_{\rm bias}$ is the difference between $I_{\rm tot}$ and $I_{\rm compen}$, $I_{\rm bias}$ does not change much even if $I_{\rm tot}$ is increased by supply noise.

The bias-current controller operates in a similar manner for process variation. When the controller is in FF corner, for example, $I_{\rm tot}$ increases because $V_{\rm th}$ of M_{p1} is smaller. However, V_1 and V_2 go up because $V_{\rm th}$ is smaller, as can be seen from (2) and (3). Then, variation in $I_{\rm tot}$ is reduced, and $I_{\rm compen}$ increases.

The amount of change in $I_{\rm compen}$ plays a critical role in compensating supply noise and process variation for $I_{\rm bias}$. Because the amount of change is determined by the size of M_{n4}, we can achieve the optimum compensation by adjusting M_{n4} size. However, this causes changes in VCO oscillation frequency, which we correct by adjusting the transistor size for the differential pair in VCO delay cells.

Fig. 3 shows how $I_{\rm bias}$ changes with supply voltage in various process corners by simulation. For the simulation, 0.13-μm CMOS process parameters with nominal supply voltage of 1.2 V are used. Without the compensation circuit, $I_{\rm bias}$ changes more than 300 μA when the supply voltage changes from -5% to $+5\%$ of the nominal value in every process corner. On the other hand, with the bias-current controller, supply voltage dependence is greatly reduced in every process corner. The simulation results also show a compensation for $I_{\rm bias}$ variation due to process variation. $I_{\rm bias}$ difference between FF and SS corners at 1.0 normalized supply voltage is reduced from 300 to 70 μA.

As shown in the figure, the slope of $I_{\rm bias}$ with compensation circuit versus supply voltage shows process-corner dependence. This is because $I_{\rm compen}$ change for compensating $I_{\rm tot}$ change is affected by process variation. In particular, if M_{n4} is in SS

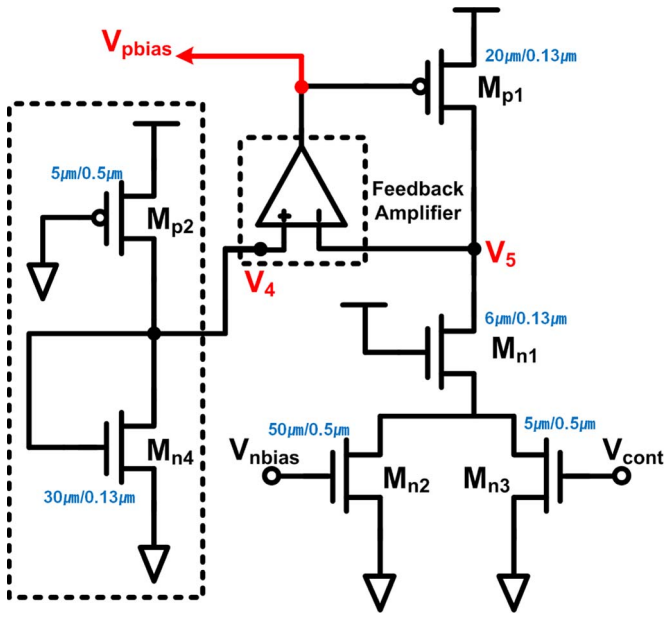

Fig. 4. Voltage-swing controller circuit topology.

or FS corner, $I_{\rm compen}$ change is reduced. Then, $I_{\rm bias}$ variation increases because $I_{\rm tot}$ change due to supply noise is less affected by process variation than $I_{\rm compen}$ change.

B. Voltage-Swing Controller

Fig. 4 shows the voltage-swing controller circuit. It also has a feedback amplifier that maintains V_5 same as V_4 by using the regulated gate voltage of $M_{p1}(V_{p\rm bias})$ even if $V_{n\rm bias}$, $V_{\rm cont}$, and supply voltage change. Because M_{p1}, M_{n1}, M_{n2}, and M_{n3} are the replica of the delay cell in RVCO, RVCO $V_{\rm swing}$ is maintained from V_{DD} to V_4. Although $V_{n\rm bias}$ from bias-current controller is supplied to the voltage-swing controller, there is no feedback loop between two controllers because $V_{p\rm bias}$, which is the output of the voltage-swing controller, does not have any effect on $V_{n\rm bias}$. Consequently, with the sufficient phase margin for each controller, there is no stability problem for two controllers.

When supply voltage increases due to supply noise, for example, $V_{\rm swing}$ of RVCO also increases because V_4 is independent of supply noise, as shown below

$$V_4 \approx V_{\rm th}. \tag{4}$$

Similarly, in the case of FF corner, $V_{\rm swing}$ also increases because V_4 is decreased. Fig. 5 shows the simulation results in which $I_{\rm bias}$ and $V_{\rm swing}$ change is measured against $\pm 5\%$ supply voltage variation in various process corners. Although the bias-current controller reduces $I_{\rm bias}$ dependence on supply voltage, it is still proportional to supply voltage. However, the voltage-swing controller makes $V_{\rm swing}$ also proportional to the supply voltage so that $I_{\rm bias}/V_{\rm swing}$ remains approximately constant and, consequently, RVCO oscillation frequency is stabilized. Although Fig. 5 shows the case of $V_{\rm cont} = 0$, simulation results for other values of $V_{\rm cont}$ show similar results.

Fig. 6 shows the simulated VCO operating frequencies with and without compensation at various control voltages

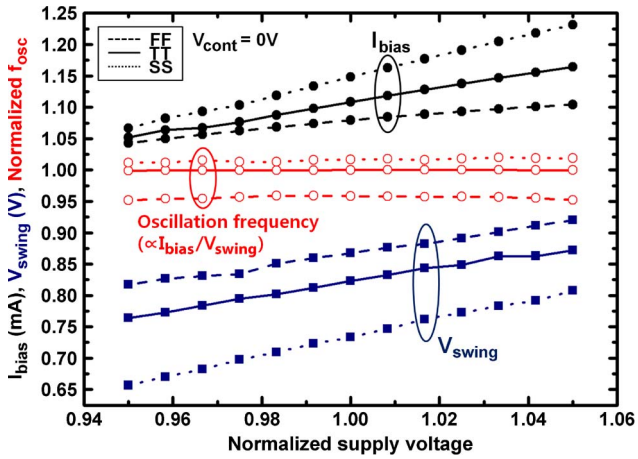

Fig. 5. Simulation results of bias-current, voltage-swing, and normalized oscillation frequency variation due to supply noise ($\pm 5\%$) in each process corner.

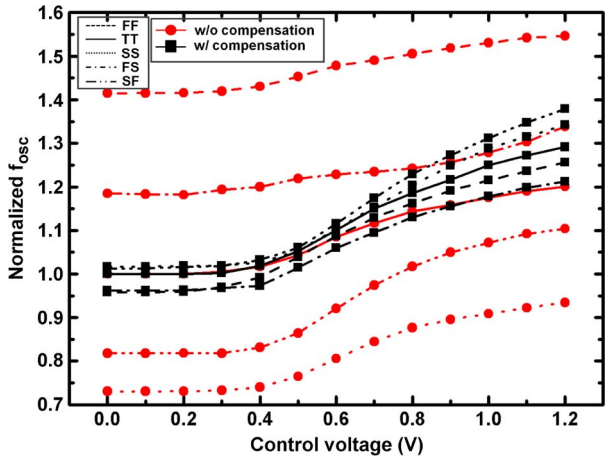

Fig. 6. Simulated RVCO operating frequency curve.

for various different process corners. The RVCO oscillation frequencies are normalized by the oscillation frequency of each RVCO at zero control voltage in TT corner. Without compensation, the oscillation frequency increases by about 41% in FF corner and decreases by about 22% in SS corner at zero control voltage. In contrast, with compensation, the oscillation frequency decreases by only 4.4% in FF corner and increases by 1.7% in SS corner. Because the VCO gain is affected by process variation, the frequency difference among each process corners becomes larger when the control voltage is higher. The oscillation frequency change due to process variation is slightly over compensated because the required changes in $I_{\rm bias}$ and $V_{\rm swing}$ for supply noise compensation is different from those for process variation compensation. For our design, we optimized the controllers for supply noise compensation.

C. Overall PLL Design

A PLL having 4-stage RVCO with the voltage-swing and the bias-current controller was fabricated in 0.13-μm CMOS technology. Fig. 7 shows the fabricated chip. The chip includes two types of PLLs: PLL1 includes both controllers and PLL2 does not have any controller. Both PLLs have the essentially

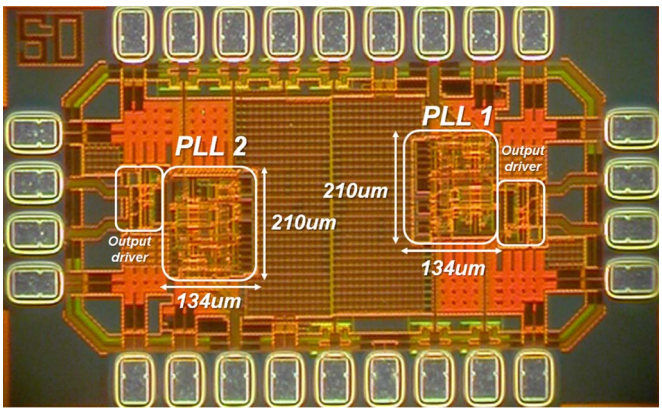

Fig. 7. Chip micrograph.

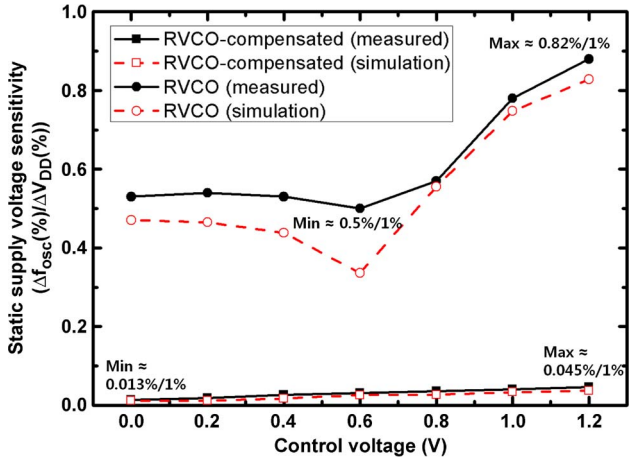

Fig. 8. Static supply voltage sensitivity of each type of RVCO.

same core area of 0.02814 mm^2 (210 μm $\times$ 134 μm), excluding the output drivers and off-chip loop filters as controllers virtually require no additional die area. The power consumption is 42 mW for PLL1 and 38 mW for PLL2.

For the feedback amplifiers inside the controllers for PLL1, we designed their bandwidth to be larger than the PLL natural frequency. This is because supply noise has the bandpass characteristics with the center frequency at the PLL natural frequency. 2pF on-chip capacitor was used for feedback stability of the amplifier as well as filtering of high-frequency noises in the controller output voltage.

III. Simulation and Measurement Results

In order to evaluate the static supply voltage sensitivity, dc supply voltage was varied by $\pm 5\%$ around 1.2 V, and the resulting free-running RVCO oscillation frequency variation was simulated and measured at various control voltages. The results are shown in Fig. 8.

The supply voltage sensitivity can be defined by the percentage change in the oscillation frequency to the percentage change in the supply voltage. Measured results show that RVCO with compensation achieves lower than $0.045\% - \Delta f_{\rm vco}/1\% - \Delta V_{DD}$ at every control voltage, whereas RVCO without compensation has higher than $0.5\% - \Delta f_{\rm vco}/1\% - \Delta V_{DD}$ at every control voltage. Simulation results agree well with measurement results.

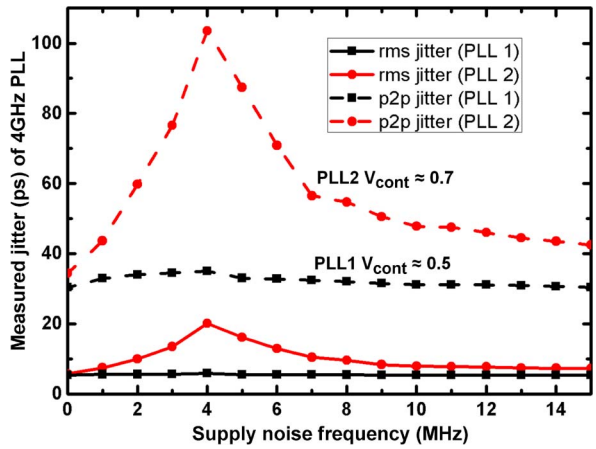

Fig. 9. Measured jitter with supply noise frequency.

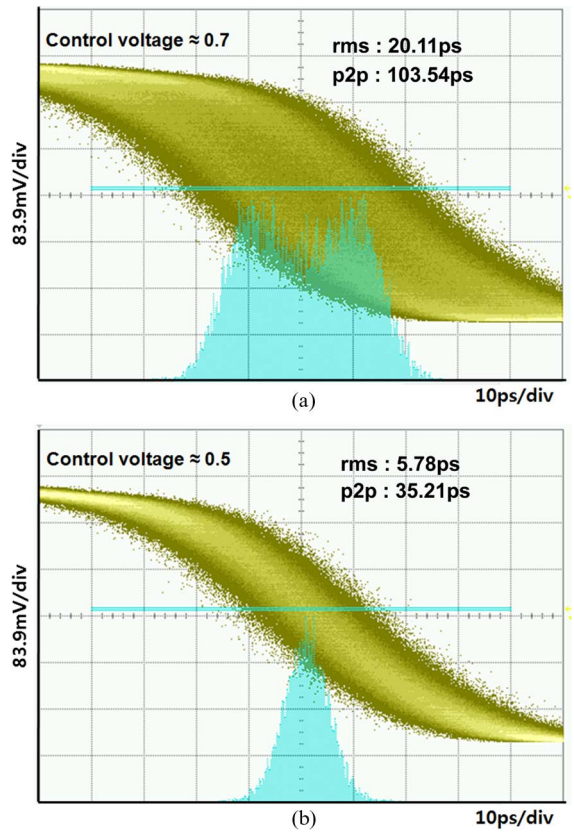

Fig. 10. Measured jitter for a 4-MHz noise frequency. (a) PLL2. (b) PLL1.

To verify the dynamic supply voltage sensitivity, two types of PLL were measured in the presence of intentional RVCO supply noise added to PLL V_{DD}. For measurement, the die was directly mounted and wire bonded on a printed circuit board without any packaging. The noise was produced by 10-mV (peak-to-peak) sinusoidal signals ranging from 1 to 15 MHz. The measured jitters of the PLL operating at 4 GHz with these supply noises are shown in Fig. 9. PLL2 shows the clear bandpass characteristics, whereas PLL1 shows a flat response. This result indicates that the VCO having compensation controllers successfully suppresses dynamic supply noises. Fig. 10(a)

TABLE I
PERFORMANCE SUMMARY

Technology	0.13μm CMOS
Supply	1.2V
Target frequency	4GHz
Reference clock	250MHz
Loop bandwidth	4MHz
Die area	$0.028mm^2$
Power @ f_{osc}	PLL1 – 42mW@4GHz PLL2 – 38mW@4GHz
Static Supply Sensitivity	PLL1 – 0.013%/1% PLL2 – 0.5%/1%
PLL rms Jitter without supply noise	PLL1 – 5.3ps PLL2 – 5.65ps
PLL rms Jitter with supply noise (4MHz)	PLL1 – 5.78ps PLL2 – 20.11ps

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED PLL

	Mansuri [5]	Wu [8]	Elshazly [10]	This work
Process	0.25μm	0.13μm	0.13μm	0.13μm
Type	Modified VCO	Digital Cal.	Digital Cal.	Modified VCO
Target frequency	1GHz	1.4GHz	1.5GHz	4GHz
Static Supply Sensitivity	0.03%/1%	N/A	N/A	0.013%/1%
PLL Jitter Reduction	N/A	from 0.024UI to 0.005UI	from 0.033UI to 0.01UI	from 0.08UI to 0.023UI
Area penalty	almost none	160μm $\times$ 90μm	140μm $\times$ 80μm	almost none
Power penalty	N/A	N/A	0.28mW	4mW

and (b) shows the measured traces of output waveforms for both PLLs with 4-MHz supply noises. The measured rms jitter is improved from 20.11 to 5.78 ps with our compensation technique. Table I summarizes and compares the performance of two PLLs.

Table II compares PLL1 with recently reported PLLs employing compensation techniques. Our technique successfully compensates the influence of supply noise on VCO with virtually no die area penalty. Moreover, this technique can also compensate process variations, which is not possible for other structures. Although the power penalty is relatively high for our scheme, this can be reduced with further optimization of feedback amplifiers and reference voltage generators.

IV. CONCLUSION

A new on-chip supply noise and process variation compensation technique for RVCO is demonstrated. In our technique, RVCOs has the bias-current and the voltage-swing controller that can compensate supply voltage and process variation. The simulation result shows that the oscillation frequency difference between FF and SS corner is about 6% of oscillation frequency in NN corner. Measurement results of PLLs implemented in 0.13-μm CMOS process show that both static and dynamic supply voltage sensitivity are greatly reduced with the compensation circuits. Our compensation circuits are simple and entirely composed of an active device having a negligible die area penalty.

ACKNOWLEDGMENT

The authors would like to thank C.-K. Seong, D.-H. Kim, K.-C. Choi, W.-S. Kim, and J.-S. Rhim in High-Speed Circuits and Systems Laboratory, Yonsei University, for many helpful discussions. The authors would also like to thank the IC Design Education Center, for the support of EDA software and chip fabrication.

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