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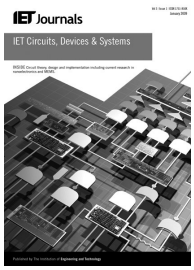

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Fully integrated serial-link receiver with optical interface for long-haul display interconnects

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Abstract: We report a fully integrated serial-link receiver with optical interface fabricated with a 0.18 μm complementary metal oxide semiconductor technology for long-haul display interconnects. The receiver includes a trans-impedance amplifier, a limiting amplifier, a clock and data recovery circuit, 1:64 de-multiplexer and a built-in error checker. The receiver produces 64-bit wide electrical signals from photodetector output signals produced by 5.28, 5.6 or 6.25 Gb/s optical signals delivered through up to 700-m multi-mode fibre. It can support serialised data for UXGA, 1080 p and WUXGA. The receiver core occupies 0.59 mm^2 with 42.4 mW power dissipation at 6.25 Gb/s bit rate from a 1.8 V supply.

1 Introduction

As information and broadcast technologies advance, there are growing interests in high-definition (HD) video and high-performance display devices such as HDTV, HD monitor and HD display wall. Consequently, higher data rates are required from interconnects for display applications. High-definition multimedia interface (HDMI) is one of the most popular interfaces for uncompressed display interconnects. Its transmission channel consists of three data channels and one clock channel. The clock channel has one-tenth frequency of the data rate in the data lanes. Our design target is realising serialiser/de-serialiser (SERDES) for HDMI, which reduces four channels into one and provides much longer transmission distance with optical interface, as shown in Fig. 1. We are interested in optical serial interface based on low-cost 850-nm vertical cavity surface-emitting laser (VCSEL) and multi-mode fibre (MMF), since it allows much longer transmission distances than is possible with electrical cables, allowing more flexible display applications [1].

Our SERDES can support HDMI version 1.2 (UXGA) as well as 1080 p and WUXGA. Since HDMI uses transition-minimised differential signaling (TMDS) coding, which requires about 75% overhead over raw data, the total TMDS data throughput is 4.95 Gb/s for UXGA, 5.26 Gb/s for 1080 p and 5.86 Gb/s for WUXGA as summarised in Table 1 [2]. Our SERDES needs additional 64/60 overhead for sequence alignment and resolution information resulting in total optical interface throughput of 5.28, 5.6 and 6.25 Gb/s for UXGA, 1080 p and WUXGA, respectively. In this paper, we demonstrate a fully integrated serial-link receiver with optical interface circuits fabricated with a 0.18 μm complementary metal oxide semiconductor (CMOS) technology. CMOS process allows higher integration levels with lower costs compared with previously reported compound semiconductor approaches [3]. Our receiver includes a trans-impedance amplifier (TIA), a limiting amplifier (LA), a dual-loop clock and data recovery (CDR), a 1:64 de-multiplexer (DEMUX) and a built-in pseudo-random bit sequence (PRBS) error checker. The paper is organised as follows. Detailed descriptions of receiver design are described in Section 2. Measurement results are discussed in Section 3 and a conclusion is given in Section 4.

2 Receiver design

2.1 Challenges for integrated receiver design

Integrated serial-link receivers having TIA, LA, CDR and DEMUX have been previously reported [4–6]. These were, however, realised with compound semiconductor technology and, although they show good performance, improvement in power consumption as well as cost-effectiveness is desired. For this, there is a great interest in realising integrated receivers in CMOS technology. Although several CMOS serial-link receivers have been reported [7–12], [7–9] had only CDR and DEMUX, [10] had only oscillator and DEMUX with global clock, and no integrated receivers having only dual-loop CDR has been reported [11, 12].

To meet our specific application, receiving serialised TMDS signal through one fibre, the proposed serial-link receiver is highly integrated with optical receiver front-end, is realised in low-cost CMOS technology, and is designed to cover the input data range (5.28, 5.6 and 6.25 Gb/s). Highly integrated receivers can result in poor jitter

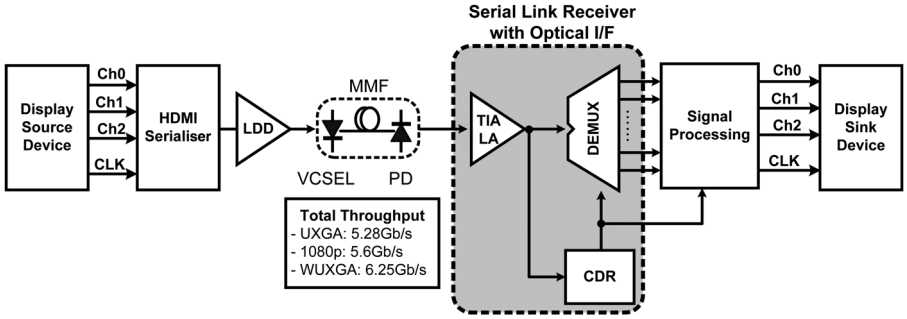

Fig. 1 *Serial link with optical interface for long-haul HDMI interconnects*

Table 1 Optical I/F data throughput according to the desired resolution

Resolution	Horizontal width	Vertical width	Colour depth [bit]	Frame frequency, Hz	Raw data throughput, Gb/s	TMDS data throughput, Gb/s	Optical I/F throughput, Gb/s
UXGA	1600	1200	24	60	2.76	4.95 (3 × 1.65)	5.28
1080 p	1920	1080	24	60	2.98	5.26 (3 × 1.75)	5.60
WUXGA	1920	1200	24	60	3.31	5.86 (3 × 1.95)	6.25

performance because of integration of different function blocks in the chip. TIA is particularly noise-sensitive because of its small input currents as well as is very dominant block in terms of noise performance. Consequently, the integration of TIA, LA, CDR and DEMUX leads to large area, large power and poor jitter performance. To solve these issues, various efforts are conducted in the prototype chip, and details are described in below.

2.2 Receiver architecture

Fig. 2 shows the receiver architecture. The photodetector (PD) output currents are converted into voltage signals by TIA and limited to 400 mVp-p differential voltage signals by LA. In CDR, clock extraction and data recovery are done in two steps, so that it can handle multi-rate input data rates. In the first step, LC-type voltage-controlled oscillator (VCO) is locked by the frequency adjustment loop to one of the three

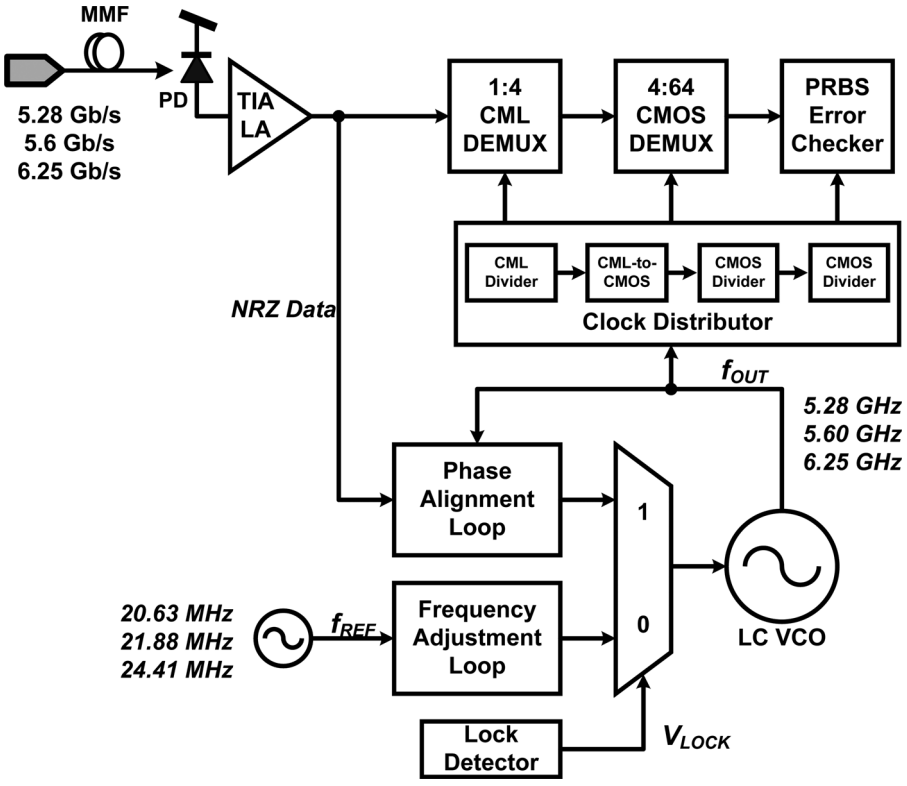

Fig. 2 *Serial-link receiver architecture*

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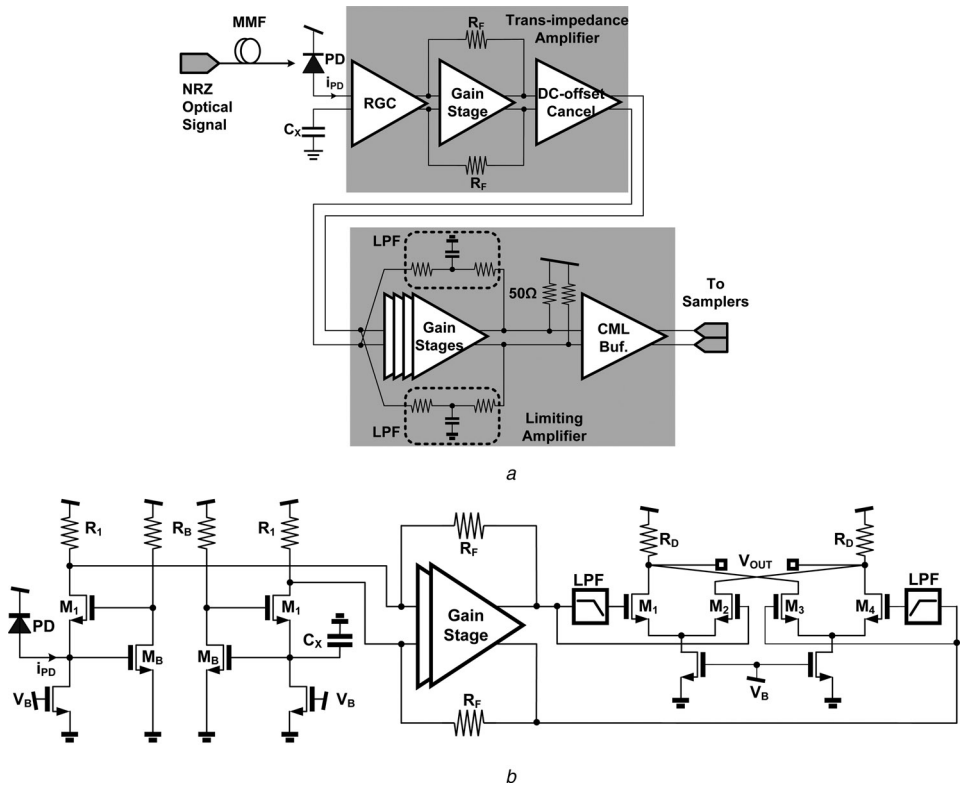

Fig. 3 *Optical receiver front-end circuit and detail schematics of the TIA*

a Block diagram of an optical receiver front-end circuit, and
b Detail schematics of the TIA

reference clocks, which have 1/256 clock speed compared with the desired transmission date rate. When frequency locking is done, the lock detector generates enable signal (V_{LOCK}), which then connects VCO to the phase alignment loop. With this, the VCO output (f_{OUT}) is aligned to the optimum sampling point to the incident NRZ data.

The clock distributor provides proper clock signals having desired frequency, driving capacity and swing levels to DEMUXs. Demuxing is done in two steps, 1:4 first step with current-mode logic (CML) and 4:64 second step with CMOS logic. To minimise power consumption, CML is used only when necessary for high-speed blocks, whereas other low-speed blocks use CMOS logic. High-speed 1:4 and 4:8 DEMUXs are designed with the tree structure for power reduction, whereas 4:64 DEMUX is based on the shift-register architecture for chip area reduction [13]. For testing purpose, a PRBS error checker is embedded.

2.3 Optical receiver analogue front-end circuit

Fig. 3*a* shows the optical receiver analogue front-end circuit. The TIA consists of a regulated cascode (RGC) current buffer, gain stage with a feedback resistor (R_F) and DC-offset cancellation amplifier. The RGC buffer is used to isolate the effect of an inherent PD junction capacitance from the bandwidth determination [14]. The TIA is designed with consideration for a commercial GaAs-based p–i–n PD having 0.5 A/W responsivity, 0.3 pF junction capacitance and 8.5 Gb/s maximum data rate [15]. A modified Cherry–Hooper amplifier with active feedback

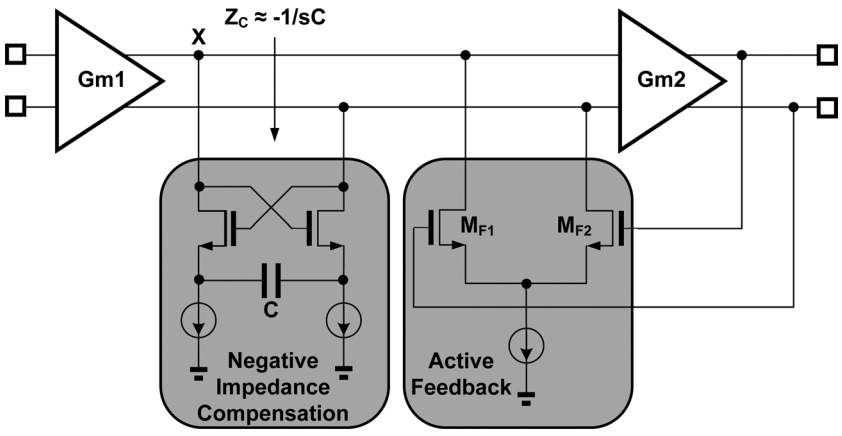

Fig. 4 *Block diagram of a modified Cherry–Hooper amplifier with negative impedance compensation*

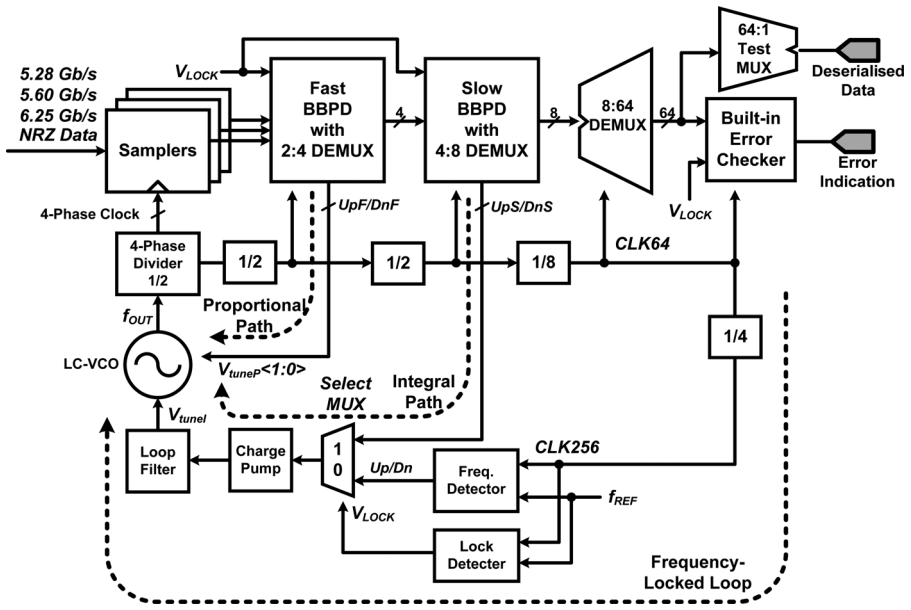

Fig. 5 *Detailed dual-loop CDR operations*

a Frequency adjustment loop by frequency-locked loop and
b Phase alignment loop by bang–bang phase detector

is used for the gain stage with 2 kΩ of R_F [16]. DC-offset cancellation amplifier is essential for a differential optical receiver to cancel DC-offset errors between differential gain-stage outputs because of an inherent pseudo-differential structure [17]. Detailed schematic diagram of the TIA is shown in Fig. 3*b*. The TIA has a 62 dBΩ trans-impedance gain, 5 GHz, 3 dB bandwidth and consumes 4.5 mA DC currents. The TIA is the most noise-sensitive and noise-dominant part in the serial-link receiver because it deals with very small-swing signals. Therefore the TIA is located as far as possible from the other blocks having above several hundred mV swing, and sub-contacts and well-contacts are added in between the TIA and the other blocks for isolation purpose. The power and ground pads of the TIA are also separated from the others, and many bypass capacitors are exploited for power and bias pads of the TIA. Simulated average noise current spectral density and input-referred noise is, respectively, 12.8 pA/√Hz and 0.96 μA, corresponding to −17.5 dBm of optical sensitivity [bit error rate (BER) $=10^{-12}$, responsivity = 0.5 A/W, extinction ratio = 7].

The LA consists of identical four-stage voltage amplifiers, a CML-type output buffer and low-pass filter for DC-offset cancellation. Modified Cherry–Hooper amplifier is also used as a gain stage with negative impedance compensation stage to cancel parasitic capacitance components, as shown

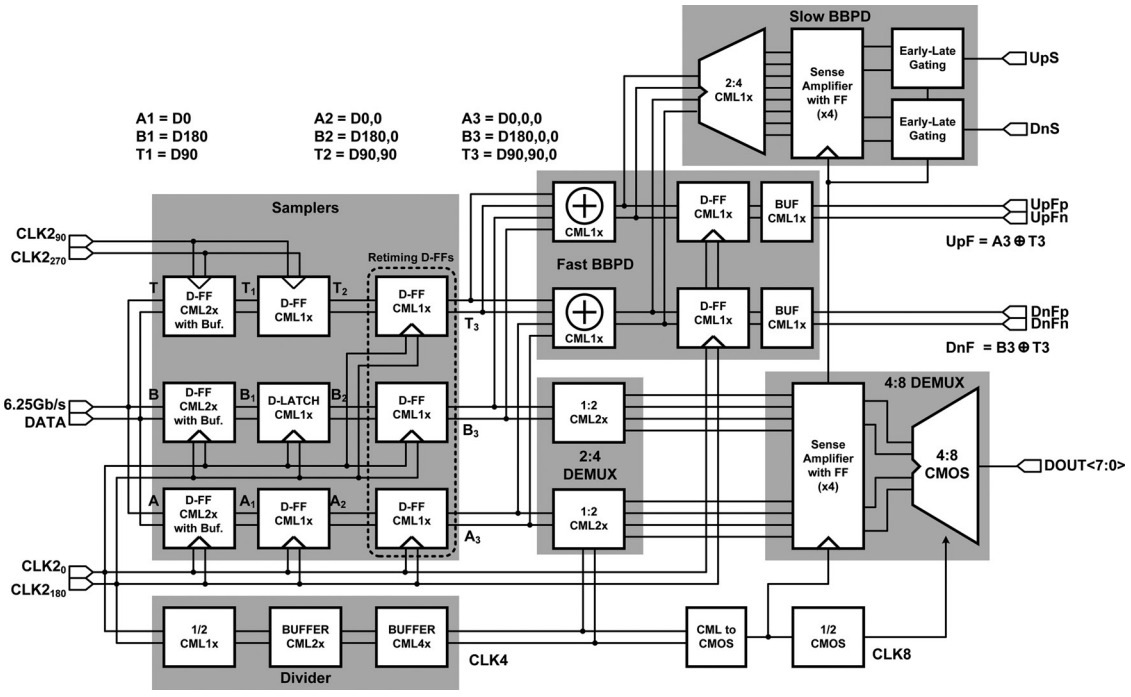

Fig. 6 *Block diagram of samplers, 2:4 CML DEMUX, 4:8 CMOS DEMUX, fast BBPD and slow BBPD*

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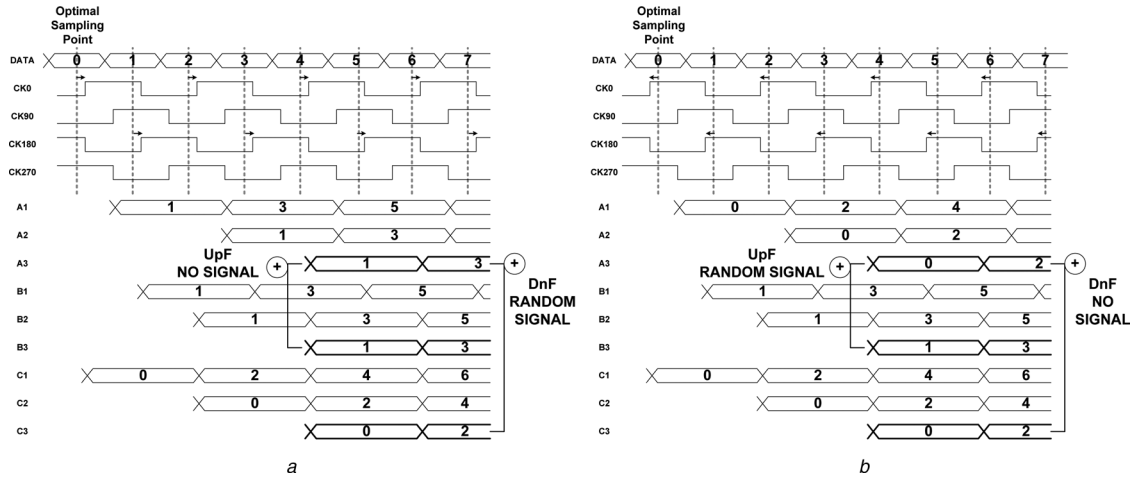


Fig. 7 *Timing diagram of fast bang–bang control signals when*

a Clock leads data and
b Clock lags data

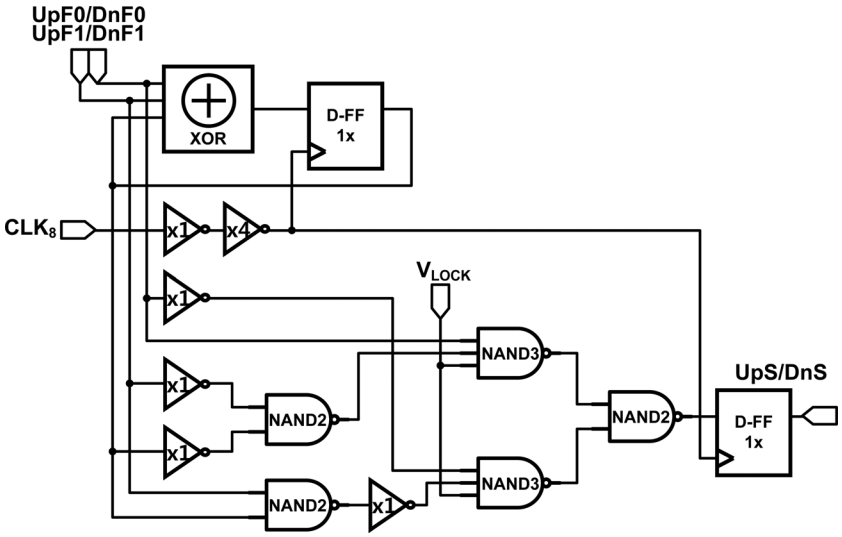


Fig. 8 *Block diagram of an early–late gating circuit*

in Fig. 4 [18]. Single-ended output swing of the LA is determined to 200 mVp-p based on the input dynamic range of the next CML D flip-flops (D-FFs), related with PVT variations, fan-out and CML latch offsets. The combination of the TIA and the LA exhibits 106 dBΩ trans-impedance gain and 4.8 GHz, 3 dB bandwidth, and

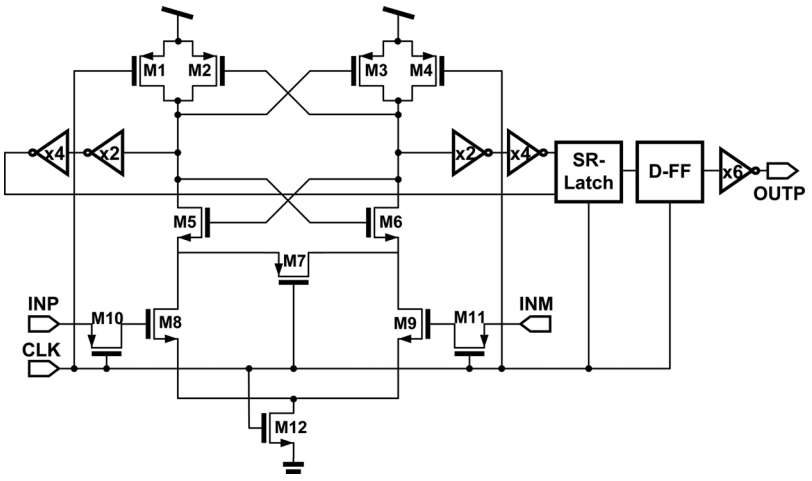
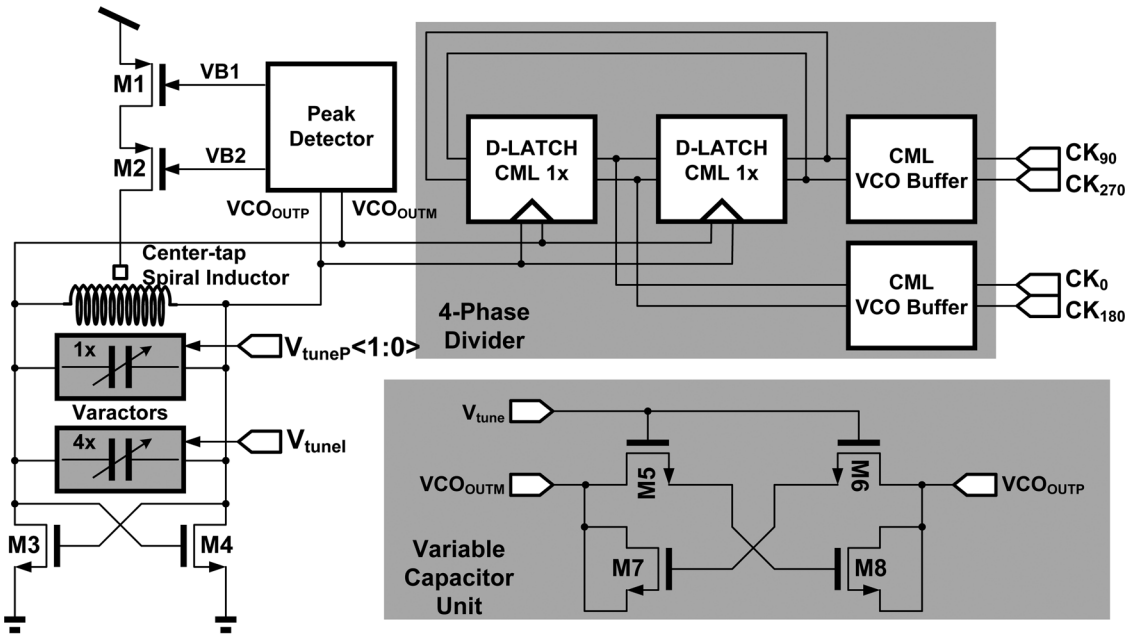


Fig. 9 *Schematic diagram of a clocked sense amplifier*



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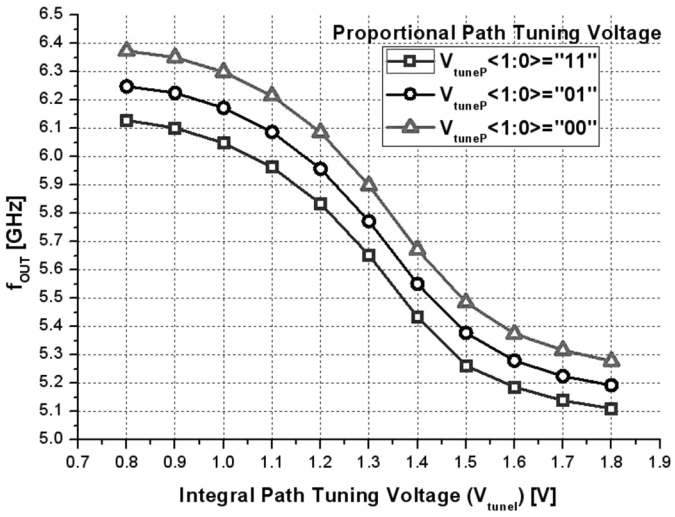

b

Fig. 10 *LC-VCO with four-phase frequency divider and VCO tuning range*

a Block diagram of LC-VCO with four-phase divider and
b VCO tuning range

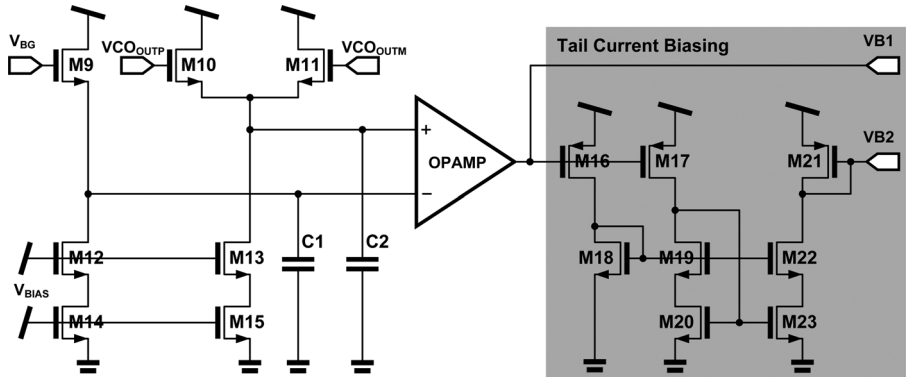

Fig. 11 *Schematic diagram of peak detector*

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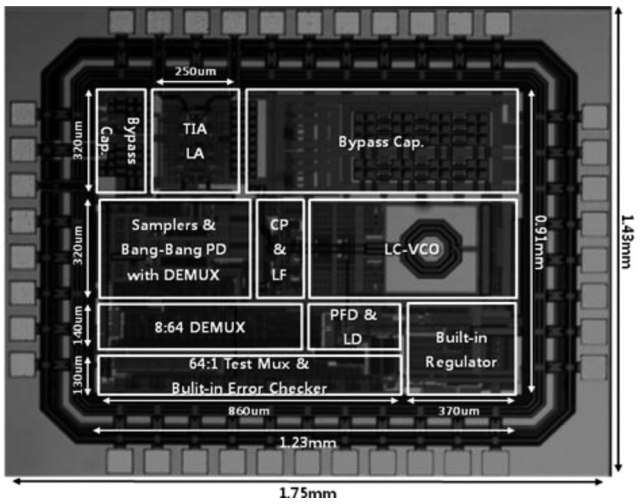

Fig. 12 *Chip microphotograph*

Table 2 Power consumption, area and power efficiency of a sort of blocks

Building blocks	Power consumption, mW	Area, mm^2
TIA	9.0	0.08
LA	14.4	–
samplers	4.6	0.12
fast BBPD	1.6	–
2:4 DEMUX with divider	1.4	–
4:8 DEMUX and slow BBPD	1.4	0.08
PFD, CP, LF and LD	2.2	–
LC-VCO	3.6	0.23
four-phase divider	2.7	–
8:64 DEMUX	1.4	0.08
subtotal	42.4	0.59
subtotal w/o optical RX	19.0	0.51
64:1 Test MUX and built-in error checker	4.5	0.11
regulator, bias circuitry and output buffers for test	6.8	0.10
bypass capacitor	–	0.31
total	49.6	1.11

consumes 12.5 mA DC currents including CML output buffer.

2.4 Dual-loop CDR circuit

Details of dual-loop CDR operation are described in Fig. 5. The frequency-locked loop consists of frequency detector, charge pump, loop filter, LC-VCO and frequency dividers. The lock detector generates selecting signal of the select multiplexer (MUX). Under unlock condition, the charge pump is controlled by the output (Up, Dn) of the frequency detector. After frequency lock, the phase alignment step starts. When V_{LOCK} goes high, fast and slow BBPDs are enabled. The bang–bang phase control path is separated into two parts: proportional path and integral path [19]. The fast bang–bang signals (UpF, DnF) of the proportional path directly control a set of varators inside LC-VCO with information on phase error polarity. The integral path is controlled by the slow bang–bang signals (UpS, DnS) through the charge pump followed by a loop filter having two poles and one zero. The CDR has loop bandwidth of 407 kHz, phase margin of 61° and closed-loop peaking of 1.32 dB. By separating the bang–bang phase control path, the feedback-loop latency can be reduced and the bandwidth requirements of the charge pump can be relaxed [11, 20]. The amount of added root-mean-square (RMS) jitter generation because of the proportional path is 960 fs corresponding to the 6 mUI RMS. To prevent this jitter generation, proportional control path can be substituted into a linear phase detector [12]. Through two parts of bang–bang phase control, the phase alignment loop tries to align the rising edge of four-phase clock to the optimal sampling point. To prevent any interactions between the two loops, simultaneous operation does not occur [21].

2.5 Samplers, DMUXs and bang–bang phase detector

Fig. 6 shows a block diagram of samplers, 2:4 CML-type DEMUX, 4:8 CMOS-type DEMUX, fast BBPD and slow BBPD. Fast and slow BBPDs are enabled by V_{LOCK} as mentioned above. 5.28, 5.6 or 6.25 Gb/s serial data go through three paths (A, B and T) by three samplers and each path consists of three sampling D-FFs with a delay buffer, sampling D-FFs or D latch (for path B) and retiming D-FFs. In Fig. 6, paths A and B represent successive data streams sampled at 0° and 180° of the clock phase. Path T samples an input data at the transition timing between paths A and B with 90° of the clock phase. When two bits of paths A and B have different polarities, path T can sense whether the clock is early or late compared with data. If T3 equals to A3, the clock leads the data and vice versa. The fast BBPD generates the maximum 3.125 GHz bang–bang control signals (UpF, DnF) by comparing paths A, B and T through exclusive OR (XOR) gates. To minimise the effect of a phase mismatch between quadrature clocks, retiming D-FFs are used before the fast BBPD. The samplers and fast bang–bang phase detector combined with 1:2 and 2:4

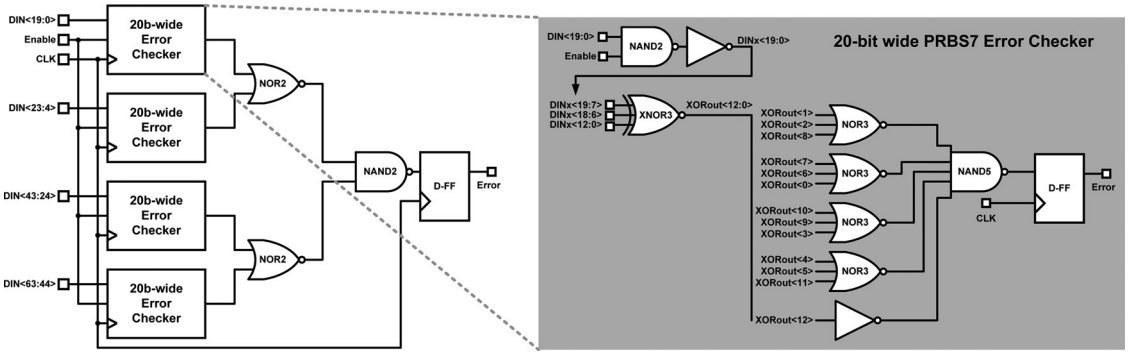

Fig. 13 *Built-in error checker for PRBS 2^7-1*

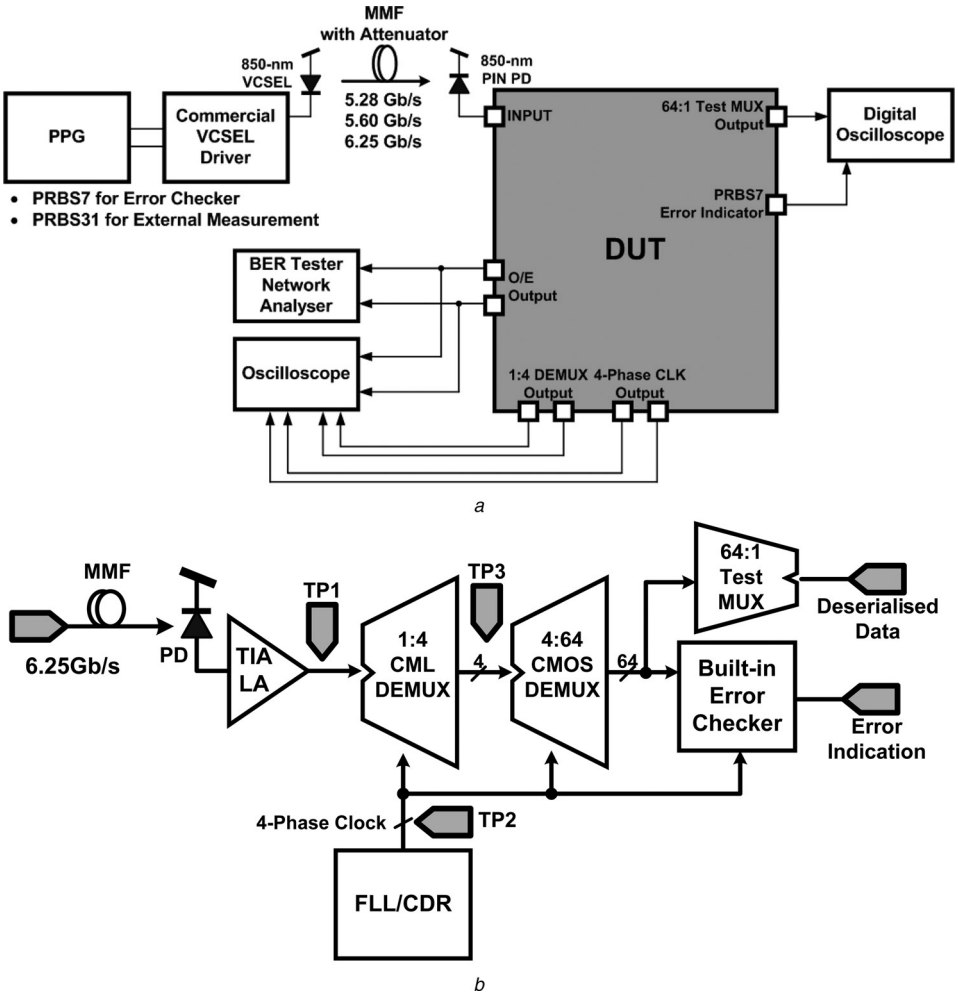

Fig. 14 *Measurement setup and additional test points of DUT*

a Measurement setup and
b Additional test points of the DUT

CML DEMUX makes the chip area small, and makes unnecessary phase alignment between proportional path and integral path. A detailed timing diagram for samplers and fast BBPD is described in Fig. 7 for both fast and slow clock conditions. Slow bang–bang signals (UpS, DnS) are generated by de-multiplexing UpF and DnF through the bang–bang gating circuit, as shown in Fig. 8. These slow bang–bang signals control VCO through the charge pump and the loop filter.

Samplers, fast BBPD, 2:4 DEMUX and divider operate on high-speed CML signals and consume a large amount of currents. To reduce current consumption, 4:8 DEMUX and slow BBPD are designed with CMOS logic. A clocked sense amplifier is used for efficient conversion from CML to CMOS logic, as shown in Fig. 9. The notations of each CML block in Fig. 6, for example, $1\times$, $2\times$ and $4\times$, indicates the amount of tail currents compared with that in the basic CML buffer, which consumes 0.15 mA. The CMOS logic can process up to 1.5625 Gb/s data.

2.6 LC-VCO with four-phase frequency divider

Fig. 10*a* shows LC-type N-core VCO with four-phase frequency divider. A centre-tap spiral inductor (1.15 nH) is used, and Miller capacitors are used as variable capacitors, shown in inset of Fig. 10*a*. The variable capacitors are controlled by two different control signals. One is a proportional control signal (VtuneP⟨1:0⟩) from the fast BBPD, and the other is an integral control signal (VtuneI) from the slow BBPD in the phase alignment loop or from the frequency detector through the charge pump and the loop filter in the frequency alignment loop. VtuneP⟨1:0⟩ have information only on the phase error polarity and rapidly changes with the data frequency, whereas VtuneI has information on the accumulated phase error. VtuneP⟨1:0⟩ are digital signals with CML level where the low level is represented by 1.2 V and the high level by 1.8 V. These proportional control signals directly control variable capacitors. Consequently, the proportional path pushes fast locking, whereas the integral path makes it possible to achieve the accuracy.

A variable capacitance controlled by VtuneI is designed to be larger than one controlled by VtuneP⟨1:0⟩ by factor of 4 in order to reduce ripple voltages. The proportional path has 208 MHz/V of VCO gain and the integral path 1.095 GHz/V. The simulated frequency tuning range at different conditions of UpF/DnF and VtuneI is depicted in Fig. 10*b*. The peak detector forces the output swing of LC-VCO to equal the bandgap voltage (1.25 V) by controlling tail currents, and its schematic is depicted in Fig. 11. LC-VCO output passes through four-phase frequency divider for half-rate bang–bang operation, shown in inset of Fig. 10*a*.

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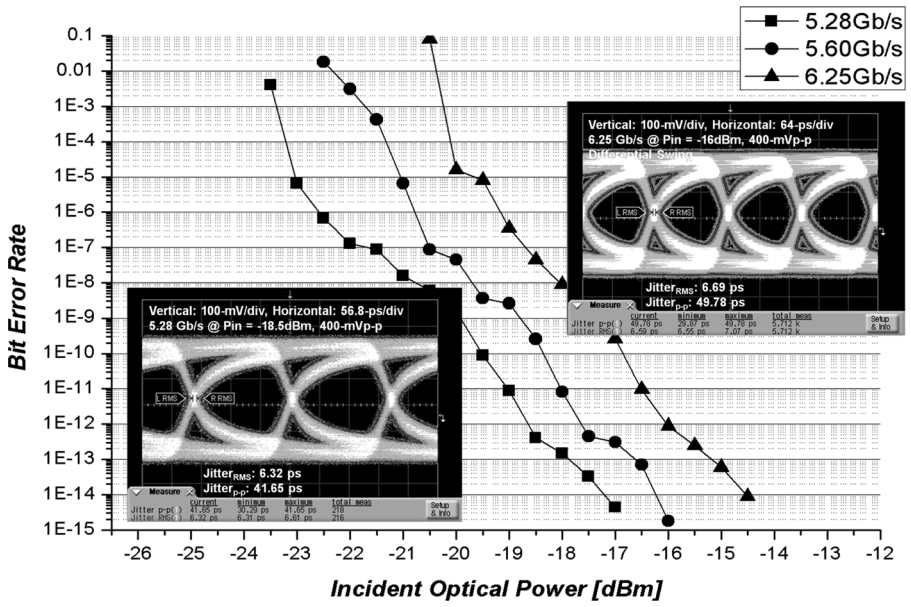

Fig. 15 *Measured BER according to the incident optical power and 5.28 and 6.25 Gb/s eye diagrams at TP1*

3 Chip implementation and measurement results

3.1 Chip implementation

A fully integrated serial-link receiver was fabricated with standard 0.18 μm CMOS technology. Fig. 12 shows a microphotograph of the chip that occupies the area of 1.75 mm × 1.43 mm including electrostatic discharge (ESD) protection diodes and bonding pads. The receiver consumes 27.55 mA of DC currents with a single 1.8 V supply voltage. Table 2 shows power consumption and chip area for each block. Core area and power consumption excluding ESD protection pads, test circuitry, bias circuitry and bypass capacitors are 0.59 mm^2 and 42.4 mW, respectively, corresponding to the 6.78 mW/Gb/s power efficiency. To confirm 1:64 DEMUX properly operates for 64-bit parallel output data, the PRBS error checker is embedded and its schematic is shown in Fig. 13. The error checker can make a decision whether 64-bit wide parallel data are correct PRBS $2^7 - 1$ data or not. For our prototype chip, the error checker did not detect any errors during about two days of continuous operation, which corresponds to above 10^{-15} of BER.

3.2 Measurement setup

Fig. 14*a* shows the measurement setup. The fabricated chip was integrated with a commercial 850 nm GaAs p–i–n PD on a printed circuit board. The PD has 7.5 GHz, 3 dB bandwidth, 0.5 A/W responsivity and 0.3 pF junction capacitance according to its data sheet. A pulse pattern generator created PRBS $2^7 - 1$ for the on-chip error checker operation and PRBS $2^{31} - 1$ for other measurements. For optical modulation, a commercial 850 nm VCSEL was used. MMF used in the measurement was 700 m long. An optical attenuator was used for the optical sensitivity measurement. For the measurement purpose, our chip had three test points, TP1 at the output of LA, TP2 at the output of four-phase clocks and TP3 at the output of 1:4 CML DEMUX, as shown in Fig. 14*b*.

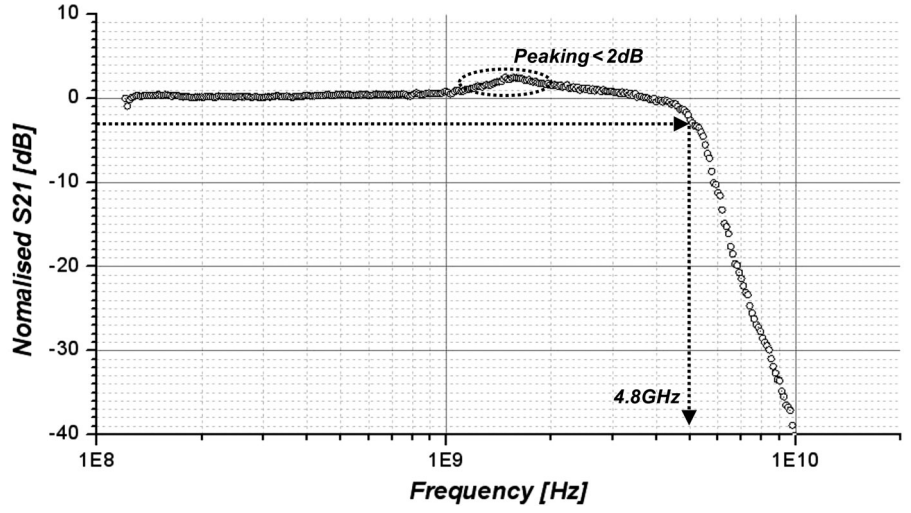

Fig. 16 *Measured S21 at TP1*

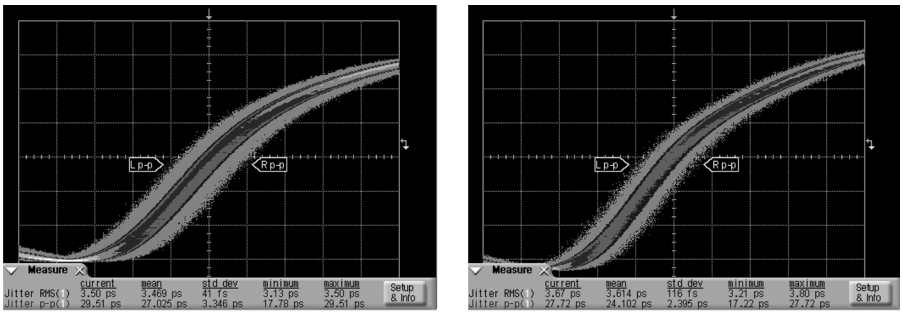

Fig. 17 *Measured four-phase clock waveforms at TP2:*
a 3.125 GHz clock for 6.25 Gb/s data and
b 2.64 GHz clock for 5.28 Gb/s data

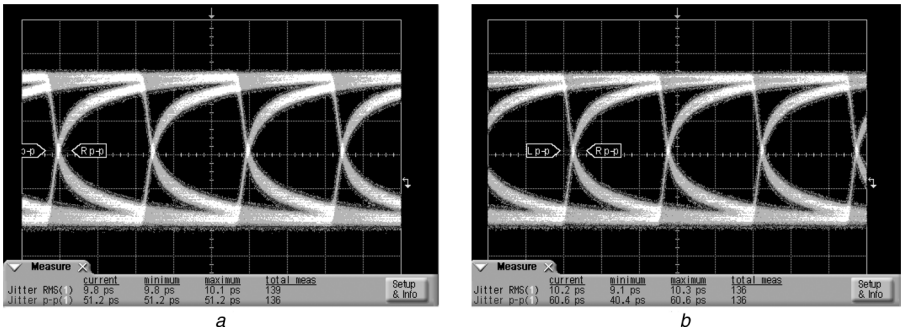

Fig. 18 *Measured 1:4 deserialised data eye diagrams at TP3:*
a 1.5625 Gb/s data for 6.25 Gb/s data and
b 1.32 Gb/s data for 5.28 Gb/s data

3.3 Measurement results

Fig. 15 shows measured BERs at different incident optical powers. Optical sensitivity of −21.1, −20.0 and −18.5 dBm were measured at TP1 for 5.28, 5.6 and 6.25 Gb/s data, respectively. Inter-symbol interference because of bandwidth limitation in our receiver makes causes the sensitivity increase for higher data rates. Measured S21 at TP1, shown in Fig. 16, shows 3 dB bandwidth of 4.8 GHz and 2 dB peaking at about 1.6 GHz which results from the modified Cherry–Hooper topology of the post amplifier. Measured bandwidth indicates 77% of the maximum bit rate; therefore the optical receiver is located at near optimal points in terms of noise. Measured eye diagrams at TP1 are shown in Fig. 15 as insets. 5.28 and 6.25 Gb/s eye diagrams exhibit 6.32 ps/6.69 ps of RMS jitters and 41.65 ps/49.78 ps of peak-to-peak jitters, respectively, with differential 400 mVp-p output swing. Fig. 17 shows the output of four-phase clocks at TP2. The half-rate 3.125 and 2.64 GHz clocks have and

Table 3 Performance summary and comparison with published receivers for serial link

Parameters	[4]	[11]	[12]	[7]	[8]	[9]	This work
technology	InP HBT	CMOS 130 nm	CMOS 130 nm	CMOS 130 nm	CMOS 65 nm	CMOS 90 nm	CMOS 180 nm
data rates, Gb/s	7.5	0.5–3.2	0.5–2.5	6.25	6.4	6.25	5.28 5.60 6.25
integration level	PD/TIA/LA CDR 1:8 DEMUX	CDR	CDR	CDR 1:8 DEMUX equaliser	CDR 1:4 DEMUX	CDR 1:16 DEMUX equaliser	TIA/LA CDR 1:64 DEMUX
core area, mm^2	12.9[a]	0.2	0.36	0.24	0.33	0.15	0.59
supply, V	3.3	1.2	1.2	1.2	1.0	1.2	1.8
power dissipation, mW	3000	7 (at 2.5 Gb/s)	6.1 (at 2 Gb/s)	210	28.9	11.6	42.4 (19.0)[b] (at 6.25 Gb/s)
power efficiency, mW/Gb/s[d]	400	2.8	3.05	33.6	4.5	1.9	6.8 (3.0)[b]
transmission channel	18 km[c]SMF	N/A	N/A	76.2 cm FR4	N/A	80 cm FR4	700 m MMF

[a]This is total chip area including bonding pads.
[b]Power dissipation and efficiency excluding the optical receiver are represented for reasonable comparison with the others.
[c]18 km of transmission distance is estimation value from 2.7 dB of single-mode fibre loss with 0.15 dB/km of average loss.
[d][7] and [9] are describing serial-link transceivers. Therefore their power efficiencies are presented excluding transmitter side.

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3.5 ps/3.67 ps of RMS jitters and 29.51 ps/27.72 ps of peak-to-peak jitters, respectively. Clear eye openings are observed at 1.5625 and 1.32 Gb/s de-serialised data at TP3 with 200 mVp-p single-ended swing, as shown in Fig. 18.

Performance summary and comparison with previously reported receivers are given in Table 3. Our receiver is capable of handling high data rates even though it is realised with 0.18 μm CMOS technology. Furthermore, it has the highest integration level compared with previous reported CMOS receivers. However, the core chip area is larger for our receiver as we used the LC-VCO.

4 Conclusions

We demonstrate a fully integrated serial-link receiver with optical interface for long-haul display interconnects in 0.18 μm CMOS technology. In order to satisfy the requirements of our application, multi-rate (5.28, 5.6 and 6.25 Gb/s) dual-loop CDR is used. Our receiver has a high integration level and it can successfully convert the maximum 6.25 Gb/s optical data into 64-bit wide electrical signals. We expect that recently reporting silicon-based avalanche or p–i–n PD [22] can be included in future integration to have more cost-efficient serial link.

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Author Queries

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Q1 Please provide expansion for UXGA, WUXGA, NRZ, PVT and BBPDs.

Q2 Please check and confirm the main captions of Figs. 3, 10 and 14.