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A 5.28-Gb/s serializer ASIC for uncompressed long-haul multimedia interconnects

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Abstract We report a 5.28-Gb/s serializer ASIC for uncompressed long-haul video interconnects. Our ASIC is based on the serializer architecture which maintains the constant output data rate for various resolutions of incoming video signals from VGA to UXGA. With this, a wide-band phase-locked-loop in a serializer and a continuous-rate clock-and-data-recovery circuit in a de-serializer are not necessary. The serializer ASIC contains clock-and-data-recovery circuits, de-multiplexers, a digital processing block, a phase-locked-loop, multiplexers. A VCSEL driver circuit is also integrated so that it can be used for long-haul transmission with multimode fiber. The ASIC produces 5.28-Gb/s serialized driving currents for VCSEL from parallel input signals. It occupies 3.45 mm^2 and consumes 151.7 mW.

Keywords Serializer · Stationary-data-rate · HDMI · Phase-locked-loop · Clock-and-data-recovery · VCSEL driver

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1 Introduction

There is a great interest in high-definition (HD) video technology. As the required transmission data rates for video technology become higher, interconnects for video signals are increasingly hard to implement. Especially, long-haul applications such as HD closed-circuit televisions, large outdoor electronic displays, and interconnects have difficulties for connection with existing copper-based cables. Optical interconnects based on a low-cost 850 nm vertical cavity surface-emitting laser (VCSEL) and multimode fiber (MMF) are receiving great attention for uncompressed long-haul video interconnect applications.

High-definition multimedia interface (HDMI) is the well-known standard for uncompressed and high-quality video interconnects. Its transmission channels consist of three data channels and one clock channel having one tenth frequency of the data channels [1]. Therefore four separate optical links including four VCSELs, photodiodes (PDs), VCSEL drivers, optical receivers, and optical fibers are required for HDMI optical transmission, making the total system complex. To reduce the complexity, coarse wavelength division multiplexing (CWDM) technique has been adopted for HDMI interconnect [2]. Although the CWDM-based HDMI interconnect has only one optical link, it requires additional lens and optical filters as well as four pairs of VCSELs and PDs. A better approach is using an electronic serializer and de-serializer (SERDES) as shown in Fig. 1. In this paper, we report a 5.28-Gb/s serializer ASIC for uncompressed long-haul HDMI optical interconnects. This paper is organized as follows. Circuit and system description of the serializer ASIC is presented in Sect. 2. Section 3 explains chip implementation and measurement results, and conclusions are given in Sect. 4.

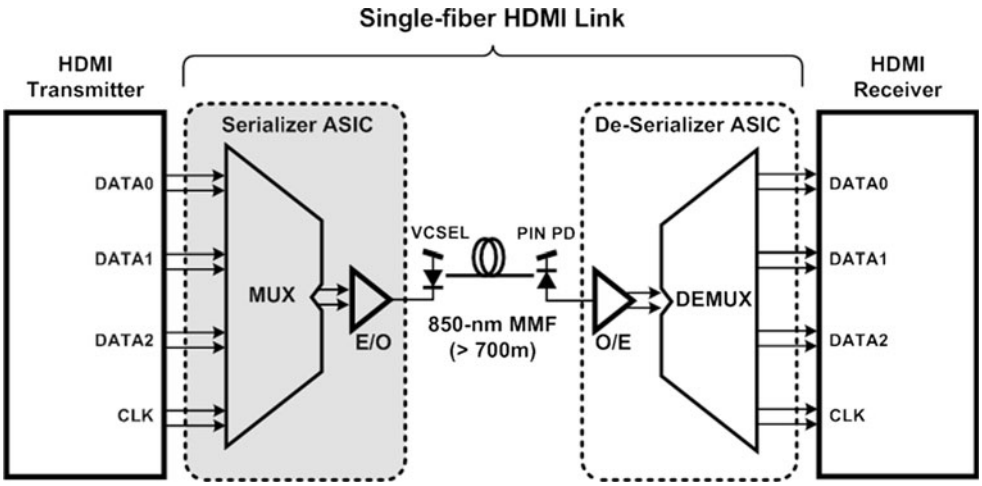


Fig. 1 Single-fiber HDMI interconnect for long-haul applications using an electronic SERDES

Table 1 Data throughput for popular display standards

Resolutions	Raw data throughput [Mb/s][a]	TMDS data throughput [Mb/s][b]	TMDS data throughput w/ overhead [Mb/s][c]
VGA (640 × 480)	442	251.75 × 3ch	805.6
SVGA (800 × 600)	691	400 × 3ch	1,280
XGA (1024 × 768)	1,132	650 × 3ch	2,080
SXGA (1280 × 1024)	1,887	1,080 × 3ch	3,456
UXGA (1600 × 1200)	2,764	1,620 × 3ch	5,184

[a] Calculated assuming follow conditions: color depth = 24 bit (each red, green, and blue have 8 bit), frame rate = 60 Hz

[b] 70–75 % of encoding overhead added to raw data

[c] 4-bit header per 60-bit wide data added

2 Serializer ASIC description

The uncompressed multimedia transmission is usually required in applications using flat panel displays (FPDs) larger than ten inches. According to the Video Electronics Standards Association (VESA), FPD resolution has different standards ranging from VGA to UXGA. Resolutions and data throughput for popular standards are summarized in Table 1 [3]. HDMI uses TMDS (transition minimized differential signaling) channel coding scheme which requires 70–75 % overheads over the raw video data. Since three TMDS signals are serialized into one in our serializer, the range of the serial data rate is 750–4,860 Mb/s. In order to handle this wide range, a wide-band phase-locked-loop (PLL) and a continuous-rate clock-and-data-recovery (CDR) are required, both of which are difficult to realize. Instead, we adapt the stationary-data-rate scheme in which all the display data are always serialized into 5.28 Gb/s data and one SERDES handles the data with the fixed data rate of 5.28 Gb/s.

Our serializer architecture is shown in Fig. 2. It is composed of three CDRs, a digital processing block, 64:1 MUX, 5.28-GHz LC-type PLL, and VCSEL driver. To cover the entire TMDS input data rates from 250 to 1,620 Mb/s, three ring-PLL-based CDRs with a programmable divider are used. Each input data stream is de-multiplexed to 20-bit wide data for digital processing, resulting in 60-bit wide parallel data with recovered clock (TCLK2). The digital processing block is composed of a data alignment block, a range detector, a dummy encoder, a first-in first-out (FIFO), a header-bit encoder, and a scrambler. The range detector senses the input data rate, and controls the programmable divider of the CDRs and the dummy encoder. The FIFO and the header encoder are critical blocks for realizing the stationary-data-rate scheme. The FIFO converts TMDS data rate into the stationary data rate. The header encoder generates 4-bit header that indicates 60-bit wide data are real or dummy. The scrambler ensures DC balance and data transition density of input data for data recovery of the de-serializer. After digital processing, 64-bit wide parallel data are serialized into one differential data with 5.28 GHz clock. Then, the VCSEL driver produces 5.28-Gb/s modulation currents for an off-chip VCSEL.

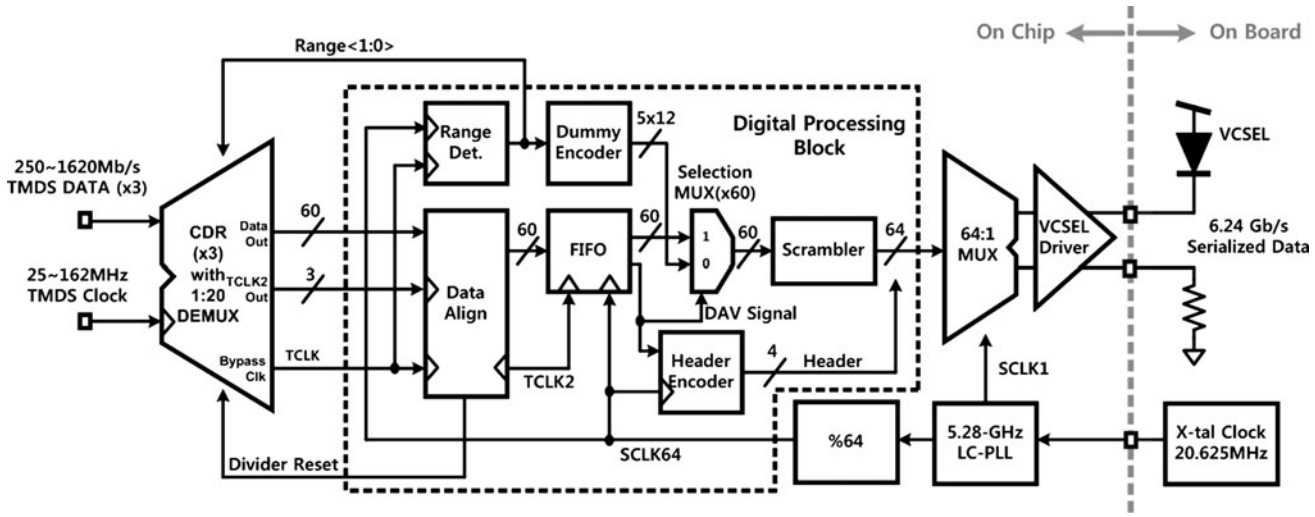


Fig. 2 Serializer ASIC architecture

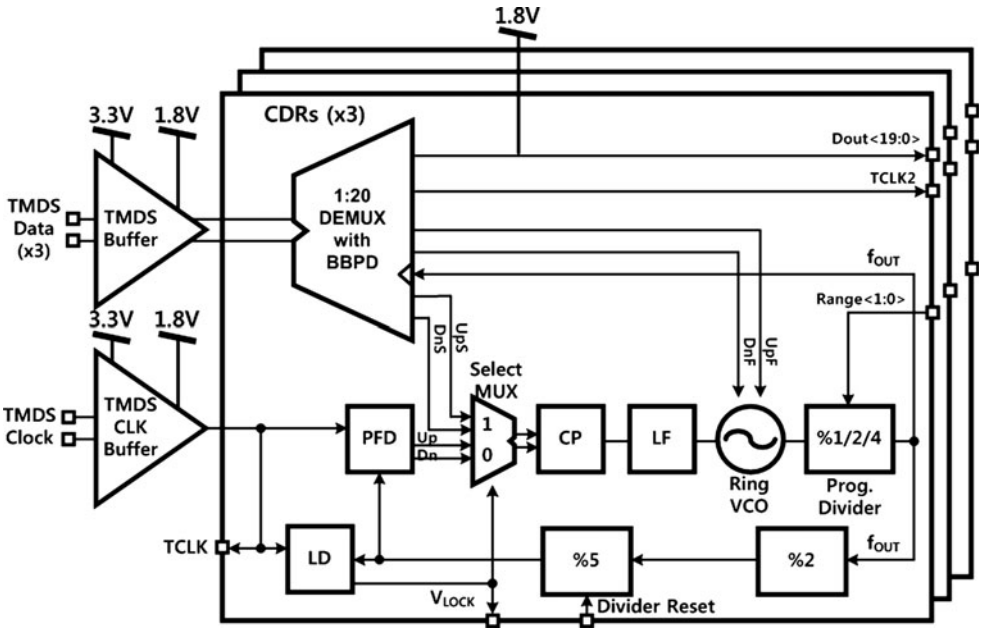


Fig. 3 Block diagram of wide-range ring-PLL-based dual-loop CDRs

2.1 Input buffer and clock-and-data-recovery circuits

Figure 3 shows block diagram of ring-PLL-based dual-loop CDR circuits. HDMI buffer with 3.3 V supply is located in front of the serializer ASIC. Therefore 3.3 V pull-up signals delivered to the serializer ASIC have to be converted into 1.8 V CML signals. In addition, differential TMDS clock should be changed into CMOS logic which can be used as input to phase-frequency detector (PFD) and lock detector (LD).

Each lane of TMDS data is parallelized to 20-bit wide data for digital processing. Since TMDS clock has one tenth frequency of TMDS data, it cannot be used as a clock for the DEMUX. Therefore CDR circuit is necessary for clock extraction from TMDS data. TMDS clock is used as a reference clock in these CDRs. Each CDR circuit consists of 1:20 DEMUX with bang-bang phase detector (BBPD) and PLL. To cover input data from 250 to 1,620 Mb/s, a programmable divider is used. The programmable divider is controlled by 2-bit range codes (Range$\langle 1:0 \rangle$) from the range detector of the digital processing block. The ring-type voltage-controlled oscillator (VCO) is used for achieving a wide locking range from 0.9 to 1.8 GHz. For the lowest data rate of 250 Mb/s, the VCO locks to 1 GHz with dividing factor of four, while for the highest data rate of 1.62 Gb/s, the VCO locks to 1.62 GHz with dividing

factor of one. The dual-loop structure and a bang-bang phase detector (BBPD) provide fast locking. The dual loop consists of a PLL loop and a phase alignment loop with BBPD. Initially, output frequency of the VCO (f_{OUT}) locks to the reference frequency (TCLK) with an appropriate dividing factor. Once f_{OUT} is adjusted to the right value by the PLL loop, LD generates a lock signal (V_{LOCK}). V_{LOCK} turns the PFD off and the BBPD on through select MUX. A full-rate BBPD is adopted to improve the jitter performance and reduce the locking time. The BBPD generates slow and fast bang-bang signals. Slow bang-bang signals (UpS and DnS) control f_{OUT} through a charge pump (CP), while fast bang-bang signals (UpF and DnF) directly control delay cells of the ring VCO. By separating the BBPD control path, the feedback-loop latency can be reduced and the bandwidth requirement for the CP can be relaxed [4].

2.2 Digital processing blocks for the stationary-data-rate scheme

To realize the stationary-data-rate scheme, there are two clock domains in our serializer ASIC. One is based on 250–1,620 Mb/s TMDS data, namely T-domain, and the other is based on 5.28-Gb/s stationary data, namely S-domain. TMDS clock comes from an external HDMI transmitter while 5.28-GHz clock is based on an external crystal oscillator having 20.625-MHz frequency. We use prefixes T- and S- for the clocks related to the each domain.

Figure 4 shows the digital processing blocks for the stationary-data-rate scheme. Parallelized three 20-bit wide data and three output clocks of CDRs (TCLK2) have no phase relationship. Therefore data alignment is necessary. Data alignment block looks for rising edges of TCLK2 near the alignment clock, as shown in Fig. 5. When the rising

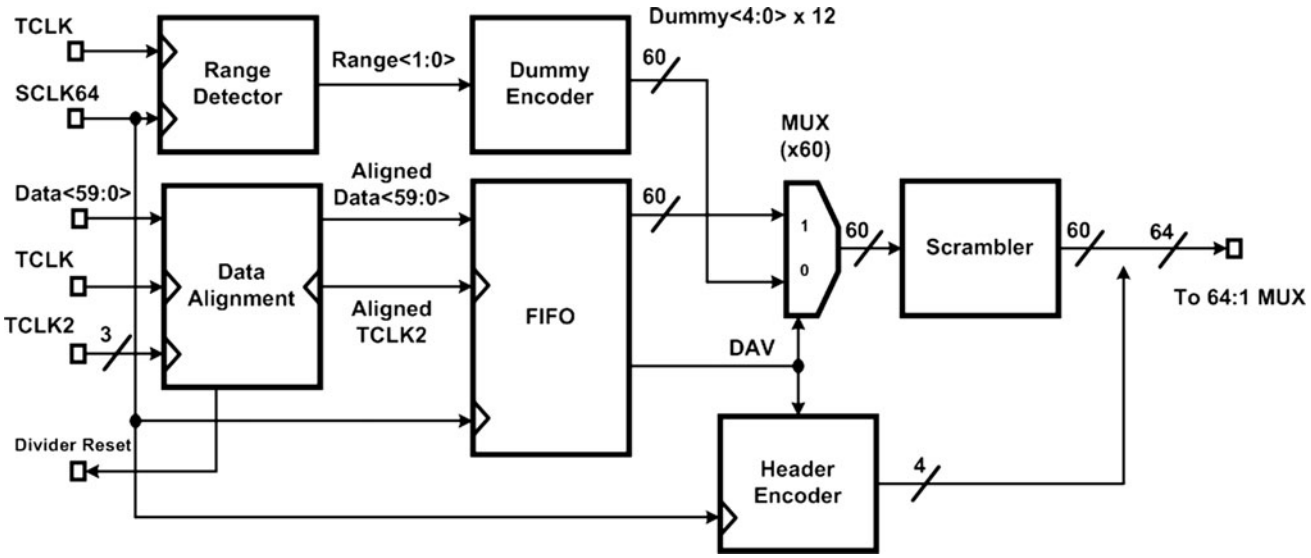
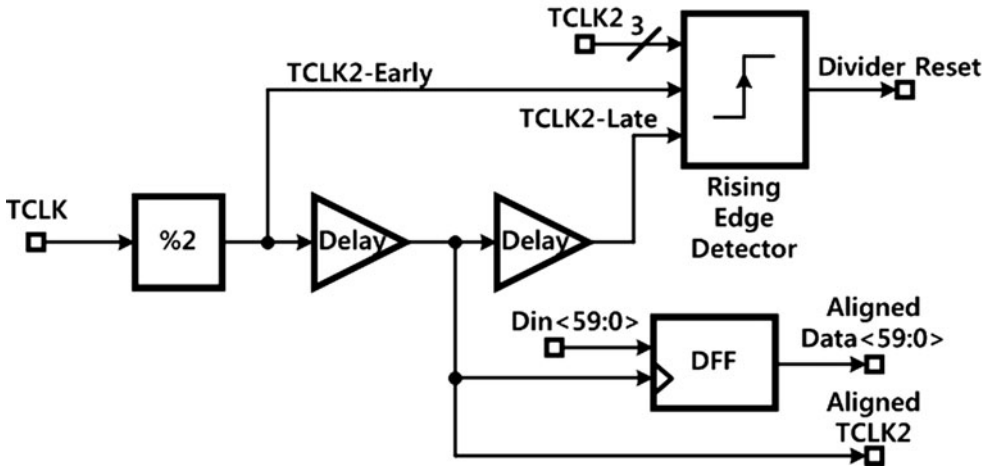


Fig. 4 Digital processing blocks for the stationary-data-rate scheme

Fig. 5 Data alignment block



edge is detected, all three frequency dividers for CDRs are reset to guarantee the phase relationship. These aligned T-domain data having 12.5–81 Mb/s data rate should be converted into 60-bit wide S-domain data having fixed 82.5 Mb/s data rate (frame rate) with 4-bit header. We call 64-bit wide parallel data one frame. 12.5–81 Mb/s data experience an underflow compared with the 82.5 Mb/s data. By filling out dummy data to these empty timing slots, we can get 64-bit wide data having stationary 82.5 Mb/s data rate for the wide-range TMDS data. Data valid (DAV) signal indicates how much underflow the incoming data have. DAV signal generated by the FIFO is only high when that timing slot is filled out by real data. DAV ratio is defined as the ratio of the real timing slots compared with total time and can be expressed as follows:

$$(DAV\ Ratio) = \frac{(TMDS\ Data\ Rate)/20}{(Stationary\ Frame\ Rate)} \quad (1)$$

If TMDS data rate is 412.5 Mb/s, then DAV ratio is 1/4, as shown in Fig. 6. DAV signal is also exploited as a select signal for the MUX. If DAV signal is low, then that frame is filled by dummy data coming from the dummy encoder. The header encoder generates 4-bit header, 1100 or 0011 according to the DAV signal. Meanwhile, S-domain 60-bit wide data is encoded to 2^{15}-1 PRBS data by 4-parallel 15-wide scramblers.

The FIFO converts T-domain 60-bit wide data into S-domain data, and generates DAV signal by comparing TCLK2 (TMDS clock divided by 2) with SCLK64 (5.28GHz clock divided by 64). Fig. 7 shows the detail FIFO blocks. The FIFO consists of 6-state Gray code counter (GCC) with enable function, one hot encoder (OHE), FIFO unit, and data-valid (DAV) generator. The first GCC generates 6-state Gray codes according to the rising edge of TCLK2 and OHE generates write pointer signals, as shown in Table 2. The first GCC is always enabled. The second GCC operates at the rising edge of SCLK64 and uses DAV signals as an enable signal. The first GCC output is retimed with SCLK64 through three D flip flops (DFFs) and these Gray codes are also converted into one-hot-codes for DAV generator. 6-bit one-hot-codes are used as read and write pointers of 6×60 FIFO units, as shown in an inset of Fig. 7. 60-bit input data are written to the FIFO with TCLK2 and the write pointer, and data are only read when read pointer is high. The read pointers have information on DAV ratio. Therefore, FIFO outputs are synchronized to SCLK64. Measured DAV signals according to the video resolutions are shown in Fig. 8, and the results are summarized in Table 3.

The range detector compares TCLK20 (TMDS clock) with SCLK64, and generates range codes. The range codes (Range$\langle 1:0 \rangle$) according to the TMDS data rates indicate in an inset table of Fig. 9. We separate TMDS data ranges into three octave parts, Range-0, Range-1, and Range-2. To prevent metastability near the boundaries between three parts, each boundary has four specific values that are overlapped. The outer boundaries are used when three CDRs are locked, and vice versa. According to the range codes, certain dummy data are selected in the dummy encoder. With these information, the de-serializer ASIC can detect the TMDS range in the receiver.

2.3 64:1 MUX with LC-PLL

The serializer jitter performance affects system bit-error-rate (BER) and the de-serializer sensitivity. For better jitter performance, LC-type PLL is used in the output data path.

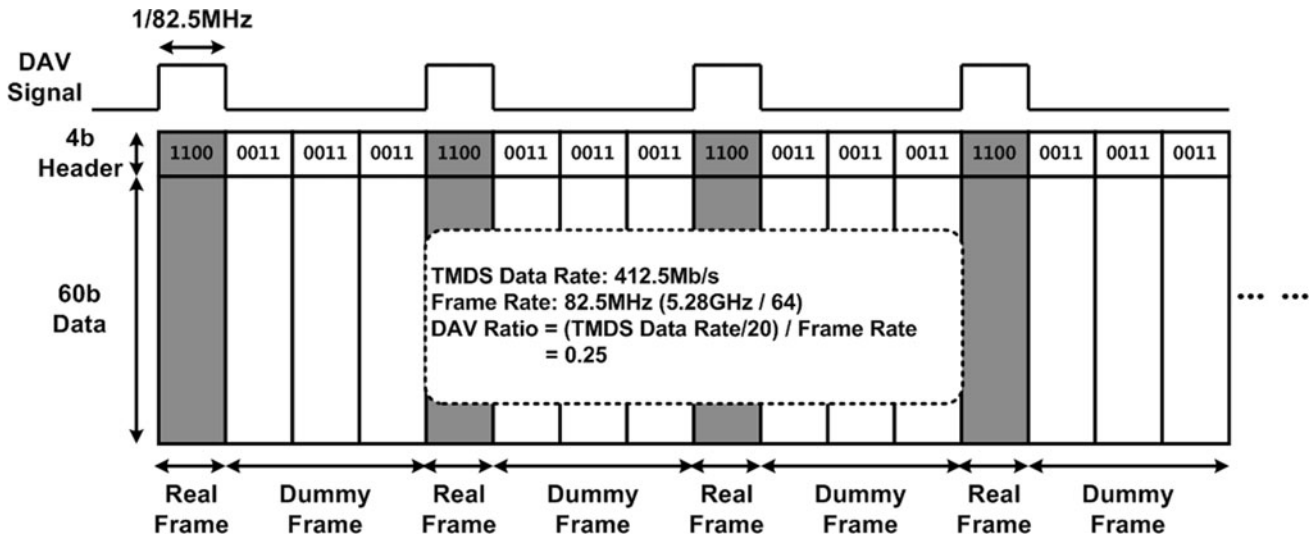


Fig. 6 Frame-based real and dummy frame diagram with DAV signal

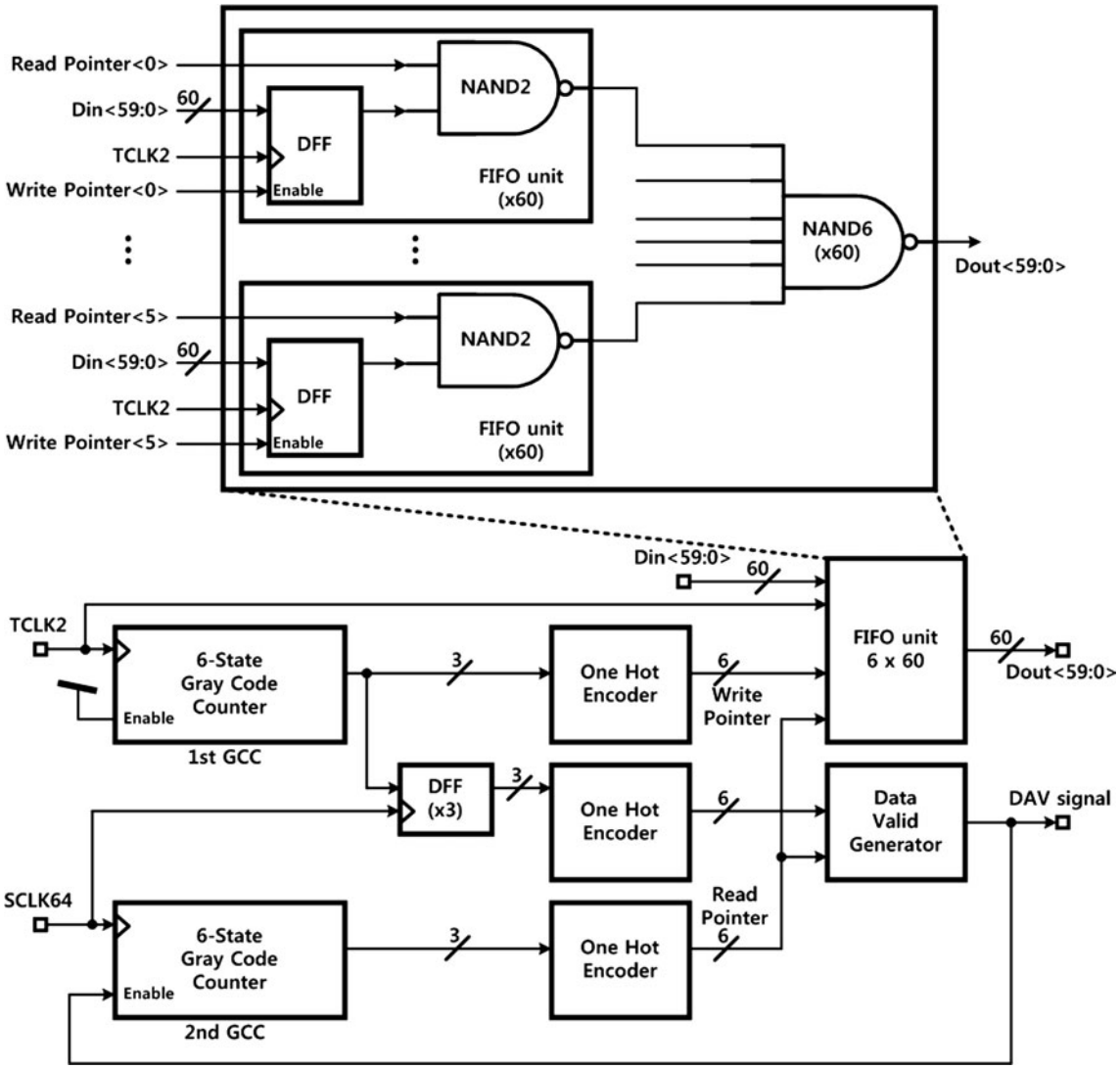


Fig. 7 Block diagram of the FIFO

Table 2 Truth table of the one hot encoder

6-State gray code output$\langle 2:0\rangle$	One hot encoder output$\langle 5:0\rangle$
000	001000
001	010000
011	100000
111	000001
110	000010
100	000100

Block diagrams for LC-PLL and 64:1 MUX are shown in Fig. 10. 64:8 and 8:4 MUXs are realized with CMOS logic, while 4:1 high-speed MUX uses CML logic. 64:8 MUX is implemented with the shift-register architecture for chip area reduction, while other MUXs are based on the tree structure for power reduction [5]. For testing 64:1 MUX with LC-PLL, 64-bit wide parallel pseudo-random bit stream 2^7-1 (PRBS7) generator is integrated in front of 64:8 MUX. By using an enable signal, 64-bit parallel inputs are selected to either data streams (DIN$\langle 63:0\rangle$) from digital processing block or PRBS7 data. The LC VCO exploits N-core switching transistors and a center-tap spiral inductor (1.15 nH). And the locking range is from 5.15 to 5.45 GHz with 1.4 V range of tuning voltage. The gain of LC-VCO is about 214 MHz/V.

2.4 VCSEL driver

A stand-alone VCSEL driver usually consists of an input buffer for electrical interface, a pre driver, and a main driver. The pre driver plays a role of driving the large switching transistors of the main driver. However, we can

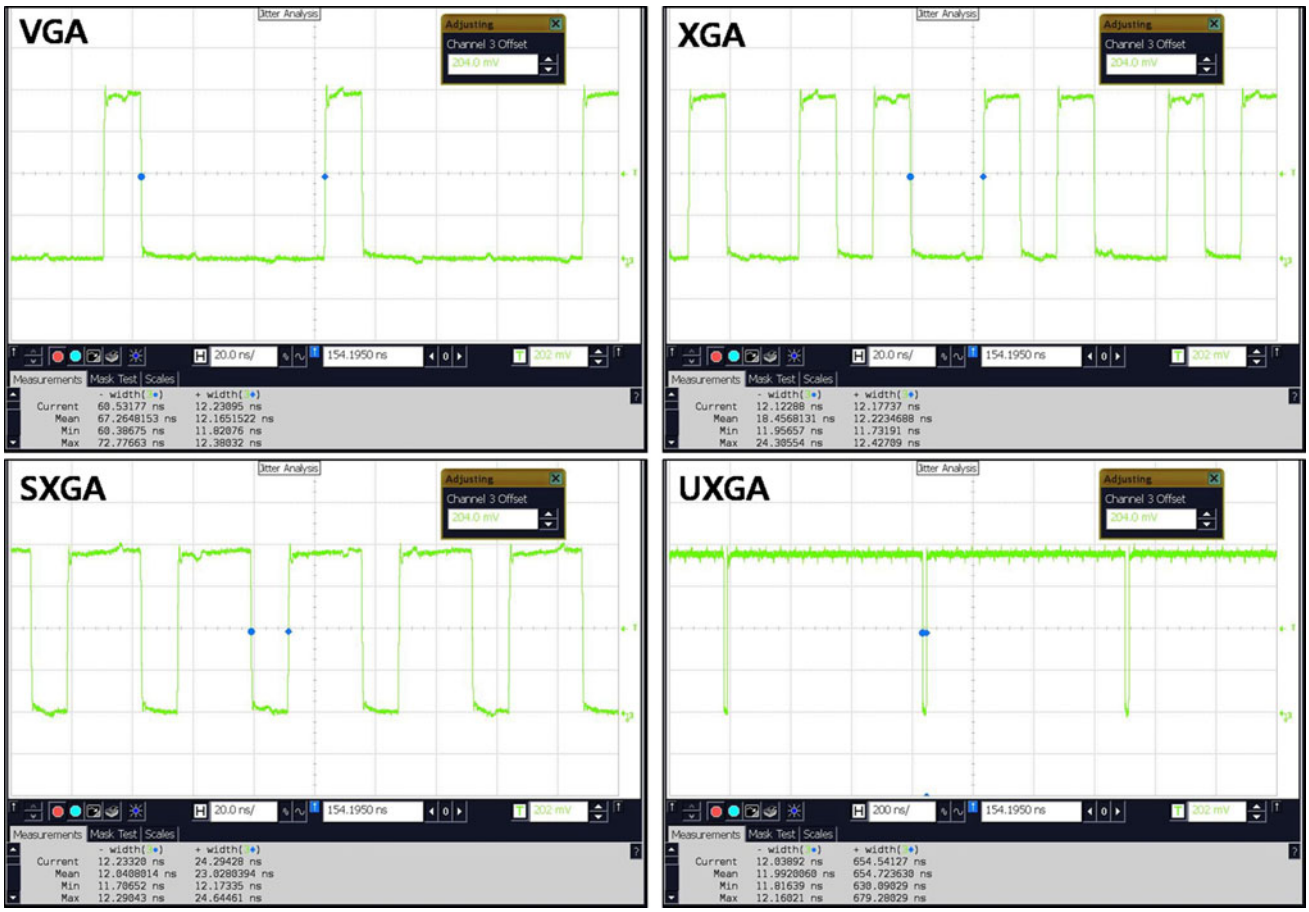


Fig. 8 Measured DAV signals according to the video resolutions

Table 3 Calculated and measured DAV ratio according to the TMDS data rates

TMDS data rates (Mb/s)	TCLK2 (MHz)	DAV ratio (Calc.)	Average time (DAV = 1) (Mea.)	Average time (DAV = 0) (Mea.)	DAV ratio (Mea.)
251.75 (VGA)	12.5875	~0.15	12.165 ns	67.265 ns	~0.15
400 (SVGA)	20	~0.24	12.189 ns	37.610 ns	~0.24
650 (XGA)	32.5	~0.39	12.223 ns	18.457 ns	~0.39
1,080 (SXGA)	54	~0.65	23.028 ns	12.041 ns	~0.65
1,620 (UXGA)	81	~0.98	654.724 ns	11.992 ns	~0.98

omit the input buffer and the pre driver. At the end of the 64:1 MUX, the CML buffer is designed to have a sufficient driving capacity. To compensate VCSEL variations due to temperature variations and aging, threshold current (I_{TH}) and modulation current (I_{MOD}) of VCSEL should be controlled [6]. External control bits for both currents are added for testing. Fig. 11 shows a block diagram of the main driver. The ITH and IMOD can respectively be controlled from 1 to 2.5 mA and from 5 to 20 mA to meet the specification of commercial VCSEL [7]. A commercial VCSEL is mounted on a printed-circuit board for testing.

3 Chip implementation and measurement results

A 5.28-Gb/s serializer ASIC is implemented with 0.18 μm CMOS technology. Figure 12 shows a microphotograph of the chip which occupies the area of 1.75 mm by 1.97 mm including electrostatic discharge (ESD) protection diodes and bonding pads. The serializer consumes 52.4 mA from a regulated 1.8 V supply, 6.4 mA at a 3.3 V supply, and 11 mA for driving an external VCSEL with 3.3 V forward bias voltage, corresponding to 151.7 mW for total power consumption. Figure 13 shows the measurement setup.

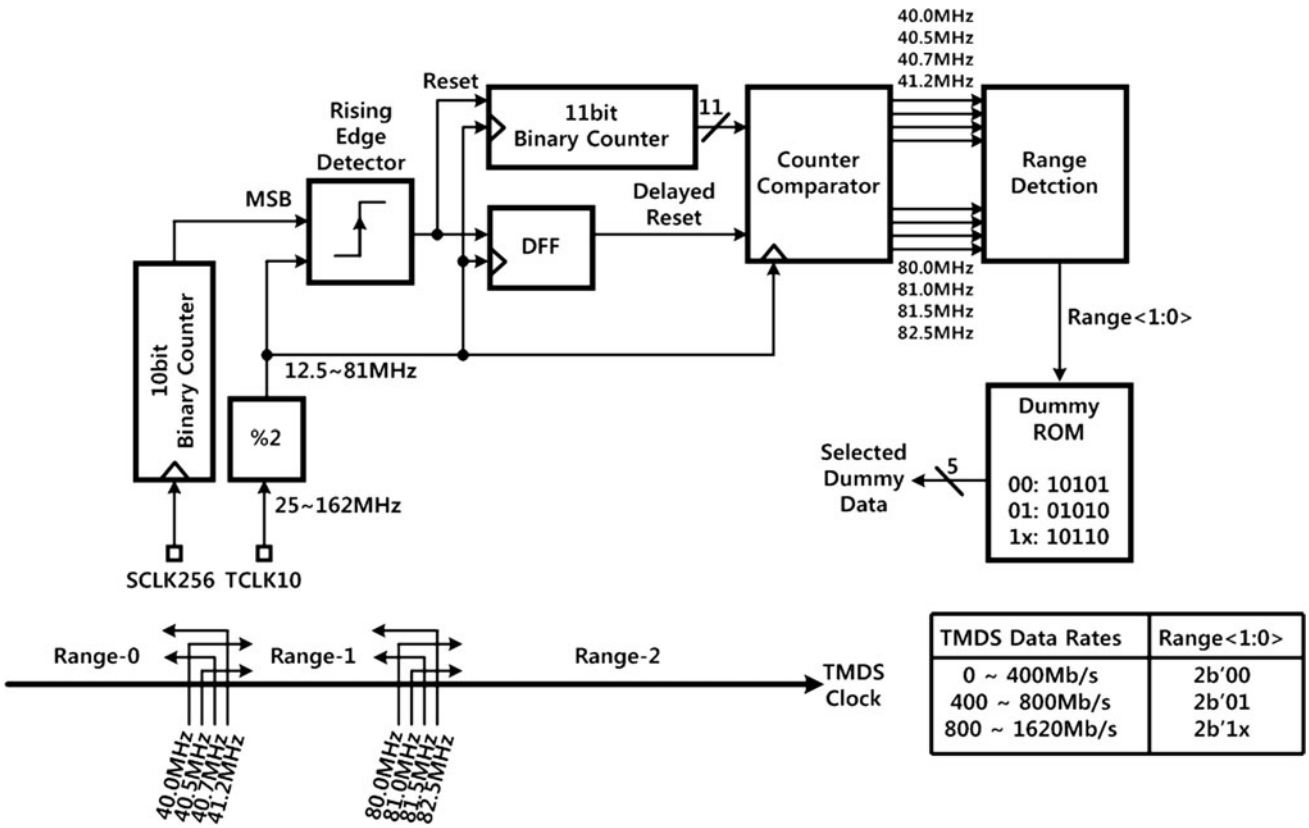


Fig. 9 Block diagram of the range detector

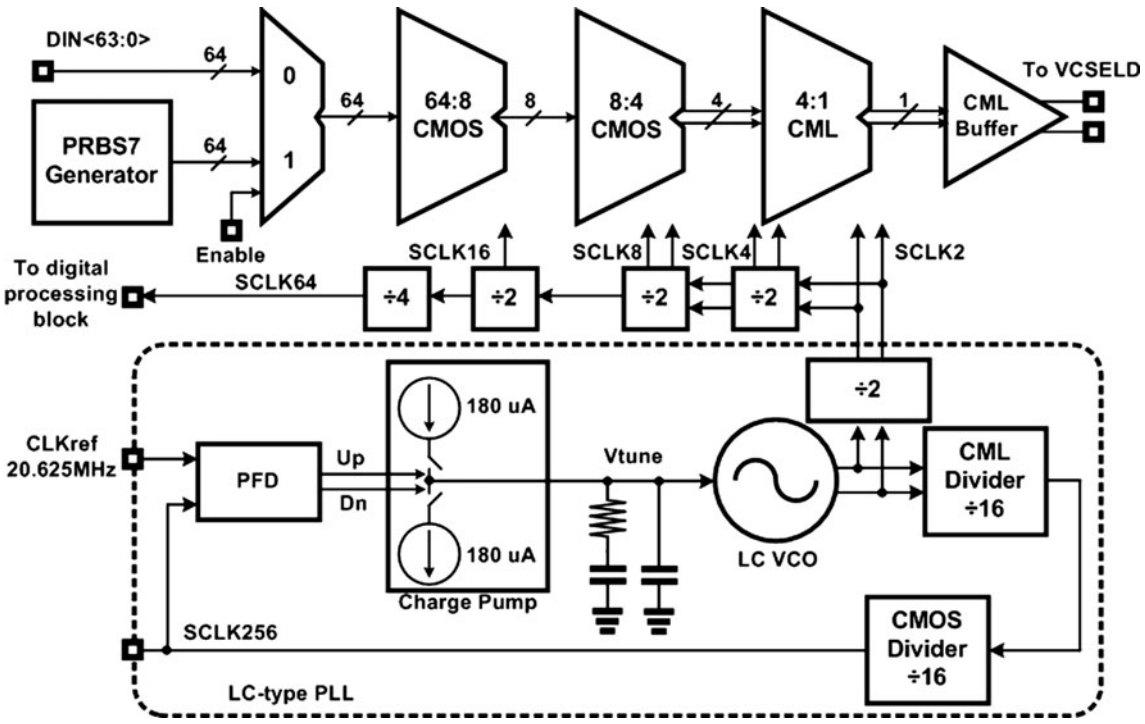


Fig. 10 Block diagram of LC-PLL

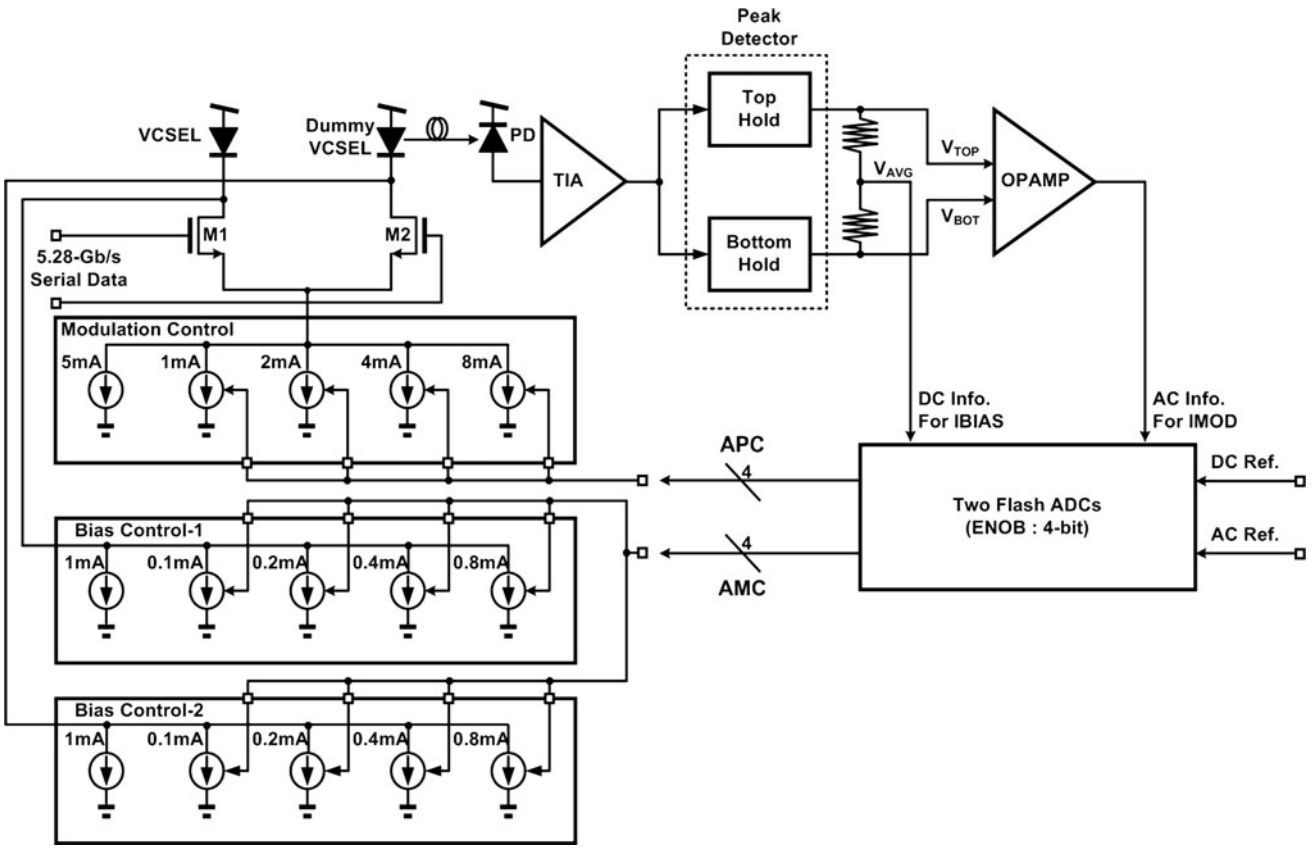


Fig. 11 Block diagram of VCSEL driver with APC and AMC

The serializer is mounted with a commercial VCSEL on a printed-circuit board. The VCSEL operates at 850 nm of center wavelength and exhibits 8 GHz of 3 dB bandwidth. It requires 1 mA of threshold current, and 10 mA of modulation current for −4 dBm of optical power. A video signal generator creates three TMDS data and synchronized TMDS clock. The output of 64:1 serializer (Test Point-1) is connected to the bonding pad through CML buffer for testing. A function generator is used instead of a crystal oscillator to generate a 20.625-MHz reference clock. 700-m MMF, a commercial optical receiver module with −20 dBm of optical sensitivity and 10 GHz of 3 dB bandwidth, and a sampling oscilloscope were used for the test. In front of the integrated VCSEL driver (Test Point-1), the serial data exhibits peak-to-peak jitter of 29.8 ps and RMS jitter of 4.97 ps, as shown in Fig. 14(a). After 700 m MMF and 10 Gb/s commercial O/E module (Test Point-2), received data have peak-to-peak jitter of 75.0 ps and RMS jitter of 12.5 ps, as shown in Fig. 14(b). The measured optical power in front of the optical receiver is −9 dBm and no bit error is observed at the 5.28 Gb/s.

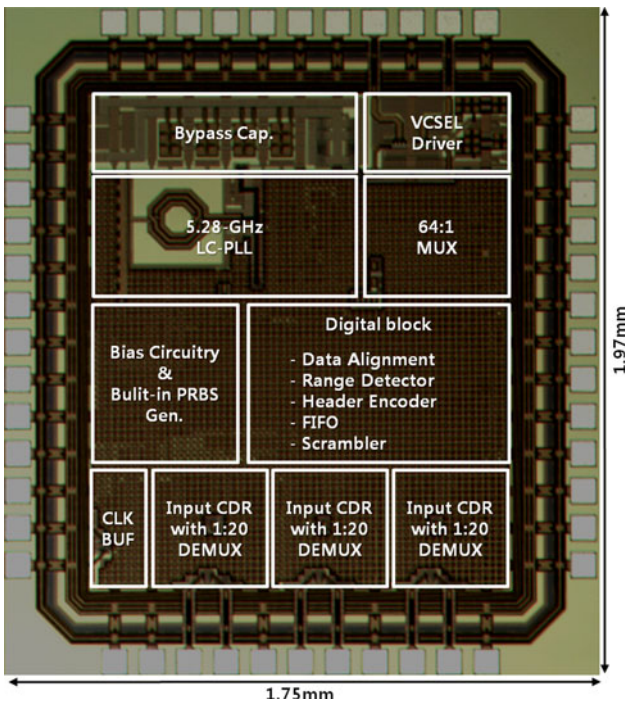
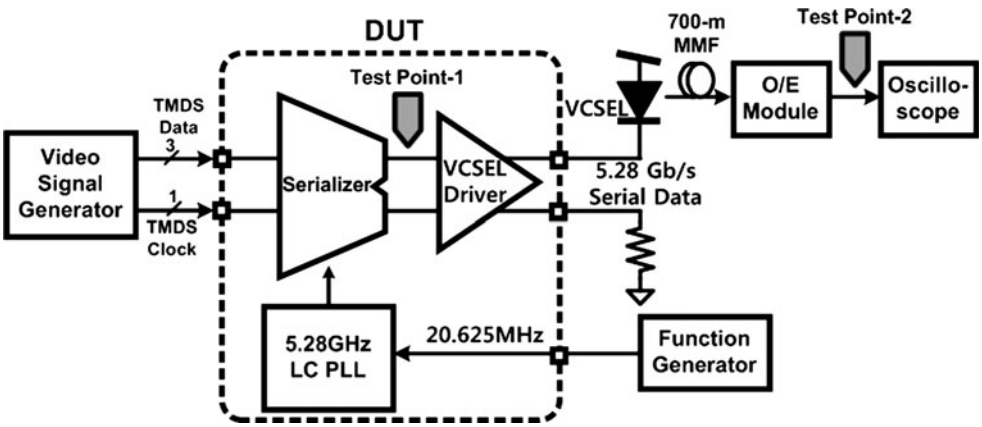


Fig. 12 Chip micophotograph



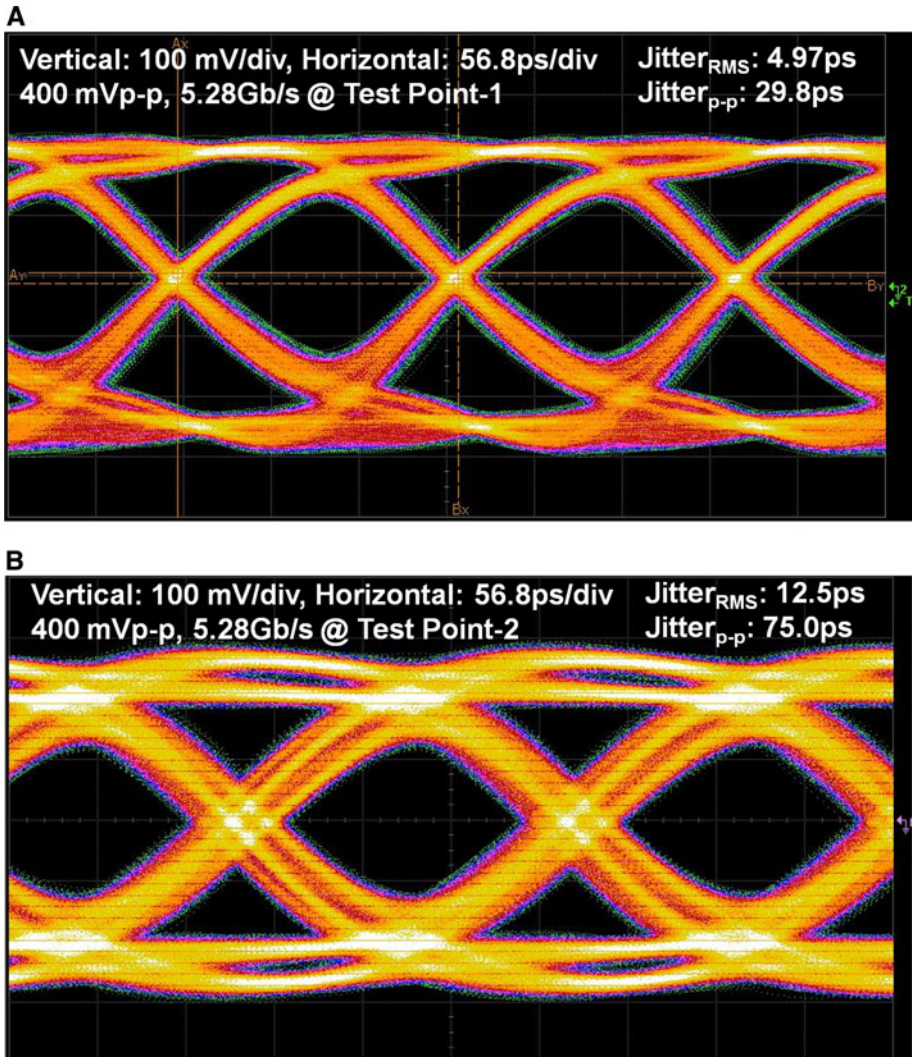


Fig. 13 Measurement setup

Fig. 14 Measured eye diagrams at **a** Test Point-1 and **b** Test Point-2

4 Conclusions

A 5.28 Gb/s serializer ASIC for uncompressed long-haul video interconnect application is realized in 0.18 μm CMOS technology. The serial ASIC employs the stationary-data-rate scheme and can handle the wide range of video standards from VGA to WUXGA. It also contains a VCSEL driver so that it can be sued for the single-channel long-haul optical HDMI

link. This serializer ASIC can provide a cost-effective solution for long-haul serial uncompressed video transmission.

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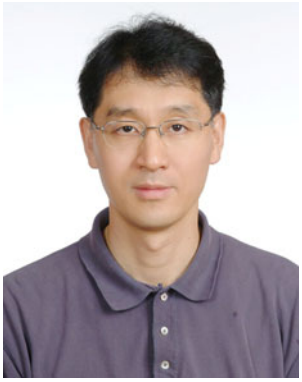

Woo-Young Choi received his B.S., M.S. and Ph.D. degrees all in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology. For his Ph.D. thesis, he investigated MBE-grown InGaAlAs laser diodes for fiber optic applications. From 1994 to 1995, he was a post-doctoral research fellow at NTT Opto-electronics Labs., where he worked on femtosecond all- optical switching devices based on low-temperature-grown InGaAlAs quantum wells. In 1995, he joined the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea, where he is presently a professor. His research interest is in the area of high-speed information processing technology that includes high-speed optoelectronics, high-speed electronic circuits, and microwave photonics.