ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.4, 1–8

A 10-Gb/s low-power adaptive continuous-time linear equalizer using asynchronous under-sampling histogram

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Abstract: This paper presents a 10-Gb/s low-power adaptive continuous-time linear equalizer, which automatically determines the optimal equalization condition by searching for the equalization coefficient producing the largest peak value in histograms obtained with asynchronous under-sampling. To reduce the power consumption, the integrated digital controller turns off the circuit blocks used for the adaptation process once adaptation is complete. A prototype equalizer realized in 65-nm CMOS technology consumes 4.66 mW during adaptation and 2.49 mW after adaptation. For 10-Gb/s $2^{31}-1$ PRBS data transmitted over 40-cm FR4 PCB trace, our equalizer achieves less than 10^{-13} BER and 26.6 ps peak-to-peak jitter.

Keywords: low-power adaptive equalizer, continuous-time linear equalizer (CTLE), asynchronous under-sampling histogram

Classification: Integrated circuits

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DOI: 10.1587/elex.10.20130030
Received January 15, 2013
Accepted January 24, 2013
Published February 18, 2013

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1. Introduction

As the required data rate for wire-line communication increases, channel bandwidth limitation becomes a critical problem as inter-symbol interference (ISI) due to high-frequency channel loss greatly degrades the transmission performance. In order to compensate this, an equalizer is essential in high-speed serial links. In addition, adaptive equalization is required so that the equalizer can properly work even with channel condition variations and process-voltage-temperature (PVT) variations.

In high-speed serial link applications, the demand for power consumption reduction is becoming stronger. Various low-power adaptive equalizers have been reported. A tunable passive filter with power comparison adaptation can achieve low-power consumption but further improvement is required in input impedance matching and output swing levels [1]. Decision feedback equalizers (DFEs) have been used in low-power transceivers [2]. For DFEs, however, clock recovery and distribution circuits are required, making it difficult to use these equalizers if received data eyes are initially closed. Adaptive Continuous-Time Linear Equalizers (CTLEs) are widely used due to their simple architecture and good linearity [3, 4, 5, 6]. In addition, they do not require synchronous clock signals for their operation.

We have previously demonstrated a 5.4-Gb/s adaptive CTLE based on asynchronous under-sampling histograms [7]. Our adaptation algorithm is based on the simple observation that the clearest eye diagram produces the largest peak value in the histogram of received data amplitudes. Our CLTE scans all possible equalization coefficients and selects the one that produces a histogram having the largest peak value as the optimal equalization coefficient.

In this paper, we report a 10-Gb/s low-power adaptive CTLE based on the same adaptation technique. We achieve low-power operation by turning off the circuit blocks used for adaptation after adaptation is accomplished. This paper is organized as follows. After introduction in Section 1, Section 2 describes details of circuit implementation and Section 3 gives measurement results. Conclusion is given in Section 4.

2. Circuit implementation

Our design goal is 10-Gb/s data transmission over 40-cm FR4 PCB trace with low power consumption. The minimum power consumption of analog circuits is basically determined by the supply voltage, the signal peak-to-peak amplitude and the required bandwidth. We set 250-mV peak-to-peak swing from 1-V supply as our design specification. Current-mode logic circuits are designed with small-size input pairs using low threshold voltage transistors for improvement in both power dissipation and circuit speed. Passive inductors are not used in order to reduce the silicon area.

DOI: 10.1587/elex.10.20130030
Received January 15, 2013
Accepted January 24, 2013
Published February 18, 2013

The target channel has 10.48 dB loss at 5 GHz. Our adaptive CTLE is designed to have up to 15 dB equalizing gain at 5 GHz. Fig. 1 shows the overall configuration of the proposed low-power adaptive CTLE. It has a 3-bit variable CTLE filter, two unit-gain buffers, output buffers, a 4-phase clock divider, two digital-to-analog converters (DACs), four track-and-hold circuits, a clocked sense amplifier, and an integrated digital controller. The digital controller turns off the circuit blocks such as DACs, clocked sense amplifier, clock divider, and unit gain buffer with high threshold voltage transistor switches after the adaptation process is complete. Also, the dynamic power of a digital controller is reduced due to operating clock off.

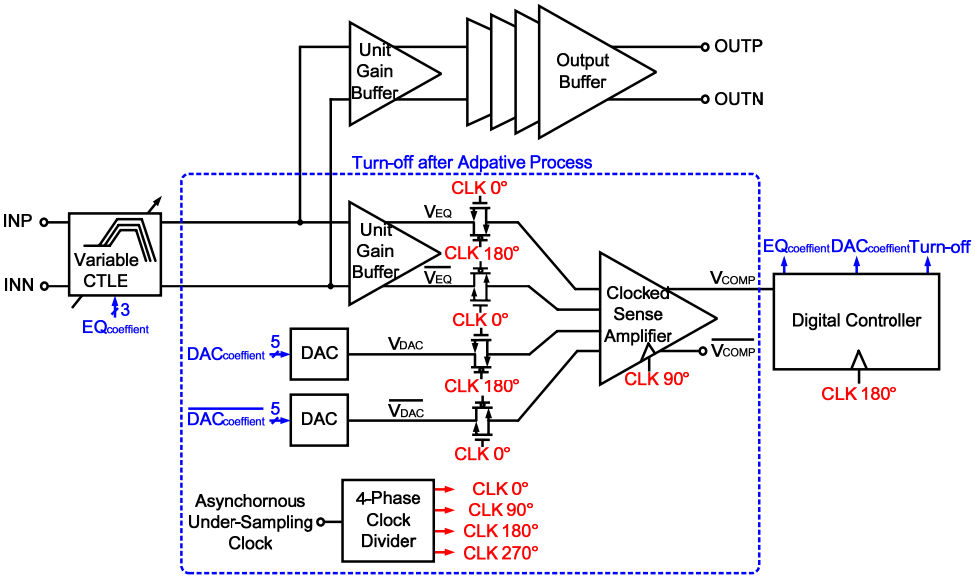

Fig. 1. Proposed low-power adaptive CTLE.

Table I compares performances of previously reported low-power CTLE filters. An active inductor technique with low voltage headroom provides area-efficient alternative for passive inductive terminations and offers channel loss compensation through tunable peaking, while consuming a small amount of overhead power. However, it cannot fulfill our design target due to limited boosting gains [4]. An interleaved active feedback topology incorporated with additional capacitive and resistive source

Table I. Performance comparison of the CTLE filters.

	ASSCC'08 [4]	TCASII'09 [5]	EL'09 [6]
Technology	90-nm CMOS	130-nm CMOS	130-nm CMOS
Filter type	Active inductor	Active feedback	Negative cap.
Data rate	10 Gb/s	10 Gb/s	10 Gb/s
Supply voltage	1 V	1.2 V	1.2 V
Power consumption	8.8 mW	14 mW	6 mW*

*: Including adaptation block

DOI: 10.1587/elex.10.20130030
Received January 15, 2013
Accepted January 24, 2013
Published February 18, 2013

degeneration achieves enough boosting gain and bandwidth extension. But several cascading gain cells with interleaved active feedback cells cannot satisfy power constraint [5]. A filter using capacitive source degeneration and negative capacitance circuits as shown in Fig. 2 provides enough high-frequency boosting without sacrificing DC gain and lowest power consumption [6]. The 2-stage filters are used for our design specification. With these filters, adaptation is achieved by tuning the zero of negative capacitor. Our CTLE is designed to have 4.5-dB to 15-dB equalizing gain with 3-bit capacitor array, which provides 8-different gain levels with approximately 1.5-dB increment controlled by 3-bit equalization coefficients. It guarantees uniform output swing despite changing equalization coefficient so that histogram is properly calculated with the fixed DAC resolution. On-chip 50-Ω resistors are integrated for input impedance matching.

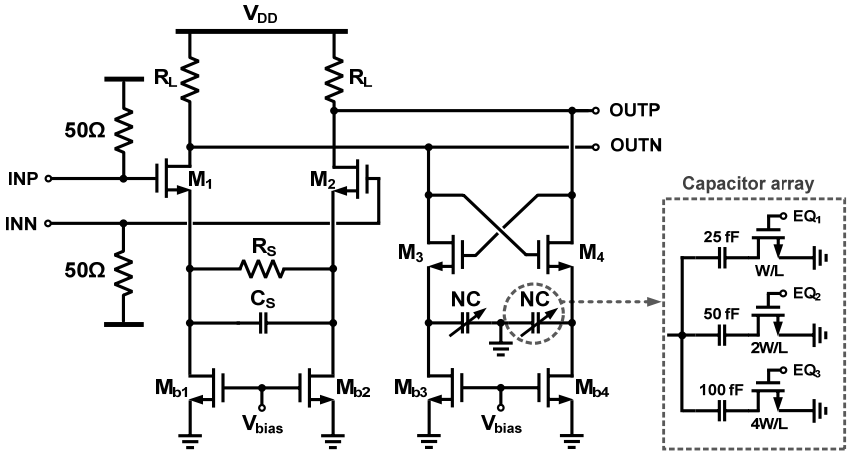

Fig. 2. The schematic of CTLE filter.

The track-and-hold circuit is made up of a pass-gate logic consisting of NMOS and PMOS switches. The unit gain buffer prevents CTLE output from clock feed-through of track-and-hold circuits. A 5-bit DAC generates 32-level reference voltages with 15.625 mV resolution. The reference level is controlled from 500 mV to 1 V by PMOS load switches with 5-bit DAC coefficients. The 4-input differentially clocked sense amplifier compares equalized data with DAC references. The clock divider provides 107-MHz quadrature clocks from external 214-MHz clock which are asynchronous to the target data rate. These quadrature sampling clocks are sequentially provided to track-and-hold circuits, the comparator, and the digital controller for stable operation.

The adaptive process in digital controller is shown in Fig. 3. Initially, a finite state machine (FSM) applies an equalization coefficient to the equalizing filter and the DAC coefficient to DAC. After that, a reference voltage, V_{DAC}, is applied to the comparator. When the signal level, V_{EQ}, is higher than V_{DAC} at the sampling point, a clocked sense amplifier generates a high pulse, V_{COMP}. A counter in FSM counts up by one and the register stores the accumulated value during 4096 samples. With a full scan of reference voltages, the resulting cumulative distribution function (CDF) for the given equalization coefficient is obtained. By differentiating the CDF, the probability density function (PDF) is obtained. The PDF values are stored in 32 registers. The maximum value selector detects the peak value

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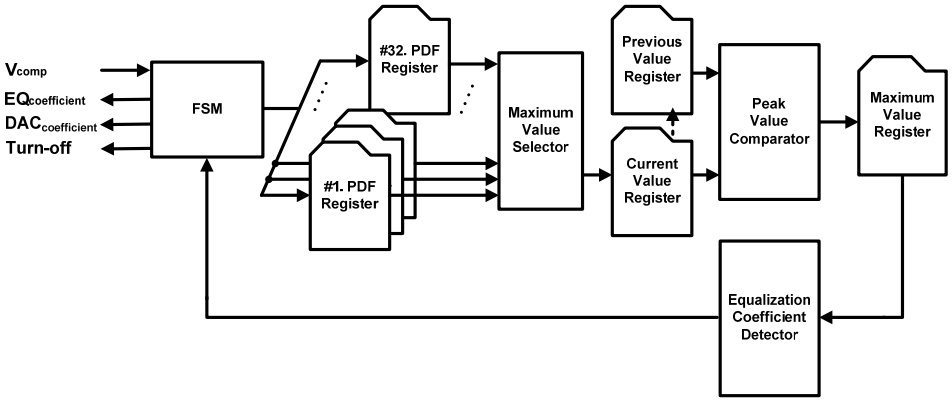

Fig. 3. The adaptive process in digital controller.

of the PDF. When the current peak value is higher than the previous peak value, the maximum value register stores the current equalization coefficient and previous value register is updated. This process is repeated for each of 8-equalization coefficients. The equalization coefficients detector determines the digital coefficient having the largest peak value and chooses this as the optimal equalization coefficient. After adaptation, the FSM turns off all the circuit blocks needed for adaptation so that power consumption can be minimized. They can be turned on again when demanded by a higher level control (not implemented) if there is any degradation in received data quality. With 4096 samples used for each histogram, the total time required for adaptation is estimated 9.8 ms.

3. Measurement results

Fig. 4 shows a die photograph of our adaptive CTLE chip fabricated in 65-nm CMOS technology. The core occupies 0.0386-mm^2 die area excluding output buffers.

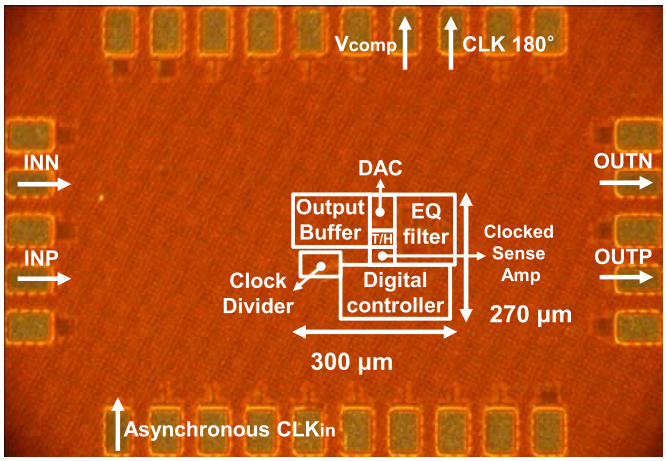

Fig. 4. Chip photograph of the designed adaptive CTLE.

Fig. 5 shows the measurement setup. A pulse pattern generator (PPG) provides differential 10-Gb/s $2^{31}-1$ pseudo random bit sequence (PRBS) data to the chip on a probe station through 40-cm FR4 PCB trace. A frequency synthesizer provides 214-MHz asynchronous clock. The equalized data is observed by an oscilloscope and a BER tester. The integrated digital controller can be operated in internal- or external-control mode. In the

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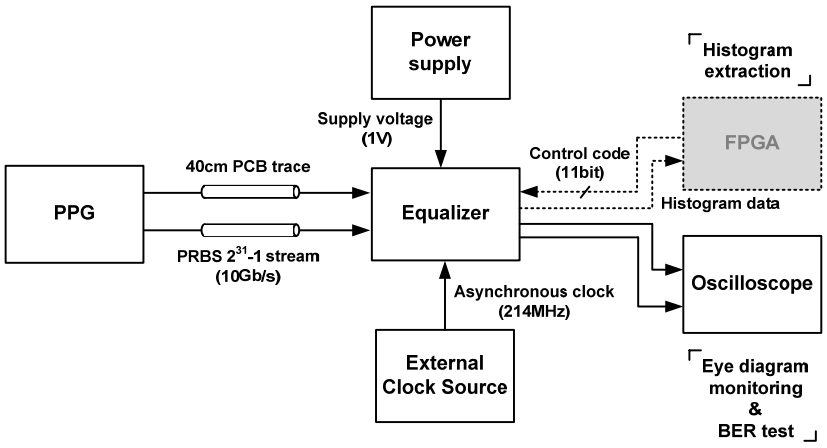

Fig. 5. Measurement Setup.

external-control mode, histogram data for any equalization coefficient can be delivered to a field-programmable gate array (FPGA) for testing purpose. In the internal control mode, the digital controller automatically determines the optimal equalization coefficient.

As the first verification, we measured the eye diagram and the histogram of equalized output for each of 8-equalization coefficients when data are transmitted through 40-cm FR4 PCB trace with the controller in the external-control mode. Fig. 6 shows measured eye diagrams and histograms for 8 different equalization coefficients. As can be seen, equalization coefficient 100 can be easily identified as the one producing the clearest eye diagram and the histogram having the largest peak value. Although histograms usually have two peaks, one of the two is larger due to uncertainty in the sampling. The controller simply searches for the peak having a larger value. With the controller in the internal-control mode, the

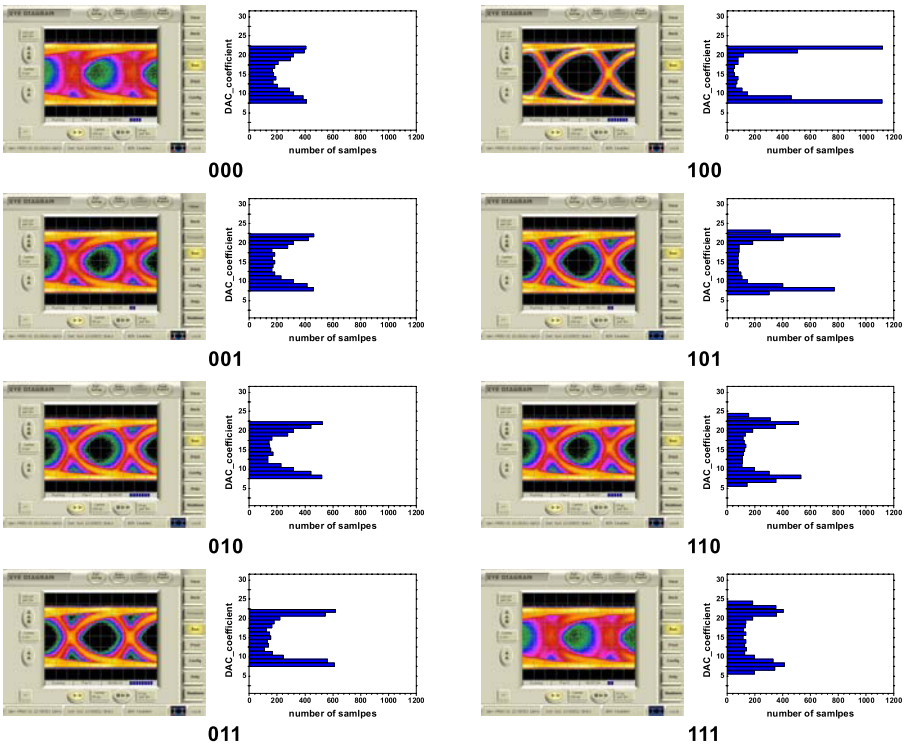

Fig. 6. Measured eye-diagram and histogram for each equalization coefficient.

DOI: 10.1587/elex.10.20130030
Received January 15, 2013
Accepted January 24, 2013
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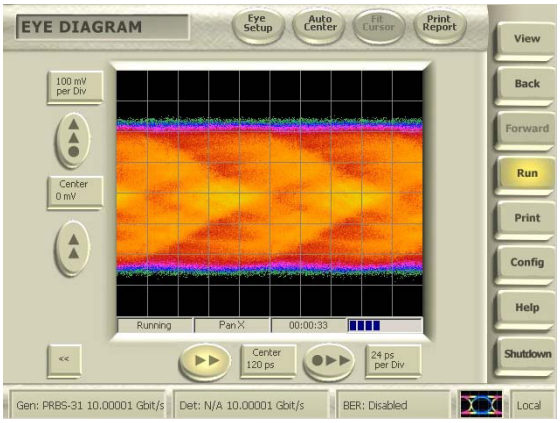
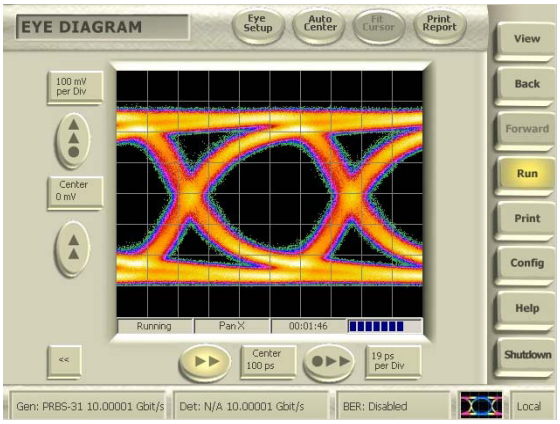
controller correctly selects equalization coefficient 100 as the optimal coefficient. The power consumption is 4.66 mW without output buffers from 1-V supply in the external-control mode when all the adaptation circuits are on.

Fig. 7 shows measured eye diagrams before and after equalization for 40-cm FR4 PCB trace with 10-Gb/s $2^{31}-1$ PRBS data. Eyes are clearly open after equalization. For this eye measurement, the optimal equalization coefficient was adaptively determined without any external control. Our adaptive equalizer achieves 10-Gb/s data transmission with less than 10^{-13} BER. The measured maximum peak-to-peak jitters are 26.6 ps. The power consumption is 2.49 mW after adaptation is completed.



(a)



(b)

Fig. 7. Eye-diagrams of (a) before and (b) after equalization.

Table II compares the performance of our CTLE reported in this work with previously reported low-power adaptive equalizers operating at around 10 Gb/s. Although the passive adaptive equalizer in [1] has the lowest power consumption, it should be noted that the equalizer in [1] does not include a limiting amplifier, which is required for boosting up the output to the desired level and can consume a substantial amount of power at 10 Gb/s. Although direct comparison of power consumption is difficult for CTLEs realized in different process technologies and having different amounts of peaking gain, our CTLE achieves the lowest power consumption. Furthermore, it has the advantage in that adaptation algorithm is

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Table II. Performance comparison of the proposed equalizer.

	CICC'09 [1]	JSSC'09 [2]	JSSC'05 [3]	EL'09 [6]	This work
Technology	90-nm CMOS	65-nm CMOS	110-nm CMOS	130-nm CMOS	65-nm CMOS
Filter type	Passive	DFE-IIR	CTLE	CTLE	CTLE
Adaptation	Power Comparison	N/A	ISI Monitoring	Power Comparison	Asynchronous Histogram
Data rate	12 Gb/s	10 Gb/s	10 Gb/s	10 Gb/s	10 Gb/s
BER	$< 10^{-10}$	$< 10^{-9}$	$< 10^{-12}$	N/A	$< 10^{-13}$
Boosting gain	13 dB at 6 GHz	27 dB at 5 GHz	20 dB at 5 GHz	15 dB at 5 GHz	15 dB at 5 GHz
Chip area	0.0336 mm^2	0.01725 mm^2	0.0156 mm^2	0.0065 mm^2	0.0386 mm^2
Supply voltage	1 V	1 V	1.2 V	1.2 V	1 V
Power consumption	1 mW	7 mW	23.2 mW	6 mW	4.66 mW* 2.49 mW**

Power consumption and chip area without output buffers.
*: During adaptation
**: After adaptation

performed with the integrated digital block, which consumes about 1 mW little power, is robust against any PVT variations, and can be turned off when not needed. We believe our adaptive CTLE can be a promising solution for demanding high-speed wire-line applications, especially for systems whose channel conditions does not change frequently.

4. Conclusion

We presented a 10-Gb/s low-power adaptive CTLE which automatically selects the optimal equalization coefficient among several pre-determined values by searching for the equalization coefficient that produces the largest peak value in histograms obtained with asynchronous under-sampling. The blocks used for adaptation are turned off for power reduction after the optimal equalization condition is achieved. A prototype chip realized in 65-nm CMOS technology successfully achieves adaptive equalization for 10-Gb/s $2^{31}-1$ PRBS data through 40-cm FR4 PCB trace. It consumes 4.66 mW during adaptation and 2.49 mW after adaptation from 1-V supply and occupies 0.0386 mm^2 of die area.

Acknowledgments

This work was supported by Samsung Electronics. We also acknowledge the support of IC Design Education Center (IDEC) for EDA software support, and Samsung Electronics for chip fabrication.

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