Optical-Power Dependence of Gain, Noise, and Bandwidth Characteristics for 850-nm CMOS Silicon Avalanche Photodetectors

Myung-Jae Lee, *Member, IEEE*, Holger Rücker, and Woo-Young Choi, *Member, IEEE*

***Abstract*—We investigate the effects of incident optical powers on the performance of 850-nm silicon avalanche photodetectors (APDs) realized with P^+/N-well junctions in standard CMOS technology. The current–voltage characteristics, responsivities, avalanche gains, noise power spectral densities, excess noise factors, electrical reflection coefficients, and photodetection frequency responses of the fabricated CMOS-APD are measured for different incident optical powers. In addition, the photodetection frequency responses at different incident optical powers are modeled with equivalent circuits and the influence of the optical power on photodetection bandwidth is analyzed. From these, we show that, near the avalanche breakdown voltage, the CMOS-APD avalanche gain and excess noise factor increase and photodetection bandwidth decreases with decreasing incident optical power. These results should be very useful for realizing high-performance CMOS integrated optical receivers for various optical-interconnect applications.**

***Index Terms*—Avalanche buildup time, avalanche photodetector (APD), avalanche photodiode, equivalent circuit model, inductive-peaking effect, optical interconnect, optical power, photodetection bandwidth, silicon photodiode, silicon photonics, standard CMOS technology.**

I. Introduction

EXISTING electrical interconnects are facing severe problems due to their link length limitation as well as increasing cross-talk noise and power consumption, while the data transmission bandwidth requirements for many interconnect applications are continuously increasing [1], [2]. As a solution for these problems, optical-interconnect technology based on the mature silicon technology has been actively investigated, because the silicon technology can provide very high cost-effectiveness and easiness in integration with complementary metal-oxide-semiconductor (CMOS) circuits [3]–[8]. 850-nm optical-interconnect technology based on the CMOS technology has been applied to various applications such as vehicular communications [9], rack-to-rack interconnects within data centers and computer clusters [10], [11], and on-board interconnects [12]–[14].

For some of these applications, realization of high-performance 850-nm monolithic optical receivers is of great interest and, for this, CMOS-compatible silicon photodetectors having high responsivity and large bandwidth are strongly needed. However, the standard CMOS technology provides too high doping concentrations and narrow depletion regions, which do not allow the optimal device structure for 850-nm photodetectors. Recently, their responsivity and photodetection-bandwidth performances have been greatly improved with CMOS-compatible avalanche photodetectors (CMOS-APDs) [15]–[22].

APDs are known to have optical-power-dependent characteristics. A Ge/Si APD with its optical-power-dependent characteristics at 1310 nm was reported in [23]. Recently, Gaberl *et al.* reported a highly sensitive APD realized in 0.35-μm CMOS technology with the optical power effects on gain, responsivity, and photodetection bandwidth performances at 670 nm [24]. However, the dependence of CMOS-APD noise on optical power has not been investigated until now. In addition, analyses for bandwidth dependence on optical power are needed for CMOS-APDs. Having detailed knowledge on these is essential for realizing high-performance integrated CMOS optical receivers having CMOS-APDs.

In this paper, we present the results of our investigation on the effects of incident optical powers on gain, noise, and bandwidth of CMOS-APDs at 850 nm. Furthermore, the measured optical-power-dependent photodetection frequency responses are modeled with equivalent circuits to identify the key element that influences CMOS-APD photodetection bandwidth dependence on incident optical power.

This paper is organized as follows. Section II describes structures of the CMOS-APD used in our investigation and its equivalent circuit model. Section III explains the measurement results. Section IV provides the results of the CMOS-APD photodetection frequency response analysis with equivalent circuits. Section V summarizes this paper.

II. Device and Equivalent Circuit Model Descriptions

Fig. 1 shows a cross section of the CMOS-APD fabricated with 0.25-μm standard BiCMOS technology provided by IHP [25]. Although the BiCMOS technology supports both bipolar and CMOS devices, the APD used for our investigation

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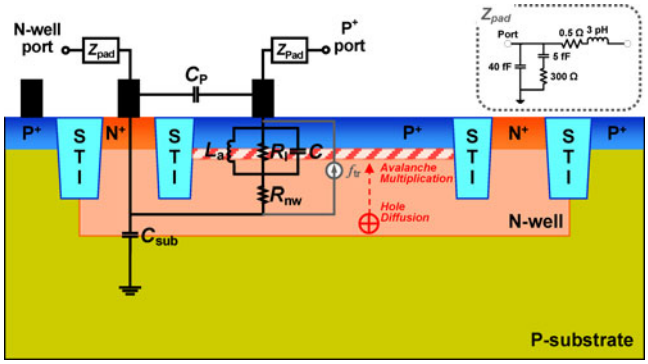
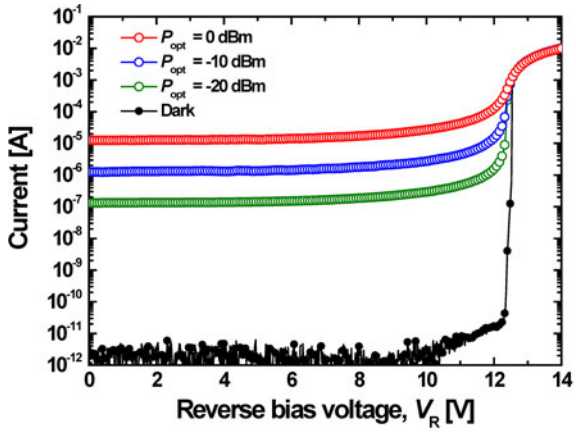
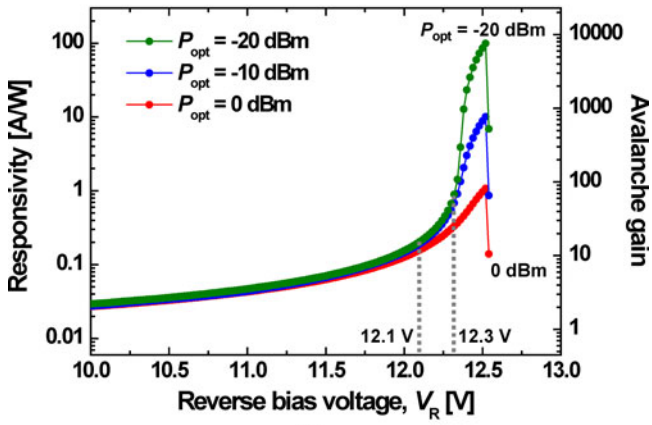


Fig. 1. Structure and equivalent circuit model of the fabricated CMOS-APD.



(a)



(b)

Fig. 2. (a) Current characteristics and (b) responsivity and avalanche gain characteristics of the CMOS-APD as a function of the reverse bias voltage at different incident optical powers.

is fabricated only with CMOS processing steps without any design or layout rule violations. It has optical-window area of 10 μm $\times$ 10 μm, formed by blocking the salicide process. The CMOS-APD has vertical P^+/N-well junction for photodetection, and the photocurrents are extracted from P^+ contacts located in the N-well region to exclude the slow diffusion currents in the P-substrate region. For bias, a positive voltage applied to the N-well, and P^+ inside N-well and P-substrate are grounded. Shallow trench isolation is used between P^+ and N^+ regions. The device structure is identical to that used in our previous investigation [20].

Also shown in Fig. 1 is an equivalent circuit model for the CMOS-APD, which is a simplified version of our previous work [26]. The equivalent circuit includes an inductor with a parallel resistor and a capacitor for the P^+/N-well junction in the avalanche regime. $R_{\rm nw}$ and $C_{\rm sub}$ represent N-well resistance and N-well/P-substrate junction capacitance, respectively. $C_{\rm p}$ is the parasitic capacitance between N^+ and P^+ electrodes, and $Z_{\rm pad}$ represents the equivalent circuit for the pad and metal interconnects. Photogenerated currents are modeled as a current source having a single-pole frequency response with $f_{\rm tr}$ representing the 3-dB bandwidth of the current source, which is determined by the diffusion time of photogenerated holes in the charge-neutral region in N-well and the avalanche buildup time of the avalanche multiplication region as shown in Fig. 1.

III. Measurement Results

A. DC Characteristics

For characterization of the CMOS-APD, an 850-nm laser diode and a 20-GHz electro-optic modulator are used as an optical source, and light is injected into the CMOS-APD through a lensed fiber having 10-μm spot size. The incident optical power is controlled by an 850-nm optical attenuator, and the CMOS-APD bias voltage is applied using a semiconductor parameter analyzer. All measurements are done on-wafer.

Fig. 2(a) shows measured current-voltage characteristics of the fabricated CMOS-APD at different incident optical powers. The CMOS-APD exhibits low dark currents below 0.1 nA before avalanche breakdown. With the reverse bias voltage approaching the avalanche breakdown voltage of about 12.4 V, currents start to increase dramatically with internal gain provided by the avalanche multiplication process. When the reverse bias voltage is larger than the breakdown voltage, the multiplied currents are saturated due to the space-charge effect. Carriers multiplied by the avalanche multiplication process modify space charges and depress the electric field in the multiplication region, resulting in the current saturation [27]. Before reaching the avalanche regime, the photogenerated currents increase linearly with the incident optical power, producing almost identical responsivities for the different optical powers as shown in Fig. 2(b). Near the avalanche breakdown, however, the CMOS-APD has larger responsivity for the smaller optical power. This is because multiplied currents are saturated at the same level regardless of the incident optical powers and, consequently, higher avalanche gain can be achieved for the smaller incident optical power producing smaller initial photogenerated currents. The maximum responsivity and avalanche gain are about 99 A/W and 7440, respectively, for the incident optical power of -20 dBm, while 1.1 A/W and 86 for 0 dBm.

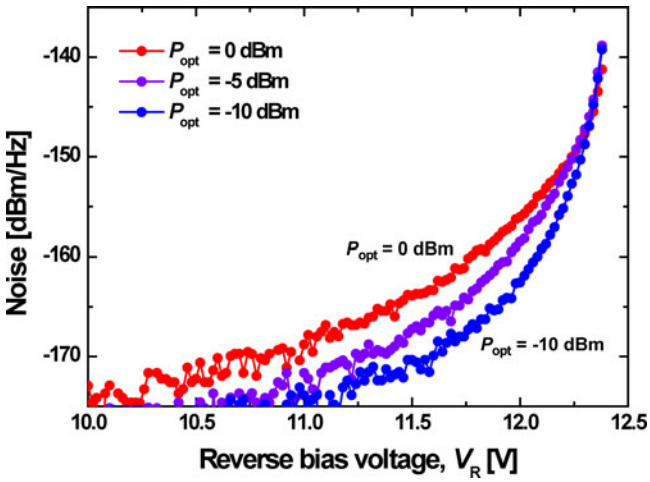


Fig. 3. Measured noise power spectral densities of the CMOS-APD as a function of the reverse bias voltage at different incident optical powers.

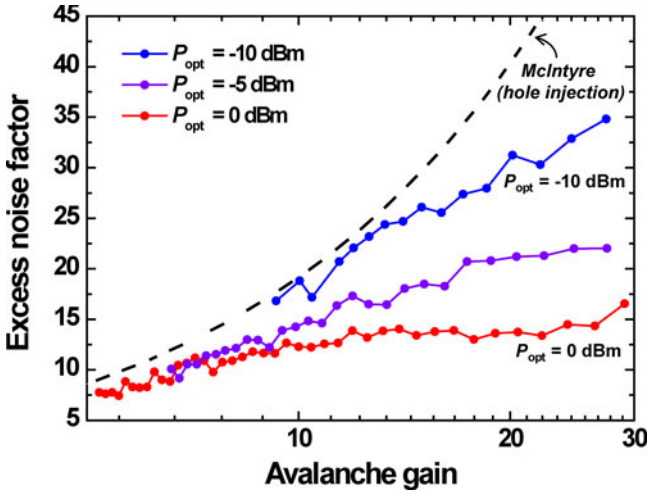


Fig. 4. Excess noise factors of the CMOS-APD as a function of the avalanche gain at different incident optical powers. The dashed line shows the prediction of McIntyre's model for hole injection.

B. Noise Characteristics

CMOS-APD noise power spectral densities are measured with a spectrum analyzer for three different incident optical powers of 0, –5, and –10 dBm. Measurement at –20 dBm does not provide reliable data due to too small noise levels. Since the directly measured noise level of our CMOS-APD is less than the sensitivity limitation of our spectrum analyzer, a commercially available low-noise amplifier (LNA) having 26-dB gain and 3-dB noise figure is used at the output of the CMOS-APD to intentionally boost up the noise level. Then, the measurement results are calibrated to exclude the effects of the LNA as well as electrical cables. Since our LNA has the low-frequency cut-off at about 0.7 GHz, the noise measurement is done at 1 GHz.

Fig. 3 shows measured noise power spectral densities as a function of the reverse bias voltage at three different optical powers. The noise power spectral density is described as

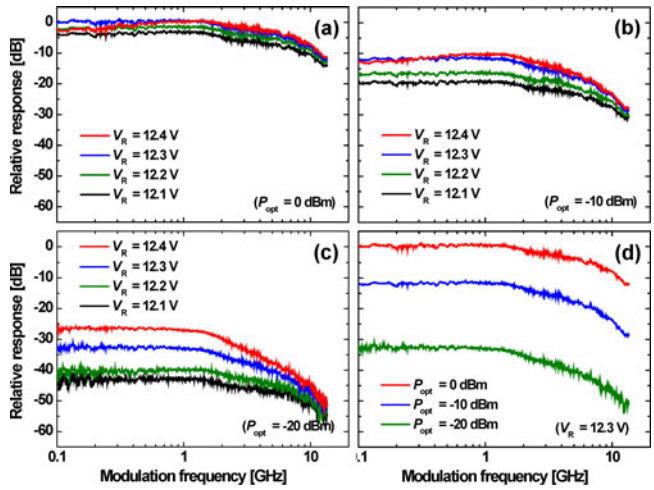


Fig. 5. Photodetection frequency responses of the CMOS-APD at different bias voltages when the incident optical powers are (a) 0 dBm, (b) −10 dBm, and (c) −20 dBm. (d) Photodetection frequency responses of the CMOS-APD at the different incident optical powers when the reverse bias voltage is 12.3 V.

$$P_{\mathrm{n\_APD}} = 2 \cdot q \cdot \langle I_{\mathrm{Illum}} \rangle \cdot \langle M \rangle^2 \cdot F(M) \cdot R \qquad (1)$$

where q is the electron charge, $\langle I_{\mathrm{Illum}} \rangle$ is the mean current under illumination, $\langle M \rangle$ is the mean avalanche gain, *F(M)* is the excess noise factor, and *R* is the 50-Ω input impedance of the LNA used for measurement. As expected, the measured noise power spectral density is larger for larger optical power due to larger $\langle I_{\mathrm{Illum}} \rangle$, and increases with the reverse bias voltage due to larger $\langle M \rangle$. However, the difference in noise power spectral densities between different optical powers becomes smaller for larger reverse bias voltages. This is because as the reverse bias voltage increases, the avalanche gain for lower optical power becomes much larger than the higher optical power, as can be observed in Fig. 2, resulting in more rapid increase in noise power spectral densities for smaller optical powers.

From the measured noise spectral density, the photocurrent, and avalanche gain, the excess noise factor can be determined using (1). Fig. 4 shows the excess noise factor as a function of avalanche gain at three different optical powers. The measured noise power spectral densities show a fair amount of fluctuations when the reverse bias voltage is not large enough especially for the small incident optical power as can be shown in Fig. 3. In order to eliminate any influence of these fluctuations on excess noise factor estimation, only those data points that have larger than −165-dBm/Hz noise power densities are used for Fig. 4.

Also shown in the figure is the excess noise factor calculated with McIntyre's model assuming hole-initiated multiplication [28], which is the case for our CMOS-APD because most carriers are generated in N-well at 850 nm. For the calculation, the effective electron and hole ionization coefficient ratio of 0.47 is used, which is determined for N-well doping concentration of 1.5×10^{17} cm^{-3} [29], [30]. As can be seen in Fig. 4, the estimated noise factors for our CMOS-APD are smaller than the value calculated with McIntyre's model. This is due to the dead

space, the minimum distance a newly generated carrier must travel to gain sufficient energy to cause impact ionization. In conventional APDs with thick multiplication regions on which McIntyre's model is based, the dead-space effect can be ignored. However, the multiplication region for our CMOS-APD is very thin as avalanche multiplication occurs only inside the N-well, and the excess noise factor is greatly influenced by the dead space [29], [30].

It is also interesting to note in Fig. 4 that the excess noise factor increases as the incident optical power decreases. This dependence cannot be easily explained with APD models known to us, and additional analysis is needed in order to clarify this dependence.

C. AC Characteristics

Fig. 5(a)–(c) show measured photodetection frequency responses of the CMOS-APD at different bias voltages for three different incident optical powers of 0, –10, and –20 dBm, respectively. As the reverse bias voltage increases, the photodetection frequency response initially increases due to the avalanche gain. With further increase in the bias voltage, however, the response begins to go down but it shows peaking in high frequency caused by the inductive-peaking effect [22], resulting in reduced response only in the low-frequency range as can be clearly seen in Fig. 5(a) and (b). The bias voltage at which this low-frequency response reduction begins is slightly higher when the incident optical power is smaller. As a result, the response at −20-dBm optical power shown in Fig. 5(c) does not show the suppressed low-frequency response. For fair comparison of CMOS-APD frequency responses at different incident optical powers, we fix the reverse bias voltage at 12.3 V where photodetection frequency responses do not show suppressed low-frequency responses, which are not desirable for applications. Fig. 5(d) shows responses at the reverse bias voltage of 12.3 V for three different optical powers. In contrast to PDs without avalanche gain where 10 (20) dB drop of optical power produces 20 (40) dB in measured electrical power, the CMOS-APD shows drop of 12 dB for 10-dB optical power reduction and 32 dB for 20-dB reduction due to higher avalanche gain for smaller optical power as shown in Fig. 2(b).

Fig. 6(a) and (b) shows normalized photodetection frequency responses of the CMOS-APD at three incident optical powers when the reverse bias voltages are 12.1 and 12.3 V, respectively. At the reverse bias voltage of 12.1 V, where the incident optical power has little effect on avalanche gain as can be seen in Fig. 2(b), the incident optical power does not affect the photodetection bandwidth. At the reverse bias voltage of 12.3 V, however, the bandwidth decreases from 4.7 to 2.2 GHz with decreasing optical power from 0 to −20 dBm as shown in Fig. 6(b).

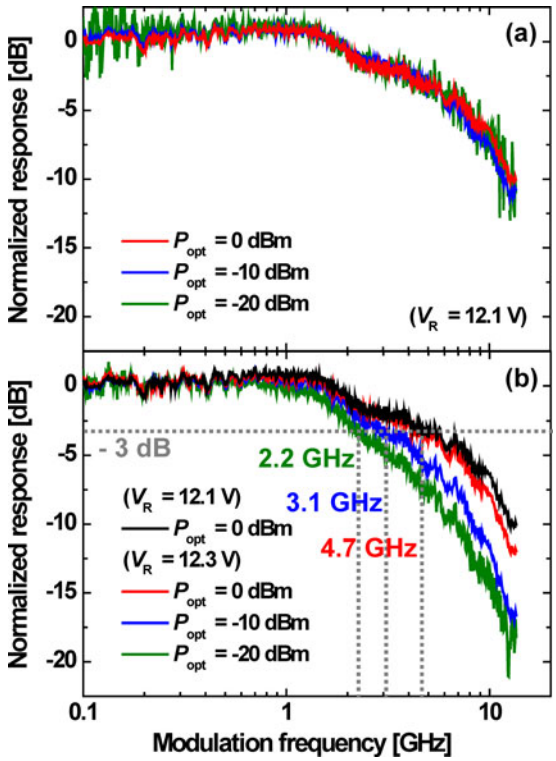


Fig. 6. Normalized photodetection frequency responses of the CMOS-APD at different incident optical powers when the reverse bias voltages are (a) 12.1 V and (b) 12.3 V.

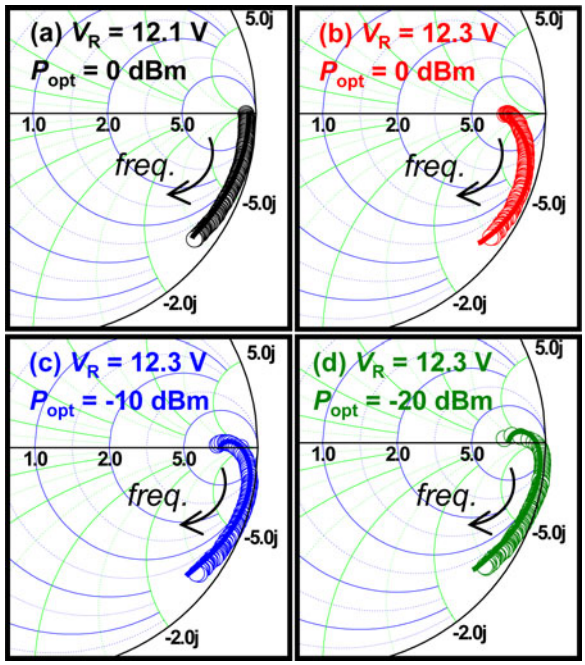


Fig. 7. Measured and simulated electrical reflection coefficients of CMOS-APDs at different operating conditions. Hollow circles represent measured data and solid lines simulated results.

IV. Equivalent Circuit Analyses and Discussions

To understand the effects of the incident optical powers on the photodetection bandwidth of the CMOS-APD, we perform analyses based on the equivalent circuit model shown in Fig. 1. Parameters for the equivalent circuit are extracted from two-port

TABLE I
EXTRACTED PARAMETERS FOR THE CMOS-APD AT DIFFERENT OPERATING CONDITIONS

	$V_{\rm R}$ = 12.1 [V]	$V_{\rm R}$ = 12.3 [V]		
	$P_{\rm opt}$ = 0 [dBm]	$P_{\rm opt}$ = 0 [dBm]	$P_{\rm opt}$ = −10 [dBm]	$P_{\rm opt}$ = −20 [dBm]
$L_{\rm a}$ [nH]	–	15	55	130
$R_{\rm l}$ [kΩ]	2		5	
C [fF]	21		21	
$R_{\rm nw}$ [kΩ]	1		0.5	
$C_{\rm sub}$ [fF]	25		25	
$C_{\rm p}$ [fF]	35		35	
$f_{\rm tr}$ [GHz]	5	3.5	2.3	1.8

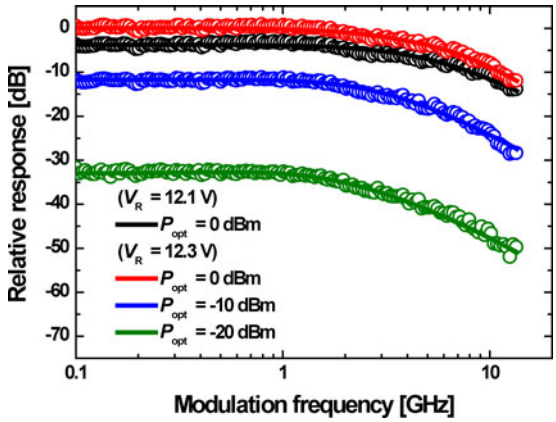


Fig. 8. Measured and simulated photodetection frequency responses of the CMOS-APD at different operating conditions. Hollow circles represent measured data and solid lines simulated results.

S-parameter and photodetection frequency response measurements as was done in our previous work [26]. Fig. 7 shows the measured CMOS-APD electrical reflection coefficients as well as the simulated results with extracted parameters on Smith charts at two different bias voltages and three different incident optical powers. Since there is virtually no difference in photodetection frequency responses at the reverse bias voltage of 12.1 V for the different incident optical powers as shown in Fig. 6(a), only the result for 0-dBm optical power is shown for the bias of 12.1 V in Fig 7(a).

Those electrical parameter values used for the simulation are given in Table I. C and $C_{\rm sub}$ are assumed the same for all the cases since they change very little with the bias voltage and the optical power, and $C_{\rm p}$ is the same for all the cases since an identical device is used for this investigation. $R_{\rm l}$ and $R_{\rm nw}$ are different for both voltages because of the different current–voltage characteristics. At the reverse bias voltage of 12.1 V, the CMOS-APD does not have the avalanche inductive component because the device does not have significant avalanche gain as shown in Fig. 2(b). At the reverse bias voltage of 12.3 V, however, the CMOS-APD has significant inductive components, and $L_{\rm a}$ increases with decreasing optical power because it is inversely proportional to the photocurrent.

$f_{\rm tr}$ is extracted from the measured photodetection frequency responses of the CMOS-APD. Fig. 8 shows measured and simulated results, and the values for $f_{\rm tr}$ used for the simulation are also given in Table I. The photodetection frequency response of the CMOS-APD is influenced by several factors such as photogenerated-carrier transit time and its *RLC* components. The carrier transit time for the CMOS-APD is determined by the photogenerated-hole diffusion time in the charge-neutral N-well as well as the avalanche buildup time in the avalanche region. Fig. 9 shows the simulated photodetection frequency responses at four different operating conditions. For each condition, comparisons are made between a case where only the photogenerated-carrier transit time without any *RLC*-component effect is considered, a case where only *RLC*-component effect without any transit-time effect is considered, and a case where both transit-time and *RLC*-component effect are considered. The third case matches well with the measured response as shown in Fig. 8. From these, it can be observed that the transit time is the photodetection bandwidth limiting factor of our CMOS-APD. This is because, as shown in Fig. 1, photogenerated carriers outside the depletion region must diffuse to the junction with considerable time delay and then go through the avalanche multiplication region which results in additional time delay. Among four different cases, the transit-time response has the largest bandwidth at the reverse bias voltage of 12.1 V since the avalanche buildup time can be negligible at this operating condition. Although the response considering only the transit time has lower bandwidth at the reverse bias voltage of 12.3 V (see Fig. 9(b)) than at 12.1 V (see Fig. 9(a)) at the same incident optical power of 0 dBm, the actual photodetection bandwidths are almost the same because of the inductive-peaking effect as can be seen in Fig. 6(b). At the reverse bias voltage of 12.3 V, the photodetection bandwidth becomes smaller for smaller incident optical powers because the avalanche buildup time increases with smaller optical powers. However, the response of the CMOS-APD includes all the factors have larger bandwidth than the limitation of the transit time because the inductive-peaking frequency is decreased with the optical-power decrease due to the increased $L_{\rm a}$.

In order to clarify the influence of the avalanche buildup time on the photogenerated-carrier transit time, we estimate the avalanche buildup time at different incident optical powers. For this analysis, the reverse bias voltage of 12.1 V can be used as a reference because the CMOS-APD depletion widths are almost the same for the reverse bias voltages of 12.1 and 12.3 V, resulting in the same diffusion length for both. In addition,

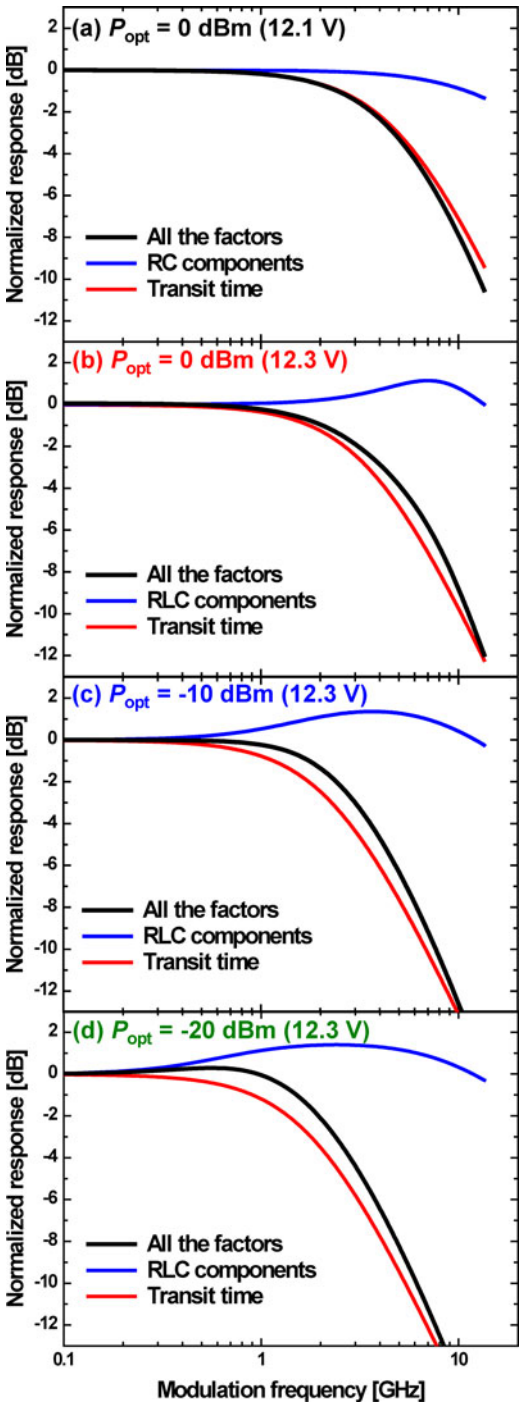


Fig. 9. Simulated photodetection frequency responses of the CMOS-APD for photogenerated-carrier transit time, *RLC* components, and all the factors at different operating conditions.

since avalanche gain is negligible at the reverse bias voltage of 12.1 V, the avalanche buildup time can be ignored and the transit time is determined by the diffusion time only. At the reverse bias voltage of 12.3 V, therefore, the avalanche buildup time according to the incident optical powers can be estimated by comparing the transit time at the reverse bias voltage 12.1 V. Table II shows the estimated transit times and avalanche buildup times for the CMOS-APD at the different operating conditions. The lower incident optical power causes lower photogenerated carriers injected into the avalanche multiplication region, and therefore the avalanche buildup time becomes higher until the saturation is reached. From this analysis we can clearly see that the avalanche buildup time becomes larger than the slow diffusion time at the incident optical power of –10 dBm and has larger influence on the transit time than the diffusion time at the incident optical power of −20 dBm.

TABLE II
ESTIMATED TRANSIT TIMES AND AVALANCHE BUILDUP TIMES FOR THE CMOS-APD AT DIFFERENT OPERATING CONDITIONS

V_R	P_{opt}	f_{tr}	τ_{tr}	τ_a
12.1 V	0 dBm	5 GHz	31.83 ps	0 ps
12.3 V	0 dBm	3.5 GHz	45.47 ps	13.64 ps
12.3 V	−10 dBm	2.3 GHz	69.20 ps	37.37 ps
12.3 V	−20 dBm	1.8 GHz	88.42 ps	56.59 ps

τ_{tr}: transit time; τ_a: avalanche buildup time.

V. CONCLUSION

We have investigated optical-power-dependent characteristics of the 850-nm silicon APD based on the P^+/N-well junction realized in standard CMOS technology. Before reaching the avalanche regime, the CMOS-APD performance has essentially no dependence on the incident optical power. Near the avalanche breakdown, however, the CMOS-APD gain and excess noise factor increase and its photodetection bandwidth decreases with the decreasing optical power. In order to understand the effects of the incident optical powers on the photodetection bandwidth, the CMOS-APD electrical reflection coefficients and photodetection frequency responses are analyzed using the equivalent circuit model. From this analysis, it is clarified that the avalanche buildup time has larger influence on the photodetection bandwidth than the diffusion time when the incident optical power becomes lower. In addition, although the photodetection bandwidth is limited by the additional avalanche buildup time, the CMOS-APD has larger photodetection bandwidth than the limitation due to the continuously available inductive-peaking effect with the decrease of the incident optical power. These results should be useful in realizing high-performance integrated optical receiver circuits in which transimpedance gain of the transimpedance amplifier and equalizer gain can be custom-designed reflecting CMOS-APD responsivity, noise, and photodetection-bandwidth characteristics.

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