A Multi-band VCO PLL with the Continuously Maintained Optimum VCO Control Voltage

Y.-S. Park, D.-H. Kwon, K.-C. Choi and W.-Y. Choi

A new architecture for a multi-band VCO PLL is presented which can continuously maintain the optimum VCO sub-band and the VCO control voltage even with severe supply voltage variation. A prototype 2-GHz PLL with the new architecture is successfully demonstrated in 0.13µm CMOS technology.

Introduction: Phase-locked loops (PLLs) are widely used for on-chip clock generation for many electronic circuits and systems. Since the clock signal quality has a great influence on system performance, PLLs with low-gain voltage-controlled oscillators (VCOs) are preferred for realizing low-jitter clock signals. However, a single low-gain VCO cannot guarantee the target operating frequency against process, voltage, and temperature (PVT) variation and, consequently, multi-band VCOs are commonly used. A multi-band VCO PLL initially selects the VCO sub-band that can provide the target locking frequency and then fine tunes the VCO control voltage (V_{cont}) within the selected VCO sub-band with the PLL feedback loop [1], [2]. Another method of performing the essentially same task is using a dual-gain VCO. With this, the initial selection of VCO sub-band is done with VCO in the high-gain mode and the fine tuning with the selected VCO sub-band is done in the low-gain mode. Fig. 1 shows the block diagram of one type of a dual-gain VCO PLL that uses the successive approximation register analog-to-digital converter (SAR-ADC) [3] for sub-band searching. In this structure, the VCO has coarse and fine control signals for high- and low-gain operation, respectively. Initially, both VCO control signals are tied together resulting in the same configuration as a conventional PLL having high-gain VCO for the initial VCO sub-band searching and V_{DAC} tracks V_{cont}. After the PLL is locked the with high-gain VCO and, therefore, the desired VCO sub-band is selected, the VCO switches into the low-gain mode and fine tuning of is V_{cont} done for the selected VCO subband, which is maintained by with the constant the SAR-ADC output.

The initial search should produce the VCO sub-band that can result in the final V_{cont} around the half of V_{DD} where the PLL has the largest margin for voltage and temperature variation. However, unexpected changes in supply voltages can cause changes in VCO characteristics and, consequently, require a shift in V_{con} in order to provide the target frequency as shown in Fig. 2. In such a case, the value of V_{cont} becomes undesirable as shown by Path (1) in Fib. 2b. In order to bring back V_{cont} into the desired range, the PLL should switch the VCO sub-band as shown Path (2) in Fig. 2b. But switching VCO sub-bands causes a sudden frequency jump and results in momentary loss of PLL lock. A dual PLL architecture with two separate PLLs can prevent such a problem [4], but it requires doubling of the chip area and power consumption. In this paper, we propose a new technique of maintaining V_{cont} in the desired voltage range against supply voltage changes without losing PLL lock.

PLL Structure: Fig. 3 shows the block diagram of our PLL that can continuously maintain optimum V_{cont}. Our PLL is based on the SAR-ADC PLL [3] and has two additional blocks: V_{cont} monitor which produces the VCO sub-band switching signal when V_{cont} is out of the pre-determined range and bandwidth controllable low-pass filter (BC-LF) whose bandwidth can be switched between 100KHz and 2MHz. During the initial VCO sub-band searching process, V_{cont} monitor is not operational and BC-LF has high-bandwidth so that the initial VCO sub-band searching process is not disturbed. Once the searching process is complete, V_{cont} monitor begins its operation and BC-LF changes its bandwidth from high to low so that the DAC output is low-pass filtered, preventing any sudden voltage jumps due to the SAR-ADC output bit changes for VCO sub-band switching.

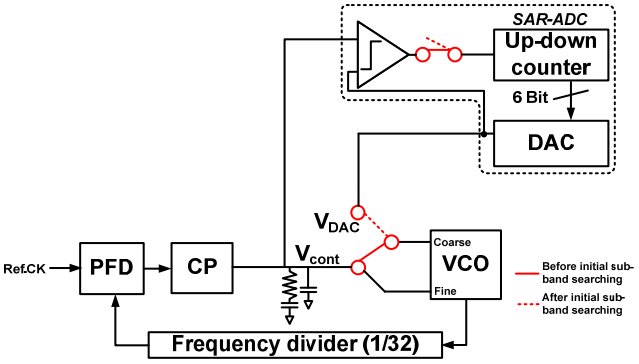

Fig. 1 *SAR-ADC PLL*

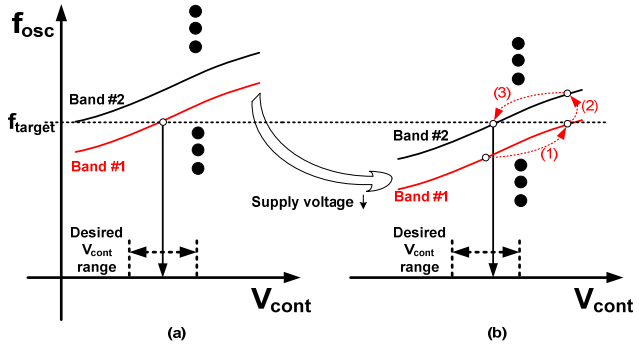

Fig. 2 *VCO sub-band switching due to supply voltage variation*

a. After initial sub-band searching

b. After supply voltage variation

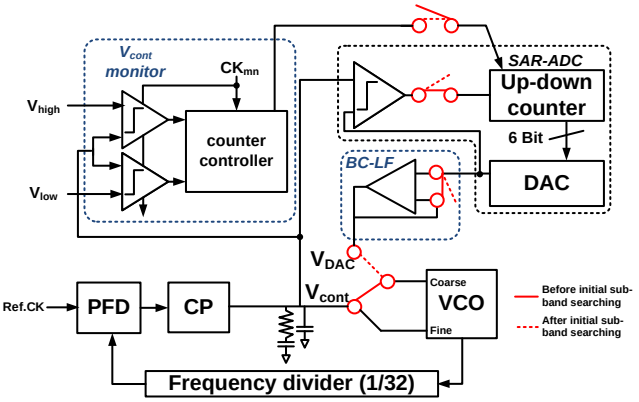

Fig. 3 *Block diagram of the Proposed PLL*

As can be seen in Fig. 3, V_{cont} monitor is composed of two comparators that check whether V_{cont} is between V_{high} and V_{low} at every rising edge of the monitoring clock (CK_{mn}). In our implementation, CK_{mn} is 1/512 of the PLL reference clock. If V_{cont} is out of this range, the up-down counter in SAR-ADC increases/decreases its output until V_{cont} is within the range. In addition, there is a switch at the input node of BC-LF so that BC-LF can be by-passed during the initial VCO sub-band searching process. After the search is complete, the switch is open and BC-LF has the same configuration as a unit-gain buffer which has low-pass filter characteristic. In our design, VCO is implemented with a ring of 4-stage inverters and its oscillation frequency is tuned by controlling the tail currents. The phase-frequency detector and the charge pump have conventional structures. A prototype chip is fabricated in 0.13 µm CMOS technology. The loop filter is realized off-chip so that PLL loop dynamics can be optimized externally. The lock detection signal that provides the control signals for the switches is provided from a FPGA during the measurement.

Measurement results: Fig. 4 shows the chip photograph. It occupies $0.084mm^2$ and dissipates 34mW from 1.2V supply. V_{cont} monitor and BC-LF occupies $0.01mm^2$ and dissipates 2mW. Fig. 5 shows measured V_{cont} during VCO sub-band switching. For this measurement, we

intentionally set the VCO bias voltage so that the initial V_{cont} value is higher than V_{high}=0.65V. As can be seen in the figure, our PLL automatically brings V_{cont} into the desired range. For this, three incidences of sub-band switching are performed as shown in the figure. During the entire process, the PLL remains locked as can be evidenced from the measured 2GHz PLL output signals shown in the figure.

Fig. 6 shows measured Vcont with a continuously increasing supply voltage. With Vcont monitor operation disabled, the SAR-ADC PLL loses its lock even with a small supply voltage increase. With our technique, the PLL continuously remains locked and maintains Vcont within the desired range even when the supply voltage changes from 1.2V to 1.6V. The output clock rms jitter is maintained around 7ps.

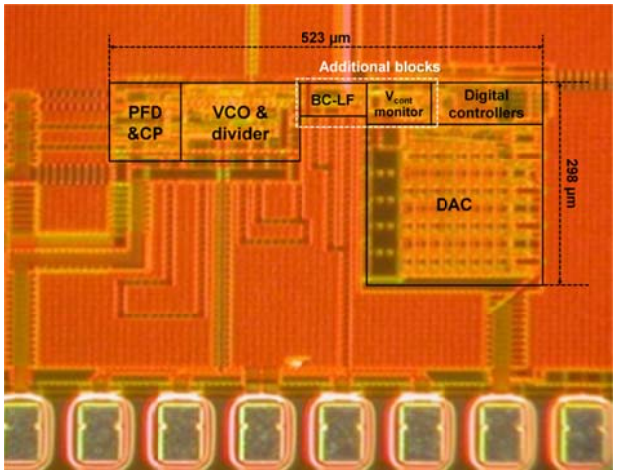

Fig. 4 *Chip microphotograph.*

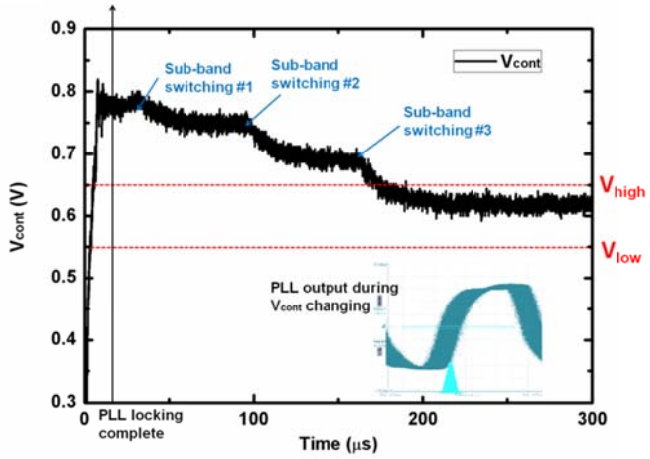

Fig. 5 *Measured V_{cont} during sub-band switching and traces of PLL output.*

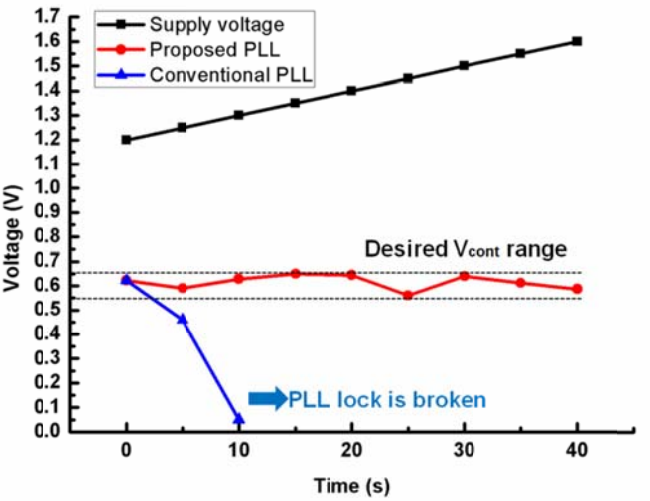

Fig. 6 *Measured V_{cont} under continuous supply voltage variation*

Conclusion: We have demonstrated a novel technique of maintaining V_{cont} within the desired range even with severe supply voltage variation. With our technique, a multi-band VCO PLL can switch the sub-band without losing its lock, and the PLL can maintain optimum V_{cont} value against any supply voltage changes. This technique should provide robust PLL operation against temperature variation as well.

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References

1. T. H. Lin and Y. J. Lai, "An Agile VCO Frequency Calibration Technique for a 10-GHz CMOS PLL", IEEE J. Solid-State Circuits, vol. 42, No. 2, pp. 340-349, Feb. 2007.
2. Lei Lu, et al., "A 975-to-1960MHz Fast-Locking Fractional-N Synthesizer with Adaptive Bandwidth Control and 4/4.5 Prescaler for Digital TV Tuners", Dig. Tech. Pprs. ISSCC, Feb. 2009, San Francisco, CA, USA, pp. 396–398
3. S. H. Cho, et al., "Dual-mode VCO gain topology for reducing in-band noise and reference spur of PLL in 65nm CMOS", IET Electronic Letter, vol. 46, No. 5, pp. 335-337, Mar. 2010.
4. J. H. Kim, "Adaptive-Bandwidth Phase-Locked Loop With Continuous Background Frequency Calibration", IEEE Trans. Circuits Syst. II, vol. 56, No. 3, pp. 205-209, Mar. 2009.