A High-Speed CMOS Integrated Optical Receiver With an Under-Damped TIA

Hyun-Yong Jung, *Student Member, IEEE*, Jeong-Min Lee, *Student Member, IEEE*, and Woo-Young Choi, *Member, IEEE*

***Abstract*— We present a CMOS integrated optical receiver having under-damped transimpedance amplifier (TIA) and CMOS avalanche photodetector (APD) realized in 65-nm CMOS technology. The under-damped TIA compensates the bandwidth limitation of CMOS APD and provides enhanced receiver bandwidth performance with reduced power consumption and better sensitivity compared with previously reported techniques. We successfully demonstrate 10-Gb/s $2^{31}-1$ PRBS and 12.5-Gb/s $2^{7}-1$ PRBS operation with the bit-error rate less than 10^{-12} at the incident optical power of −6 and −2 dBm, respectively. The receiver has core size of 0.24 mm × 0.1 mm and power consumption excluding output buffer of ∼13.7 mW with 1.2 V supply voltage.**

***Index Terms*— CMOS PD, optical receiver, optoelectronic, transimpedance amplifier, under-damped response.**

I. Introduction

As THE bandwidth requirement for various interface applications continuously increases, there are growing research efforts for optical interconnects that can overcome the limitation of electrical interconnects. As one of these, 850-nm optical interconnects based on vertical-cavity surface-emitting lasers (VCSEL) and multimode fibers (MMF) are receiving much attention especially for such short-reach applications as chip-to-chip, board-to-board, or rack-to-rack interconnects [1]. For these applications, fully integrated 850-nm optical receivers implemented in standard complementary metal-oxide-semiconductor (CMOS) technology can provide great advantages in terms of fabrication cost and manufacturability [2], [3].

For CMOS integrated optical receivers, the bandwidth limitation of photodetectors (PDs) realized in standard CMOS PDs suffers from slow diffusive photocurrents. Although several high-speed monolithically integrated optical receivers realized in CMOS technology have been reported, they rely on either special PD structures such as spatially-modulated PDs (SM PDs) [4], [5] or electronic equalizers [6], [7]. However, SM PDs suffer from low responsivity and electronic equalizers require additional power and chip area. In this letter, we demonstrate a new and simple technique of compensating PD bandwidth limit with an under-damped TIA which can have better power efficiency and small chip area.

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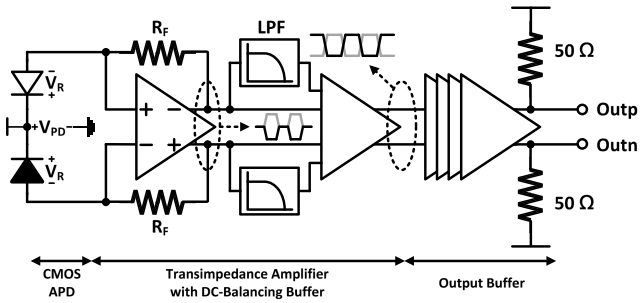

Fig. 1. Block diagram of the proposed optical receiver.

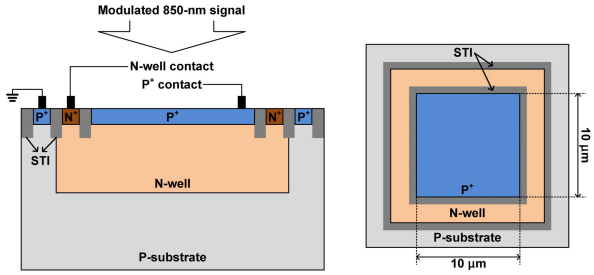

Fig. 2. (a) Cross section and (b) top view of the fabricated CMOS APD.

II. CMOS Integrated Optical Receiver

Fig. 1 shows the simplified block diagram of our CMOS integrated optical receiver. It is composed of a CMOS APD with a dummy PD, an under-damped TIA with a DC-balancing buffer, and an output buffer with 50-Ω load. The dummy PD provides symmetric capacitance to the differential TIA input. Our receiver does not contain a limiting amplifier (LA) since we are interested in a fully integrated optical receiver in which PD, TIA and clock and data recovery (CDR) circuits are integrated together. Since typical CDR circuits require input voltage levels in the order of tens of mV, a LA is not needed if CDR circuit can be directly integrated with the TIA. The goal of this work is to verify the performance of PD and TIA before we can implement the fully integrated optical receiver.

A. CMOS Avalanche Photodetector

Fig. 2(a) and (b) show the cross-section and the top view of the CMOS APD used in our integrated receiver. It is realized with P^+ source/drain and N-well junction in standard CMOS technology without any design-rule violation.

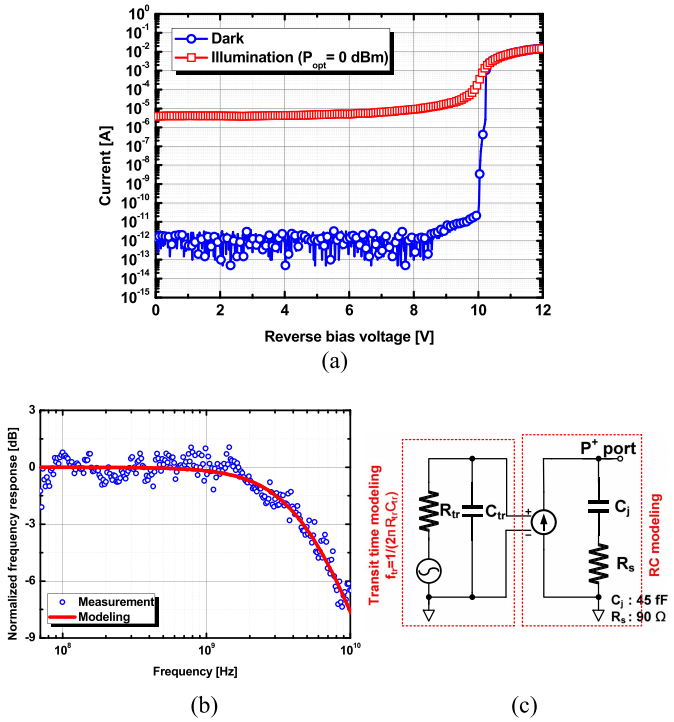

Fig. 3. (a) DC characteristic, (b) frequency response for measurement and model and (c) equivalent circuit model of CMOS APD.

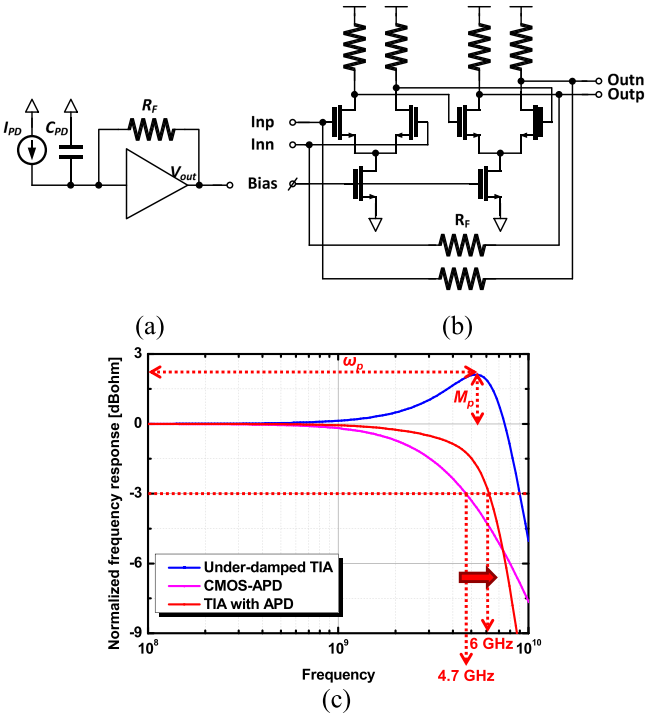

Fig. 4. (a) Block diagram, (b) schematic diagram and (c) simulated frequency response of the TIA.

Shallow trench isolation surrounding the vertical PN junction provides large and uniform electric fields that are desired for avalanche gain. Photo-generated currents are taken from P^+ contact to TIA since currents from N-well include diffusive components due to light absorbed in P-substrate. The CMOS APD has 10 μm $\times$ 10 μm of optical-window for optimal photo-detection bandwidth [8].

For TIA design optimization, an accurate APD model is essential. The 3-dB bandwidth of our CMOS APD, f_{PD}, can be determined as $f_{PD} = 1/[(1/f_{tr})^2+(1/f_{RC})^2]^{1/2}$ where f_{tr} and f_{RC} represent the 3-dB bandwidth due to photogenerated hole transit time and the APD RC time, respectively. Fig. 3(a) shows the measured DC characteristic of our APD with 0-dBm input optical power. For our optical receiver, the reverse bias voltage of 9.7 V is used, where the APD provides the best bit error rate (BER) performance as determined by measurement. Fig. 3(b) shows the measured photo-detection frequency response of our APD and Fig. 3 (c) shows the equivalent circuit model of the APD. C_j and R_s represent the depletion region capacitance and N-well series resistance, respectively. R_{tr} and C_{tr} are used to model the influence of hole transit time in the APD. The numerical values of these parameters are determined by fitting equivalent circuit simulation results to measured s-parameter and frequency responses of CMOS APD. As can be seen in Fig. 3(b), the APD has limited 3-dB bandwidth of about 4.7 GHz.

B. Under-Damped TIA

The limited bandwidth of CMOS APD can be compensated by an under-damped TIA, which gives peaked frequency response and, consequently, enhanced optical receiver bandwidth.

Fig. 4(a) shows the block diagram of our under-damped TIA. The shunt-shunt feedback configuration is used, which provides low noise characteristics and high gain-bandwidth product. Since the transfer function of the core voltage amplifier can be approximated as [9]

$$A(s) = \frac{A_0}{1 + s/\omega_0}, \tag{1}$$

the closed loop transfer function of the TIA is given as

$$\frac{V_{out}}{I_{PD}} = -\frac{A_0\omega_0}{C_{PD}} \frac{1}{s^2 + \frac{R_F C_{PD}+1/\omega_0}{R_F C_{PD}/\omega_0} s + \frac{(A_0+1)\omega_0}{R_F C_{PD}}}, \tag{2}$$

which results in low-frequency transimpedance gain of $A_0R_F/(A_0+1)$. The denominator of above equation can be expressed as the standard second-order system function as $s^2+ 2\zeta\omega_n s + \omega_n^2$, where ζ is the damping factor and ω_n is the natural frequency with [9]

$$\zeta = \frac{1}{2} \frac{R_F C_{PD}\omega_0 + 1}{\sqrt{(A_0+1)\omega_0 R_F C_{PD}}} \quad \text{and} \tag{3}$$

$$\omega_n = \sqrt{\frac{(A_0+1)\omega_0}{R_F C_{PD}}}. \tag{4}$$

The limited bandwidth of CMOS APD can be compensated by the peaked response of the under-damped TIA. For the under-damped response, we need $\zeta < \sqrt{2}/2$ and the peaking magnitude, M_p, and the peaking frequency, ω_p, are given as [10]

$$M_p = \frac{1}{2\zeta\sqrt{1-\zeta^2}} \quad \text{and} \tag{5}$$

$$\omega_p = \omega_n\sqrt{1-2\zeta^2}, \tag{6}$$

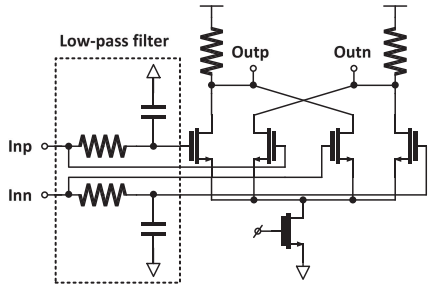

Fig. 5. Schematic diagram of the DC-balancing buffer.

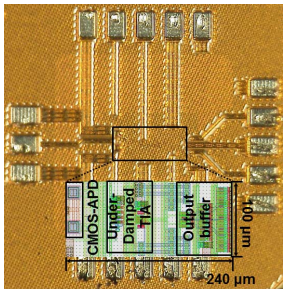

Fig. 6. Microphotograph and layout of the fabricated optical receiver.

M_p and ω_p should be carefully determined so that the limited bandwidth of CMOS APD can be effectively compensated. Fig. 4(b) presents the schematic diagram of our TIA and Fig. 4(c) shows the simulated frequency response of CMOS APD, under-damped TIA and the integrated optical receiver. The under-damped TIA used for simulation has 2-kΩ feedback resistor and core amplifier which provides 20-dB gain and 4.5-GHz bandwidth. The under-damped TIA results in 3.5 dB of M_p and 25 GHz of ω_p, which gives the optimal frequency compensation performance. As shown in the Figure 4(c), the under-damped TIA achieves 3-dB bandwidth of 6 GHz with a CMOS APD having 4.7-GHz bandwidth. It should be noted that this enhancement is achieved without any additional active circuits consuming additional power or SM PD decreasing responsivity only with TIA design modification.

C. DC-Balancing Buffer and Output Buffer

Delivering photo-generated currents to only one port of two differential TIA input ports induces a DC offset in TIA differential output, which can result bit errors with the decision threshold problem. To solve this problem, a DC-balancing buffer is added. Fig. 5 shows the schematic diagram of the designed DC-balancing buffer. Two on-chip low-pass filters and f_T-doubler are used, and to avoid any DC-wander effect, the low cut-off frequency is set to 1 MHz. Output buffers are designed so that they can deliver 200-$mV_{peak\text{-}peak}$ swing to the 50-Ω load of the measurement equipment.

III. Measurement Results

Fig. 6 shows the micro photograph and layout of the fabricated optical receiver. The core size is 0.24×0.1 mm^2,

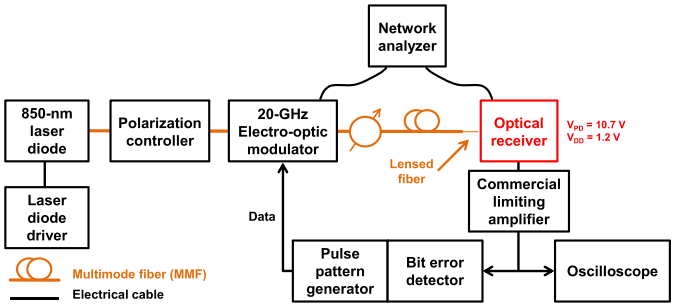

Fig. 7. Measurement setup.

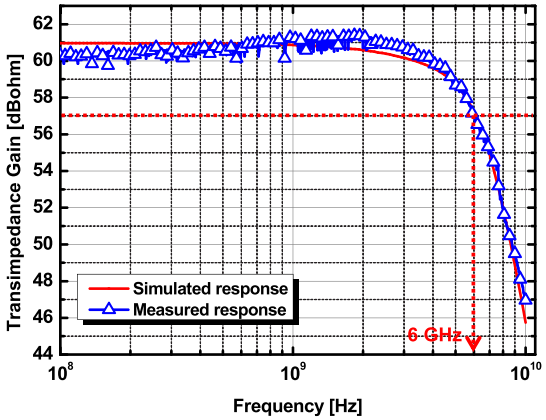

Fig. 8. Measured and simulated frequency response.

and the power consumption of the receiver excluding the output buffer is 13.7 mW with 1.2-V supply voltage.

Fig. 7 shows the measurement setup for photo-detection frequency response and optical data detection. All experiments are done on-wafer. The 850-nm modulated optical signals are generated by an 850-nm laser diode and a 20-GHz external electro-optic modulator. The modulated optical signals are injected into the optical receiver with lensed fiber. For measurement, V_{PD} of 10.7 V is used, which provides the optimal reverse bias voltage of 9.7 V to the CMOS APD. For BER evaluation, a 12.5-Gb/s commercial limiting amplifier is used in order to satisfy the input sensitivity requirement of our equipment.

Fig. 8 shows the measured and simulated photo-detection frequency responses. The transimpedance gain and 3-dB bandwidth is about 60 dBΩ and 6 GHz, and measured response is well matched with simulated response.

Fig. 9 shows the measured BER performances for 10- and 12.5-Gb/s input data. For 10 Gb/s, BER of 10^{-12} is achieved with −6-dBm incident optical power for $2^{31}-1$ PRBS input data and −6.5 dBm for 2^7-1 PRBS data. For 12.5 Gb/s, BER of 10^{-12} and 10^{-11} are achieved with −2-dBm incident optical power for $2^{31}-1$ and 2^7-1 PRBS input data. Inset of Fig. 9 shows measured eye diagrams for 10- and 12.5-Gb/s data transmission with −6- and −2-dBm input power. Table I shows the performance comparison of our optical receiver with previously reported CMOS integrated optical receivers. The table also contains a column, which includes the power consumption and chip area of a LA having 0.076-mm^2 chip area, 38.4-mW power consumption,

TABLE I
PERFORMANCE COMPARISON OF THE REPORTED CMOS OPTICAL RECEIVERS

	[4] 11′ JSSC	[7] 12′ JQE	[5] 14′ OE	This work		Estimated work
Technology	180-nm CMOS	130-nm CMOS	130-nm CMOS	65-nm CMOS		65-nm CMOS
Structure	*SM-PD + TIA + LA (Inductors)	APD + TIA + **EQ + LA	*SM-APD + TIA + **EQ + LA	APD + TIA (No LA)		APD + TIA + LA (LA is assumed)
Gain (dBΩ)	88	100	104	60		100
Bandwidth (GHz)	5.8	6	8	6		6
Data rate (Gb/s)	10	10	12.5	12.5	10	12.5
BER (PRBS)	10^{-11} (2^7-1)	10^{-12} (2^7-1)	10^{-12} (2^7-1)	10^{-12} (2^7-1)	10^{-12} (2^{31}-1)	N/A
Sensitivity	-6 dBm	-4 dBm	0 dBm	-2 dBm	-6 dBm	N/A
Supply voltage	1.8 V (Circuit) 14.2 V (PD)	1.2 V (Circuit) 10.5 V (PD)	1.3 V (Circuit) 10.5 V (PD)	1.2 V (Circuit) 10.7 V (PD)		1.2 V (Circuit) 10.7 V (PD)
Power	118 mW	66.8 mW	72.4 mW	13.7 mW		52.1 mW
Chip area	0.76 mm^2	0.26 mm^2	0.26 mm^2	0.024 mm^2		0.1 mm^2
***GB/P (Ω/mW)	1235	8982	17512	438		11516
Power efficiency (mW/Gb/s)	11.8	6.68	5.79	1.10	1.37	4.17

*SM PD: spatially-modulated photodetector, **EQ: equalizer, ***GB/P = gain×bandwidth/power dissipation

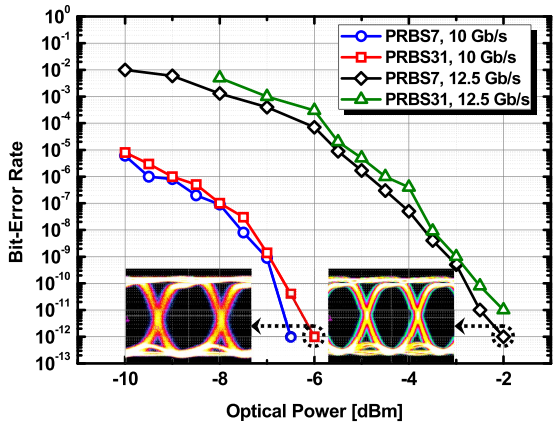

Fig. 9. Measured BER performances with various incident optical power 10- and 12.5-Gb/s data.

20-dB voltage gain and 12.5-GHz bandwidth [7] so that our optical receiver performance can be fairly compared with others. Two different types of figure of merit (FoM) are used in the table. For FoM of gain-bandwidth product per power, our integrated receiver without the LA shows inferior performance. This is due to the fact the LA provides most of the gain. This is needed when the output signals are delivered outside the circuit, but if the optical receiver is fully integrated including CDR circuits, then LA providing high gain is not necessary. For such an application, FoM for power efficiency defined as mW per Gb/s becomes more relevant. Chip area is another important factor for integrated solutions. For our integrated receiver application that does not require a LA. For this FoM, our receiver achieves the lowest value of 1.10. The power efficiency FoM becomes 4.17 if we include above-mentioned LA.

IV. CONCLUSION

A high-speed CMOS integrated optical receiver in which an under-damped TIA compensates the CMOS APD bandwidth limitation is realized in 65-nm CMOS technology. With precise CMOS-APD modeling and careful design of the under-damped TIA, the bandwidth enhancement can be achieved without any additional equalizing circuits or SM PDs. Also, optical data up to 12.5 Gb/s are successfully detected by our integrated optical receiver. The design strategy employed in our receiver should be valuable for various high-performance electronic-photonic integrated circuit applications, in which careful design of both electronic circuits and photonic devices in an integrated manner can provide better performances with less power consumption and smaller system sizes.

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