A Clock and Data Recovery Circuit With Programmable Multi-Level Phase Detector Characteristics and a Built-in Jitter Monitor

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***Abstract*—We demonstrate a clock and data recovery (CDR) circuit having a new type of a multi-level bang-bang phase detector (ML-BBPD). The gain characteristics of our ML-BBPD can be programmed by scanning the dead-zone width of a variable dead-zone BBPD in the time domain. Its linear-like gain characteristics result in less sensitive CDR performance against input jitter and process, voltage, and temperature (PVT) variations. In addition, a built-in on-chip jitter monitor can be easily implemented using our ML-BBPD. A prototype 1.25-Gb/s CDR based on our ML-BBPD with a built-in jitter monitor is realized with 0.18-μm CMOS technology and its performance is successfully verified with measurement.**

***Index Terms*—Clock and data recovery circuit, multi-level bang-bang phase detector, on-chip jitter monitoring.**

I. Introduction

IN SERIAL DATA communication systems, clock and data recovery (CDR) circuits play a critical role for achieving required receiver performance. In particular, the phase detector (PD) should operate on the incoming asynchronous data without producing bit errors. Bang-bang PDs (BBPDs) which produce only the direction of the phase error are widely used especially for high-speed applications due to their simplicity [1], [2]. However, BBPDs have unpredictable and large gain and this makes it difficult to achieve optimized CDR performance especially when input signals to BBPDs contain jitters and CDR loop characteristics are susceptible to process, voltage, and temperature (PVT) variations [3]. CDRs with linear PDs suffer less from these problems, but it is difficult to realize linear PDs for high-speed applications [4].

Multi-level BBPDs (ML-BBPDs) can provide high-speed operation with more linear-like PD characteristics [5]–[8]. Fig. 1 shows the overall structure of previously reported ML-BBPDs. In this structure, several delayed clock signals are generated and each of them is compared with data at a separate BBPD. When all the BBPD output currents are summed, multi-level PD characteristics can be produced. For such an operation, N BBPDs are required for producing $N+1$ multi levels and, consequently, the resulting CDR circuits require a large chip area and consume a large amount of power. Because of this, previously reported ML-BBPDs have a very limited number of multi levels of PD gain [7], [8].

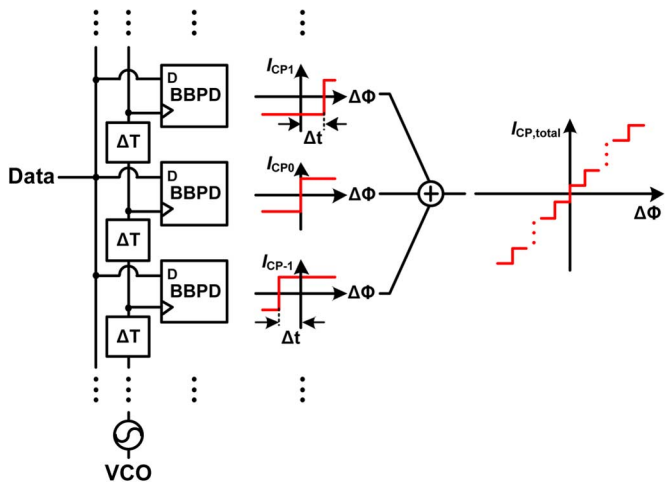

Fig. 1. Structure of previously-reported ML-BBPD.

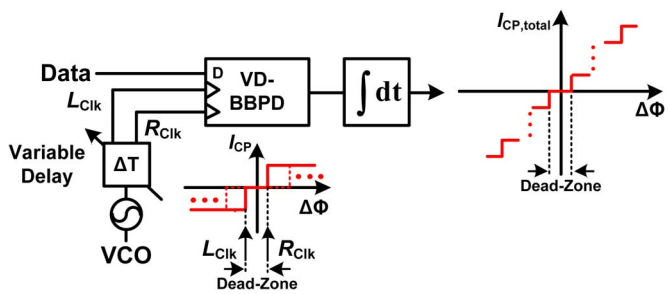

Fig. 2. Structure of newly proposed ML-BBPD.

We propose a novel PD structure that produces step-like PD characteristics by scanning the dead-zone width of one variable dead-zone (VD) BBPD instead of using multiple delayed clock signals. Fig. 2 shows the basic structure of our new ML-BBPD. The VD-BBPD can be realized with the same structure as in [9], where VD-BBPDs are used for reduction of jitter dependence on input data. In our ML-BBPD, the VD-BBPD dead-zone width is controlled by the voltage-controlled oscillator (VCO) clock signal, which experiences a variable amount of delay. Although each data transition experiences a BBPD with a fixed dead-zone width, by slowly scanning the dead-zone width and integrating the resulting charge-pump (CP) currents, the desired

Manuscript received May 07, 2014; revised August 07, 2014 and January 16, 2015; accepted March 07, 2015. Date of current version May 25, 2015. This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) [2012R1A2A1A01009233] and Samsung Electronics. This paper was recommended by Associate Editor N. M. Neihart.

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Digital Object Identifier 10.1109/TCSI.2015.2415180

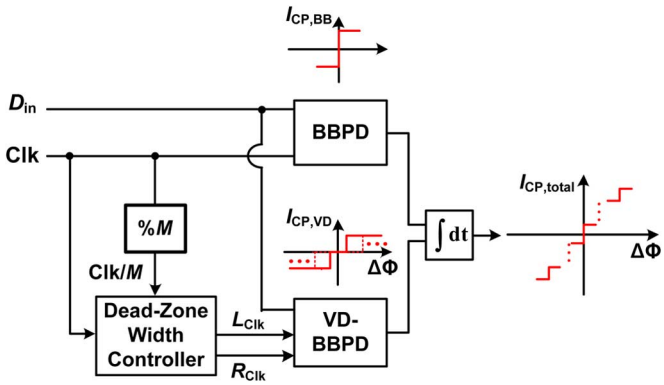


Fig. 3. Block diagram of newly proposed ML-BBPD.

ML-BBPD characteristics can be obtained. Although the same ML-BBPD characteristics can be implemented by supplying the clock signal to a BBPD through variable delay, our structure with the VD-BBPD can provide the additional benefit of a built-in jitter monitor as will be discussed in Section II. The dead-zone width can be either continuously tuned or scanned over discrete steps. In our demonstration, we choose the latter approach so that we can digitally program the scanning profile. With sufficiently large N, we can essentially linearize PD characteristics.

This paper is organized as follows. In Section II, the structure of our ML-BBPD is described in detail and its gain characteristics are analyzed. In addition, its jitter monitoring capability is explained. Section III gives details of circuit implementation for key circuit blocks. Section IV discusses measurement results of a prototype chip. Section V gives the conclusion.

II. PD Structure

A. Step-Like PD Characteristics

Fig. 3 shows the detailed structure of our ML-BBPD CDR. It has a VD-BBPD whose dead-zone width is determined by the amount of separation between $L_{\rm Clk}$ and $R_{\rm Clk}$ provided by the dead-zone width controller. The dead-zone width is scanned over N discrete steps with equal duration for every M clock cycles. An additional BBPD having the conventional structure is included so that we can eliminate the dead-zone in the multi-level characteristics by adding CP currents produced by the BBPD and the VD-BBPD as shown in Fig. 3. The conventional BBPD operation can be realized by turning off the VD-BBPD and this allows us the performance comparison of our ML-BBPD with the conventional BBPD. With this structure, N discrete dead-zone widths produce $2N + 2$ multi levels.

Fig. 4 shows graphically how the total CP current changes in time and produces the desired step-like characteristics. For simplicity in explanation, the case of $N = 3$ having three different dead-zone widths of $2\Phi_1$, $2\Phi_2$, and $2\Phi_3$ provided by VD-BBPD is used as an example. Fig. 4(a) shows four different cases of data transition timing relative to the clock. Case I has data transition within Φ_1, Case II between Φ_1 and Φ_2, Case III between Φ_2 and Φ_3, and Case IV out of Φ_3. When the dead-zone width is scanned in $N = 3$ steps from $2\Phi_1$ to $2\Phi_3$, the sum of $I_{\rm CP,BB}$ and $I_{\rm CP,VD}$ shows different time-dependent characteristics for different cases as shown in Fig. 4(b). $I_{\rm CP,VD}$ is produced only when data transition is out of VD-BBPD dead zone whereas

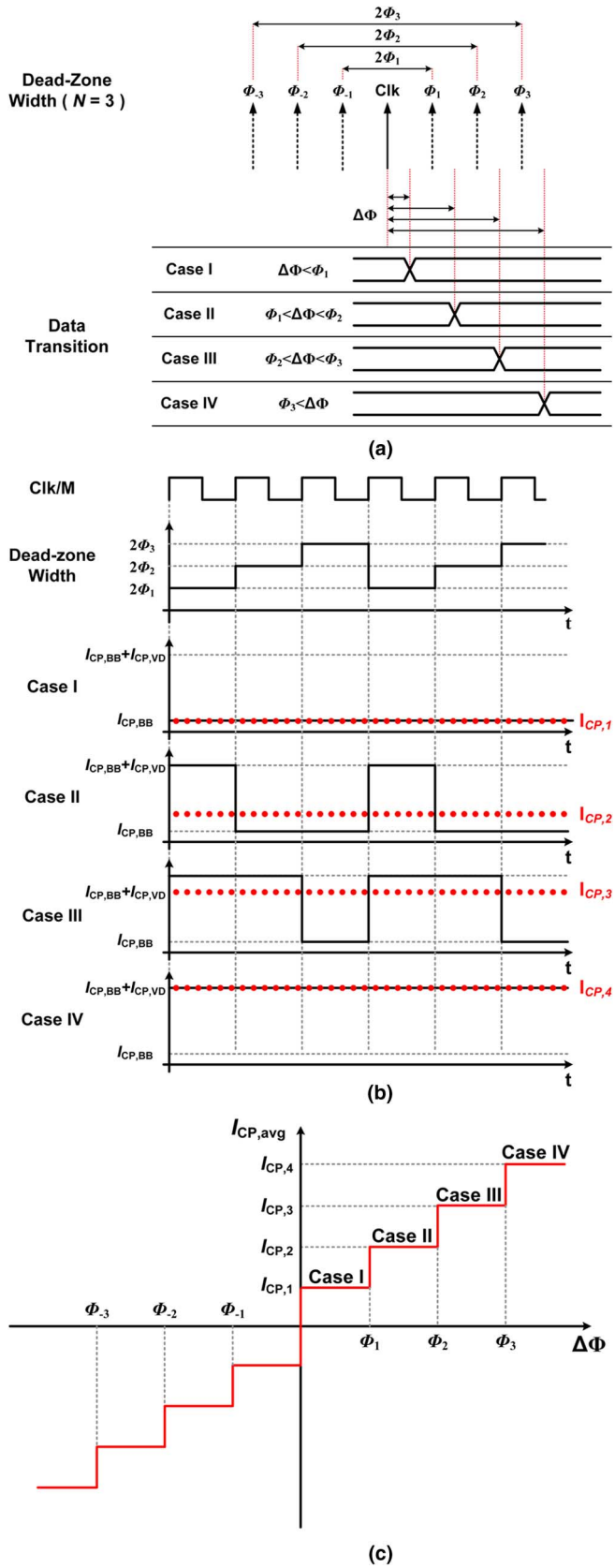


Fig. 4. (a) Four different cases of data transition with different dead-zone width; (b) changes in CP currents; (c) ML-BBPD characteristics.

$I_{\rm CP,BB}$ is constant. The whole operation repeats itself every $M \times N$ clock cycles, and when the total CP currents are properly integrated, different average CP currents are produced for

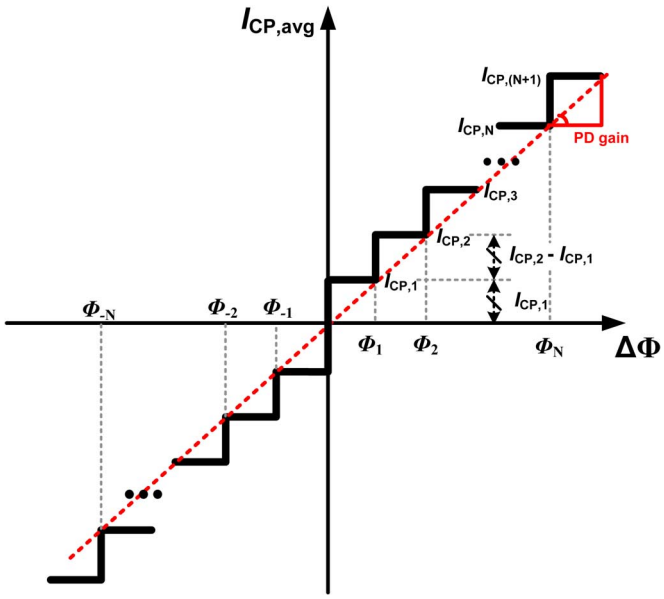


Fig. 5. Step-like PD characteristics.

different amounts of phase differences between data and clock, resulting in step-like PD characteristics as shown in Fig. 4(c).

Values for M and N should be determined with consideration for the trade-off between implementation complexity and performance. As N becomes larger, PD gain becomes more linear-like. However, this comes at the cost of more complicated phase interpolators since finer phase steps and more control bits are required. When M becomes smaller, ML-BBPD detects more data transitions but this requires higher frequency operation of phase interpolators and digital blocks. In addition, N and M should be properly selected so that spurs due to VCO control voltage ripples caused by periodically fluctuating CP currents can be avoided. This is possible if the spur frequency lies outside the CDR loop bandwidth. Since dead-zone width changes every $(M \times N)/f_{\mathrm{Clk}}$ seconds, above requirement can be expressed as

$$\omega_{3\ \mathrm{dB}} \leq \frac{2\pi \times f_{\mathrm{Clk}}}{M \times N} \tag{1}$$

where $\omega_{3\ \mathrm{dB}}$ represents the CDR loop bandwidth.

B. PD Gain Analysis

In CDR operation, $I_{\mathrm{CP,n}}$, the average CP current produced when the phase error is $\Phi_{\mathrm{n-1}} < \Delta\Phi < \Phi_{\mathrm{n}}$, is influenced by D_{P}, the probability for data transition, as well as P_{DZ}, the fraction of time VD-BBPD has the corresponding dead-zone width. Then, $I_{\mathrm{CP,n}}$ can be expressed as

$$I_{\mathrm{CP,n}} = D_{\mathrm{P}}\left(I_{\mathrm{CP,BB}} + (n-1) \times P_{\mathrm{DZ}} \times I_{\mathrm{CP,VD}}\right), \tag{2}$$

where $I_{\mathrm{CP,BB}}$ and $I_{\mathrm{CP,VD}}$ are the charge-pump current produced by the BBPD and the VD-BBPD, respectively. Here, $D_{\mathrm{P}} = 0.5$ for random data input and $P_{\mathrm{DZ}} = 1/N$ as there are N different dead-zone widths. In order to make multi-levels with the identical step size, $I_{\mathrm{CP,2}} - I_{\mathrm{CP,1}}$ should be equal to $I_{\mathrm{CP,1}}$ as shown in Fig. 5. This along with (2) tells us

$$I_{\mathrm{CP,BB}} = \frac{1}{N} \times I_{\mathrm{CP,VD}}. \tag{3}$$

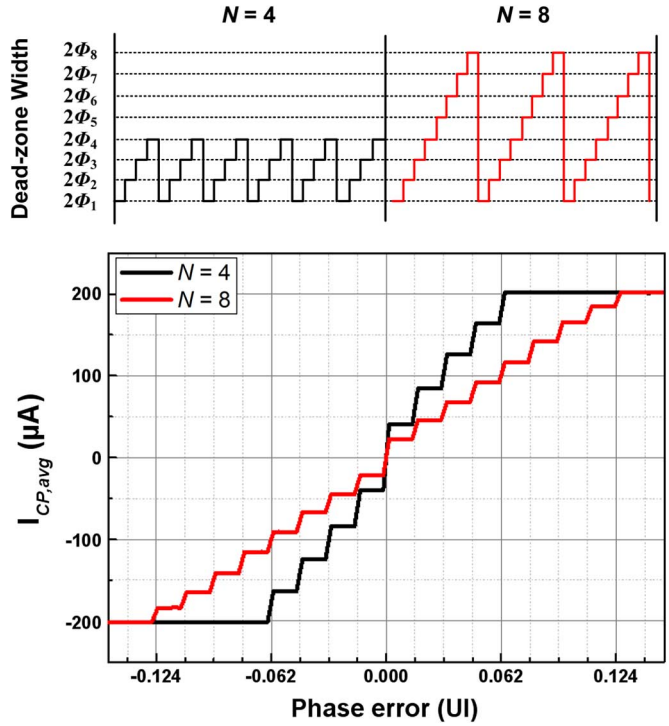


Fig. 6. PD characteristics for different dead-zone width scanning profile.

The difference between two adjacent levels can be determined from (2) as

$$I_{\mathrm{CP,(n+1)}} - I_{\mathrm{CP,n}} = 0.5\left(\frac{1}{N} \times I_{\mathrm{CP,VD}}\right). \tag{4}$$

Then, $K_{\mathrm{ML-BBPD}}$, the gain for our ML-BBPD, can be approximated as

$$K_{\mathrm{ML-BBPD}} = \frac{I_{\mathrm{CP,(n+1)}} - I_{\mathrm{CP,n}}}{\Phi_{\mathrm{n}} - \Phi_{\mathrm{n-1}}} = \frac{0.5 I_{\mathrm{CP,VD}}}{\Phi_{\mathrm{n}} - \Phi_{\mathrm{n-1}}}\frac{1}{N}. \tag{5}$$

The above equation tells us that $K_{\mathrm{ML-BBPD}}$ can be changed by N, which can be easily controlled when the dead-zone width controller is digitally implemented. Fig. 6 shows the behavior-level simulation results for ML-BBPD characteristics for two different dead-zone width scanning profiles having $N = 4$ and $N = 8$. The simulation is done for $M = 8$ and $f_{\mathrm{Clk}} = 1.25$ GHz.

BBPD gain characteristics are smoothed out by jitters inherent in input data and oscillator outputs and also by meta-stability of samplers, causing uncertainty where the phase error is zero [10]. In order to determine how above-determined gain characteristics are influenced by input jitters, behavior-level simulations are done for BBPD and our ML-BBPD gain characteristics with different amounts of input jitters. The simulation results are shown in Fig. 7. For ML-BBPD simulation, a PD having ideal samplers with infinite sensitivity is used with $N = 8$, $M = 8$, and $f_{\mathrm{Clk}} = 1.25$ GHz. As can be seen in the figure, the gain characteristics of our ML-BBPD do not change much with input jitters unlike those of BBPD.

C. Jitter Monitoring

Our ML-BBPD provides another benefit of jitter monitoring capability without much additional hardware. The accumulated output signals of VD-BBPD within our ML-BBPD can be used

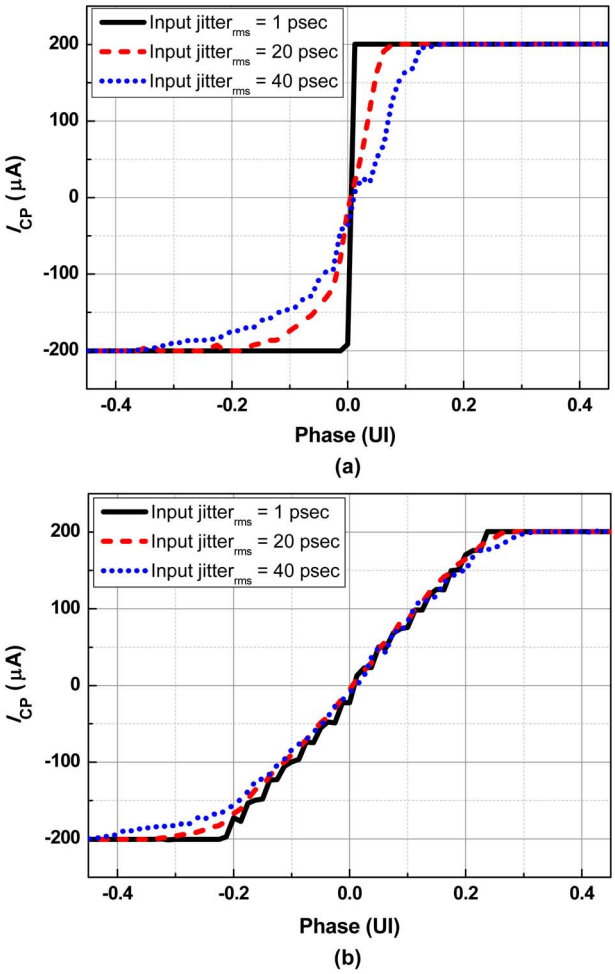


Fig. 7. (a) BBPD gain with input jitter. (b) ML-BBPD gain with input jitter.

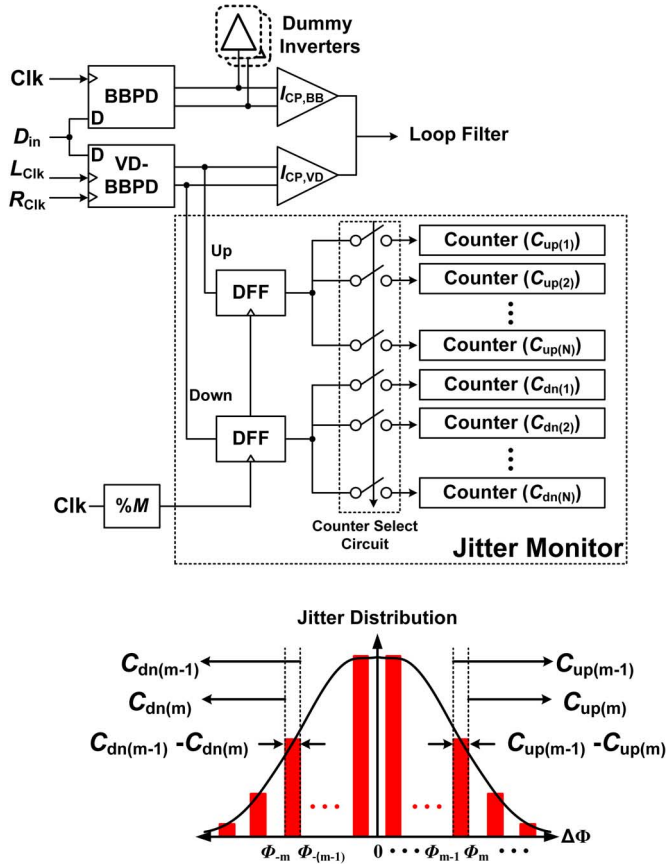


Fig. 8. Jitter monitor block diagram.

for generating jitter histograms since they contain the information regarding whether the data transition is inside or outside the VD-BBPD dead-zone at a given moment. Fig. 8 shows the block diagram of the jitter monitor, which takes output signals from VD-BBPD and stores jitter distribution information in counters. Data transitions outside the m-th dead-zone having the range of $\Phi_{-\mathrm{m}}$ to Φ_{m} are counted and stored in $C_{\mathrm{up(m)}}$ for $\Delta\Phi > \Phi_{\mathrm{m}}$, and in $C_{\mathrm{dn(m)}}$ for $\Delta\Phi < \Phi_{-\mathrm{m}}$. Then, the number of transitions in phase interval $\Phi_{\mathrm{m-1}}$ to Φ_{m} can be determined by subtracting $C_{\mathrm{up(m)}}$ from $C_{\mathrm{up(m-1)}}$. The number of transitions between 0 to Φ_1 is obtained by subtracting $C_{\mathrm{up(1)}}$ from C_0 representing the total number of transitions for $\Delta\Phi > 0$, which can be determined as

$$C_0 = \frac{C_{\mathrm{total}}}{4 \times N} \tag{6}$$

where C_{total} is the total number of samples. Because the transition probability is 0.5 and the probability for up or down is also 0.5, C_{total} should be divided by 4. Since $C_{\mathrm{up(m)}}$ and $C_{\mathrm{dn(m)}}$ are counted only when the dead-zone width is $\Phi_{-\mathrm{m}} < \Delta\Phi < \Phi_{\mathrm{m}}$, C_{total} should be also divided by N. The number of transitions for $\Phi_{-1} < \Delta\Phi < 0$ can be determined by subtracting $C_{\mathrm{dn(1)}}$ from C_0. During jitter monitoring, our ML-BBPD CDR continuously maintains its operation. Dummy inverters are added after the BBPD in order to balance the load capacitance for both types of PDs, as shown in Fig. 8.

Our jitter monitoring technique has several advantages compared to previous works [11]–[13]. First of all, it does not require much additional power because there is a significant amount of hardware sharing between VD-BBPD and the jitter monitor. It does not require high-speed comparators and phase controllers as most previously reported jitter monitors do. In addition, the complexity of the phase generator can be significantly reduced. In conventional jitter monitors, the phase generator should provide more than 1-UI phase range since the initial phase error is unknown. With our technique, the initial phase error is statistically zero due to the CDR operation. However, the jitter distribution provided by our jitter monitor is in reference to the retimed clock and it is not able to subtract/exclude CDR jitter due to input jitter.

III. Circuit Implementation

Fig. 9 shows the block diagram of 1.25-Gb/s full-rate CDR circuit with the proposed ML-BBPD and jitter monitor. An off-chip resistor and a capacitor are used for the loop filter so that we can easily modify the loop filter dynamics for evaluation purpose. The BBPD and VD-BBPD are realized with Alexander PDs [14]. The BBPD operates with Clk, whereas VD-BBPD with L_{Clk}, and R_{Clk}. The CDR is designed in 0.18-μm CMOS technology. In our circuit implementation, N is programmable from 4 to 8, $M = 32$, and $f_{\mathrm{Clk}} = 1.25$ GHz. A very conservative value for f_{Clk} is chosen so that digital circuits in our CDR do not suffer any unforeseen problems and the functionality of our CDR can be guaranteed. One undesirable effect is

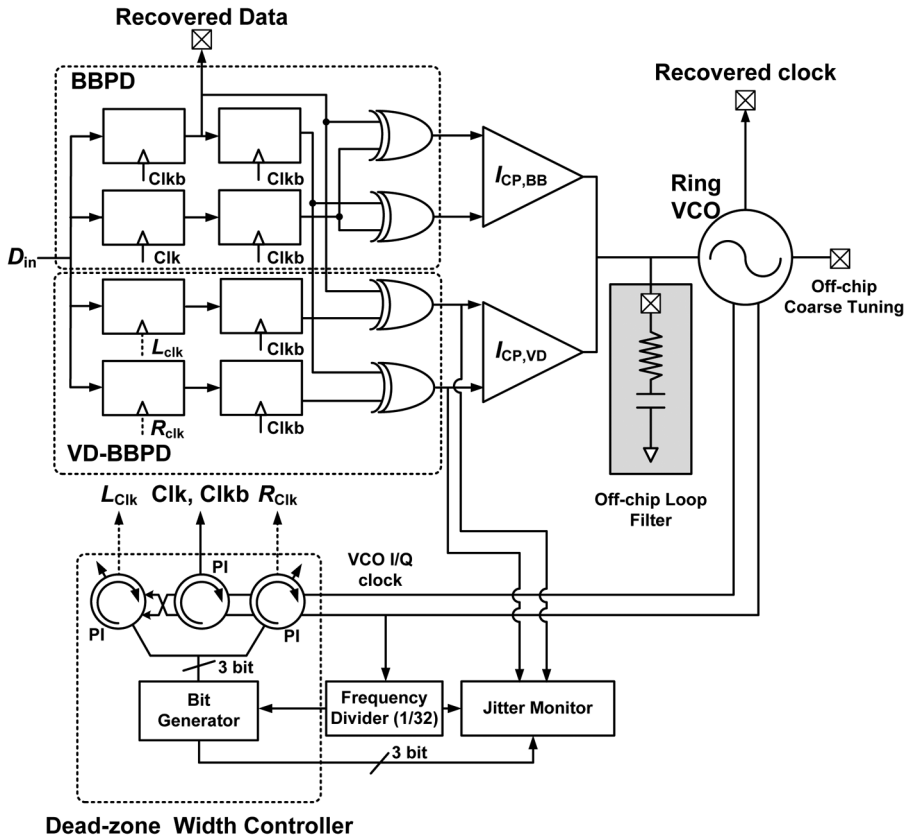


Fig. 9. CDR architecture with jitter monitor.

that our selection of above values does not satisfy (1), which results in spurs in the spectrum of recovered clock signals as will be shown in Section IV.

A. VCO

Fig. 10 shows the schematics of the 2-stage pseudodifferential ring-type VCO with Lee-Kim delay cell [15] used in our design. The VCO is controlled by externally supplied V_{Coarse} for coarse tuning and V_{fine} connected to the loop filter for phase acquisition. By supplying the V_{Coarse} externally, locking point variation can be realized directly to prove insensitivities of ML-BBPD CDR to the variation of K_{VCO}. For correcting duty-cycle distortion, a feed-forward duty cycle corrector is used [15].

B. Dead-Zone Width Controller

The dead-zone width controller is composed of three phase interpolators (PIs), a bit generator, and a frequency divider as shown in Fig. 9. The PI operates with I/Q signals supplied by the VCO. Two of three PIs are used for generating L_{Clk} and R_{Clk} for VD-BBPD. Each of L_{Clk} and R_{Clk} provide clock signals with up to 8 different phases, allowing up to $N = 8$ or 18 multi levels in PD characteristics. The PI has the phase resolution of 1/64 UI corresponding to 13 ps and the maximum dead-zone phase is 1/8 UI. The clock signal with the desired phase is selected by 3-bit control signal provided by the bit generator. The center PI is used for generating clock signals for the BBPD.

Fig. 11 shows the schematic diagram of PI used in the prototype chip. For improving PI linearity, the current source of two

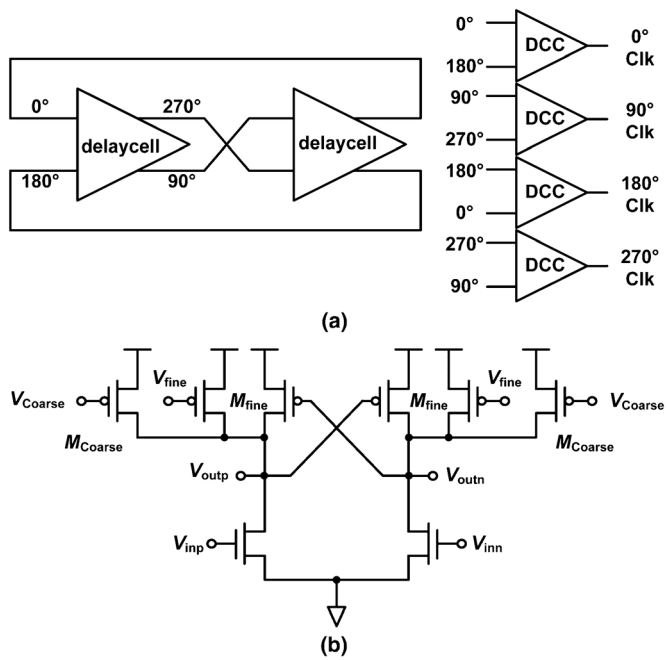


Fig. 10. (a) VCO (b) modified Lee-Kim delay cell.

differential pairs is realized with thermometer controlled elements (T00∼T07) generated by a 3-bit binary to thermometer decoder. The bit generator is synthesized with standard cells. It produces thermometer codes for controlling the number of dead-zone width which can control the PD gain easily. A 39.0625-MHz signal generated from 1/32 frequency divider is used as its clock.

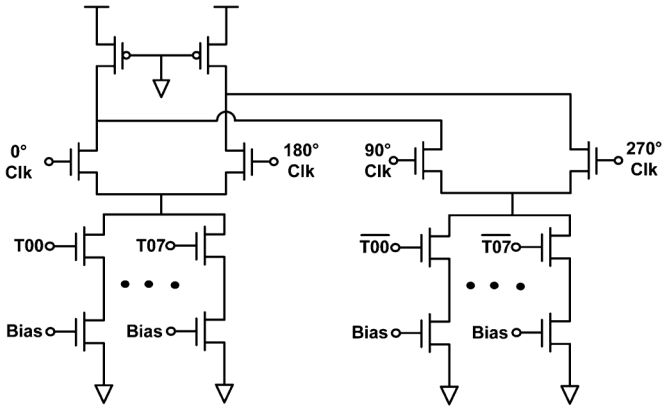


Fig. 11. Phase interpolator.

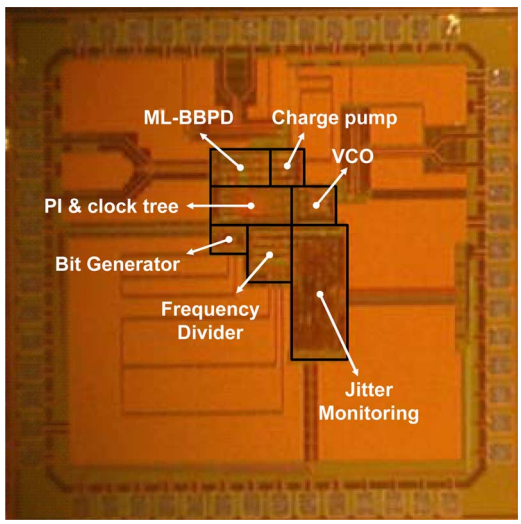


Fig. 12. Chip microphotograph.

TABLE I
POWER AND AREA CONSUMPTION

Blocks	Chip Area (mm^2)	Power (mW)
ML-BBPD	0.017	14.4
PI & Clock Tree	0.017	9
Charge Pump	0.007	1.8
VCO	0.005	10.8
Bit Generator	0.004	0.6
Frequency Divider	0.015	1.5
Jitter Monitoring	0.042	1.5

C. Jitter Monitoring

The jitter monitor is composed of samplers, counter selector, and 16 counters as shown in Fig. 8. Eight counters are used for monitoring early data compared to the clock signal and 8 for late data. The control code from the bit generator selects the counters used for accumulating VD-BBPD output signals. The jitter monitor is also synthesized with standard cells and operates with 39.0625-MHz clock.

IV. Measurement Results

A prototype chip is fabricated in 0.18-μm CMOS technology. The chip microphotograph is shown in Fig. 12. The power consumption and the area of each block are given in Table I.

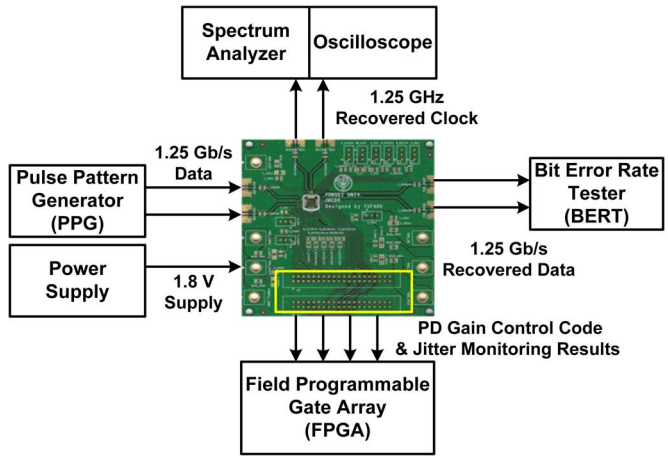


Fig. 13. Measurement setup for evaluating the CDR performance.

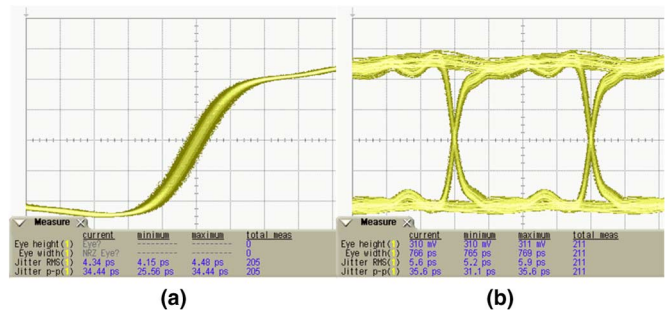


Fig. 14. Eye diagram of (a) recovered clock and (b) recovered data.

Fig. 13 shows the measurement setup for evaluating the CDR performance. The bare-chip is mounted on PCB and wire bonded. The pattern pulse generator (PPG) generates 1.25-Gb/s $2^{31}-1$ PRBS pattern for CDR input. A digital sampling scope is used to measure the recovered clock and data, whose eye diagrams are shown in Fig. 14. A bit error rate tester is also used to confirm the CDR does not generate any error. A FPGA board is used to set the control code for the desired dead-zone width profile and collect the accumulated counter values from the on-chip jitter monitor.

In order to confirm our ML-BBPD provides the advantages of less sensitive CDR loop dynamics compared to simple BBPD, we performed two comparison measurements in which the loop characteristics are intentionally changed and their influence on the recovered clock jitters are measured for CDRs having ML-BBPD and BBPD. Two types of CDRs used for the comparison are identical except the values for N; $N = 0$ for BBPD CDR and $N = 8$ for ML-BBPD CDR.

Fig. 15 shows the measured rms jitters of retimed clock when K_{VCO}, the VCO gain, varies from 90 MHz to 230 MHz. Changes in K_{VCO} are induced by externally setting the VCO coarse tuning voltage. For each VCO coarse tuning voltage, K_{VCO} is measured. This measurement emulates K_{VCO} variation due to shifting of the VCO locking voltage due to PVT variation or wide VCO tuning range [16], [17]. As shown in the figure, the rms jitter of recovered clock for BBPD CDR shows significant increase with K_{VCO}. This is because K_{VCO} variation changes the values of CDR loop damping factor and natural frequency, which affects the amount of recovered-clock jitter. In contrast, ML-BBPD CDR does not show any significant amount of change with K_{VCO}. This clearly demonstrates

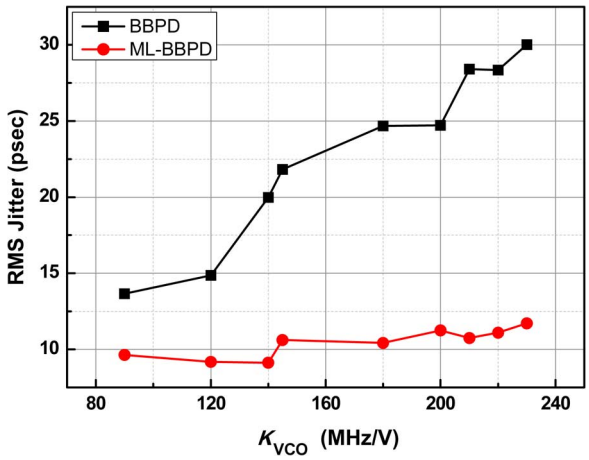
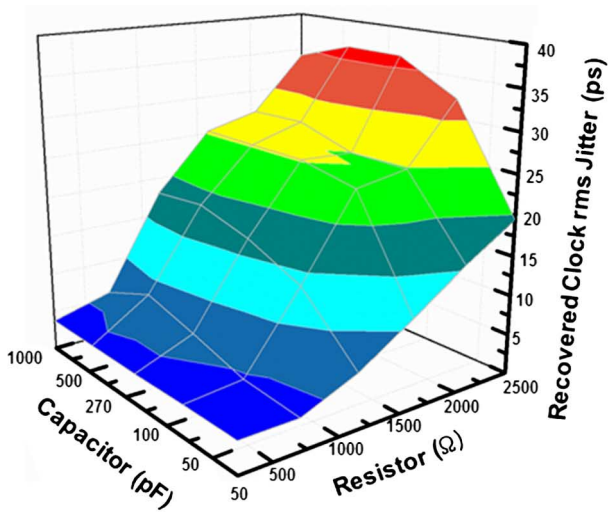


Fig. 15. K_{VCO} variation according to control voltage.



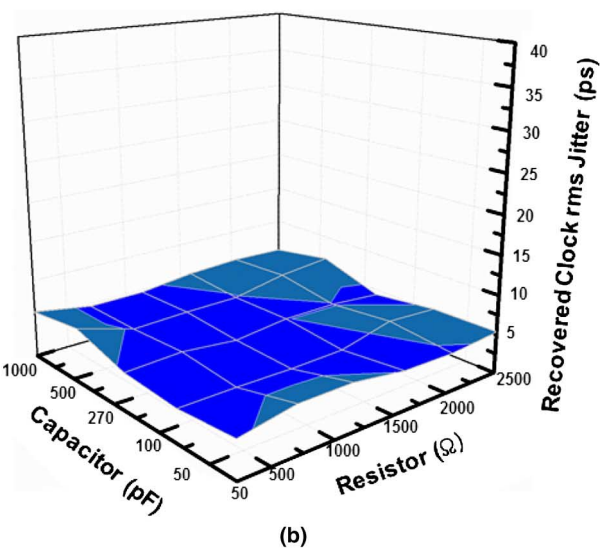
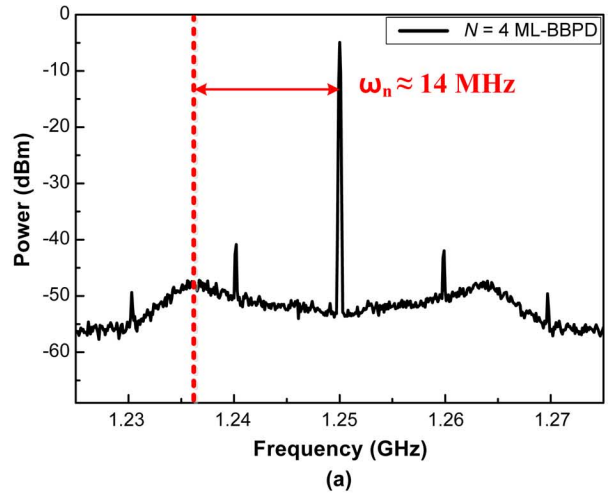


Fig. 16. Measured recovered clock jitter: (a) BBPD; (b) ML-BBPD.

that the gain characteristic of our ML-BBPD is insensitive to K_{VCO} variation.

Fig. 16 shows the measured rms jitters of retimed clock when R, C values for the loop filter vary. This measurement emulates changes in loop filter characteristics due to PVT variation.



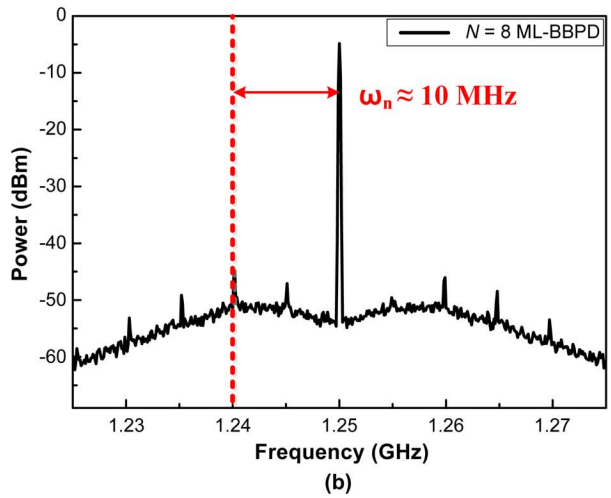


Fig. 17. Measured spectra of recovered clock: (a) $N = 4$ ML-BBPD; (b) $N = 8$ ML-BBPD.

Although the range of R, C variation covered in this measurement is much wider than typical variations due to PVT variation, Fig. 16 clearly demonstrates that our ML-BBPD CDR shows much more robust performance against changes in loop filter characteristics.

In order to investigate how the CDR performance is influenced by the difference in multi-level numbers, the loop bandwidth is compared for CDRs with different N values. As shown in (5), CDRs with different N values have different PD gain and this should result in different CDR loop bandwidth. Fig. 17 shows measured spectra of recovered clock signals for $N = 4$ and $N = 8$ CDR along with their loop bandwidth estimation. According to (5), $N = 4$ CDR should have twice as large PD gain as $N = 8$, and this should result in $\sqrt{2}$ larger CDR loop bandwidth since CDR bandwidth is proportional to $\sqrt{K_{PD}}$ [14]. Fig. 17 clearly shows that $N = 4$ CDR has about 1.4 times larger bandwidth than $N = 8$.

In addition, spurs are produced having the spur frequency given by the right side of (1). In our implementation, $f_{\mathrm{Clk}} = 1.25$ GHz and $M = 32$. These design decision was made so that synthesized digital blocks can operate reliably at 39.0625 MHz. Consequently, $N = 4$ CDR generates spurs at 9.76 MHz and its harmonics, and $N = 8$ CDR has spurs at 4.88 MHz and its harmonics. As can be seen in Fig. 17, these spurs are clearly

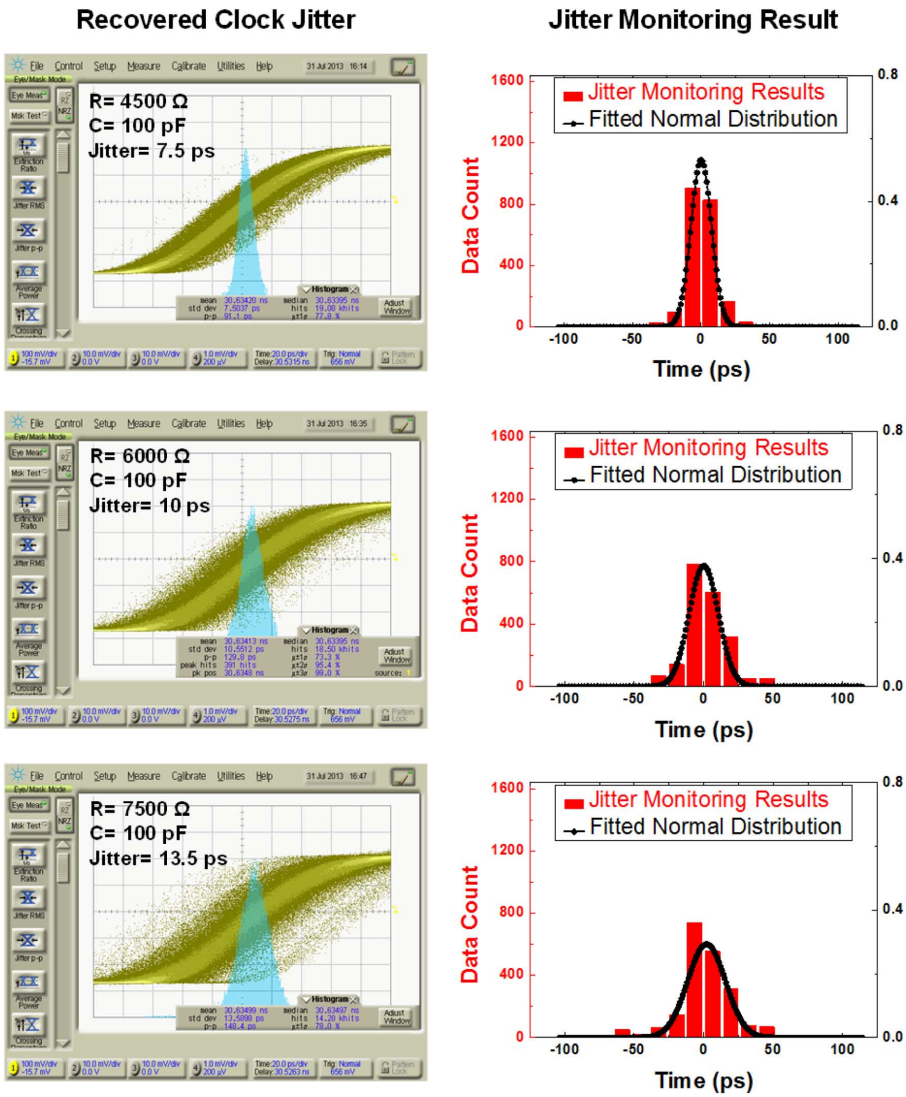


Fig. 18. Measured jitter distributions and jitter histograms obtained with on-chip jitter monitoring.

TABLE II
PERFORMANCE COMPARISON WITH ML-BBPD CDRS

	[5]	[6]	[7]	This work
Data Rate	5 Gb/s	5 Gb/s	1.25 Gb/s	1.25 Gb/s
Technology	180-nm CMOS	90-nm CMOS	180-nm CMOS	180-nm CMOS
Supply Voltage	1.8 V	1.2 V	1 V	1.8 V
Power	80 mW	16.8 mW	68 mW	39.6 mW
Area	N/A	0.3 mm^2	N/A	0.107 mm^2
Jitter of Recovered Clock (UIrms)	2.4 %	0.88 %	1 %	0.54 %
PD type	ML-BBPD	ML-BBPD	ML-BBPD	ML-BBPD
Rate of PD	1/2 rate	1/4 rate	Full rate	Full rate

observed since they are within the CDR bandwidth. These can be avoided if a larger value for f_{Clk}/M is used.

Fig. 18 shows oscilloscope-measured recovered clock jitter distributions for CDRs having three different loop filter R, C values and jitter histograms obtained from our on-chip jitter monitor with $N = 8$ and $C_{\mathrm{total}} = 32\,768$. On top of histograms, the normal distributions having the measured mean and variance values are added. As can be seen in the figure, our histograms match well with the normal distributions. The slight skew in jitter histograms is caused by mismatch among three PIs in our circuit.

The performance of our ML-BBPD CDR is compared in Table II with those of previously reported CDRs having ML-BBPD. As can be seen in the figure, our CDR produces the smallest rms jitter for the recovered clock and consumes less power than other CDRs fabricated with the same CMOS technology. In addition, our ML-BBPD CDR contains the on-chip jitter monitoring capability, which other CDRs do not.

V. Conclusion

We demonstrate a 1.25-Gb/s CDR circuit with a novel ML-BBPD having multi-level gain characteristics obtained by scanning of dead-zone width of a VD-BBPD discretely and periodically. Our ML-BBPD can provide programmable linear-like PD characteristics and, consequently, robustness against input jitters and any CDR loop characteristic fluctuation. In addition, it allows simple implementation of a built-in jitter monitor. A prototype CDR realized in 0.18-μm CMOS technology confirms the operation and the advantages of our new ML-BBPD.

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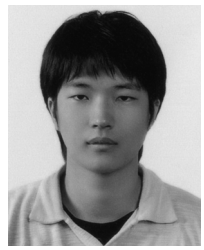

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