Bandwidth Improvement of CMOS-APD With Carrier-Acceleration Technique

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***Abstract*— We present a silicon avalanche photodetector (APD) based on multiple P^+/N-well junctions fabricated in standard complementary metal–oxide–semiconductor (CMOS) technology. In order to overcome the photodetection-bandwidth limitation of the CMOS-APD based on P^+/N-well junction, carrier-acceleration technique is proposed. With this technique, the photogenerated carriers in the charge-neutral N-well region are accelerated by the extrinsic electric field. To induce the extrinsic electric field inside N-well, the CMOS-APD is designed with multiple junctions to reduce the distance between two different N-well biasing contacts. Its performance is simulated and measured with different bias voltages applied to N-well, and it is demonstrated that the CMOS-APD with the carrier-acceleration technique provides higher photodetection bandwidth.**

***Index Terms*— Avalanche photodetector (APD), avalanche photodiode, carrier acceleration, multiple junction, optical interconnect, photodetection bandwidth, silicon photodiode, silicon photonics, standard CMOS technology.**

I. Introduction

THERE are great research interests in developing high-speed monolithic optical receivers based on standard complementary metal-oxide-semiconductor (CMOS) technology for various 850 nm short-distance optical-communication and optical-interconnect applications [1]–[7], because the optical receivers developed in standard CMOS technology can take full advantage of the powerful CMOS technology such as low-cost and high-volume fabrication. In addition, they can provide better performance by eliminating parasitic pad capacitances and bonding wire inductances unavoidable in hybrid approaches [8]–[10]. In order to realize high-speed optical receivers in standard CMOS technology, development of CMOS-compatible silicon photodetectors (CMOS-PDs) having large photodetection bandwidth is essential. However, CMOS-PDs have disadvantage of small photodetection bandwidth due to large optical penetration depth and narrow depletion regions caused by high doping concentrations. A large portion of the incident light is absorbed in charge-neutral regions, outside depletion regions, and transport of photogenerated carriers in this region is dominated by the slow diffusion process, which severely limits the CMOS-PD photodetection bandwidth in the MHz range.

Several methods have been tried to overcome the inherent drawbacks of the CMOS-PDs by reducing the effect of the slow diffusion process [11]–[15]. We have investigated CMOS-compatible avalanche photodetectors (CMOS-APDs) based on P^+/N-well and N^+/P-well junctions to exclude the slow diffusion currents from the P-substrate region, resulting in large photodetection bandwidth in the GHz range along with high responsivity by avalanche gain [14], [15]. Nevertheless, we have found the photodetection bandwidth of the CMOS-APDs is still limited by the diffusion process in the charge-neutral region of the well region, because the diffusion time is much larger than drift time in the depletion region and device RC time constant [15]. To achieve further improvement of the CMOS-APD photodetection bandwidth, we need to reduce the effect of the slow diffusion process in the well region.

In this letter, we propose a new CMOS-APD based on multiple P^+/N-well junctions with carrier-acceleration technique. The carrier-acceleration technique was reported with a CMOS-PD integrated in an optical receiver, but only the bit error rate of the receiver was reported with the technique without any characterization of the CMOS-PD [12]. To the best of our knowledge, no CMOS-APD has yet to be demonstrated with the carrier-acceleration technique. In addition, the multiple-junction structure proposed in this work reduces lateral transit time of the photogenerated carriers and also increases the effect of the carrier-acceleration technique. By applying different bias voltages to N-well, an extrinsic electric field is produced inside the charge-neutral region of N-well, and this accelerates the photogenerated-carrier migration, resulting in reduction of the carrier transit time. With this, we achieve photodetection bandwidth of 5.6 GHz, which corresponds to 40 % bandwidth enhancement compared to the same device without the carrier-acceleration technique.

II. Device Description

Fig. 1 shows the cross section of the proposed CMOS-APD having multiple P^+/N-well junctions, which is fabricated with standard CMOS technology available within IHP 0.25 μm BiCMOS process without any design rule violations [16].

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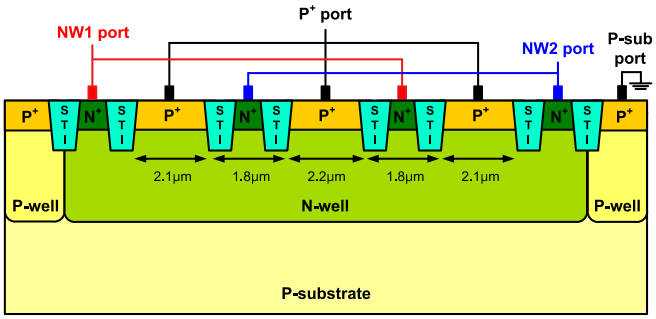

Fig. 1. Cross section of the CMOS-APD based on multiple P^+/N-well junctions. Two different bias voltages are applied to NW1 and NW2 ports to improve its photodetection bandwidth with an extrinsic electric field inside the charge-neutral N-well region.

In order to operate as an APD, the P^+/N-well junctions are reverse biased by applying a negative voltage to the P^+ port, and connecting P-substrate to the ground. Photocurrents are extracted from the P^+ port located inside the N-well region to exclude slow diffusion currents from the P-substrate region. Shallow trench isolation (STI) guard rings (GRs) are formed at the edge of the each junction because the GR structure provides high gain without premature edge breakdown [17]. In order to apply bias voltages to N-well for implementing the carrier-acceleration technique, N^+ contacts are included between the junctions. The active-region width of each junction should be reduced as much as possible because a shorter distance between NW1 and NW2 ports provides a larger electric field inside the charge-neutral N-well region, but there is a trade-off between the electric field and optical coupling loss. If the number of multiple junctions increases with the reduction of the active-region width, the electric field increases due to the decreased lateral distance between NW1 and NW2 ports, but the optical coupling loss also increases due to the increase of the redundancy areas for N^+ contact and STI regions, required for each junction. We implemented our CMOS-APD with three P^+/N-well junctions having active-region width of about 2.1 μm as shown in Fig. 1, and the measured optical coupling loss of this structure is about 24 % compared to the non-multiple structure. It has the total active area of 10×10 μm^2, and it is formed by blocking the self-aligned silicide (salicide) process.

Fig. 2 shows the movement of photogenerated holes in N-well without and with applied bias voltages to N-well. As shown in Fig. 2(a), the photogenerated carriers transport by two different processes: diffusion in the charge-neutral region and drift in the depletion region. The slow hole diffusion process in the charge neutral N-well region limits the CMOS-APD photodetection bandwidth. On the other hand, as shown in Fig. 2(b), with a voltage applied between NW1 and NW2 ports, an electric field is produced inside the charge neutral N-well region, and the photogenerated holes are accelerated by the extrinsic field, resulting in the enhanced photodetection bandwidth.

III. Simulation and Measurement Results

Fig. 3 shows the results of simulation carried out for analyzing the effect of the carrier-acceleration technique.

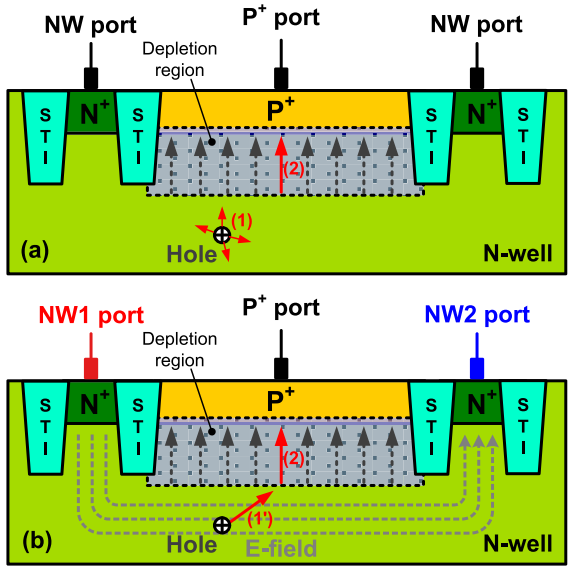

Fig. 2. Movement of photogenerated carriers in N-well (a) without and (b) with an extrinsic electric field inside the charge neutral N-well region.

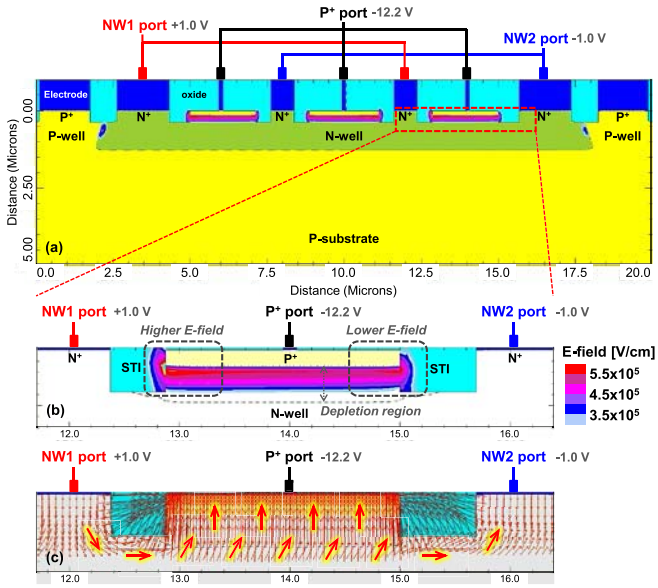

Fig. 3. (a) Simulated electric field profile of the CMOS-APD. +1.0 V and −1.0 V bias voltages are applied to NW1 and NW2 ports, respectively, at the reverse bias voltage of 12.2 V for the multiple P^+/N-well junctions. (b) Zoom-in plot of electric field profile. (c) Zoom-in plot of electric field lines.

The simulation is done with MEDICI using doping profiles provided by IHP [16]. In the simulation, a reverse bias voltage of 12.2 V is applied to the multiple P^+/N-well junctions by applying −12.2 V to the P^+ port, which is about 0.1 V below its avalanche breakdown voltage, and +1.0 V and −1.0 V are applied to NW1 and NW2 ports, respectively, which is one bias condition for measurements. Because the different bias voltages are applied to N-well, the electrical potential in N-well varies with the distance between NW1 and NW2 ports, which has a fairly linear behavior [12]. With the NW2 bias voltage of −1.0 V, therefore, the N-well/P-substrate junction doesn't exceed its forward threshold voltage due to the

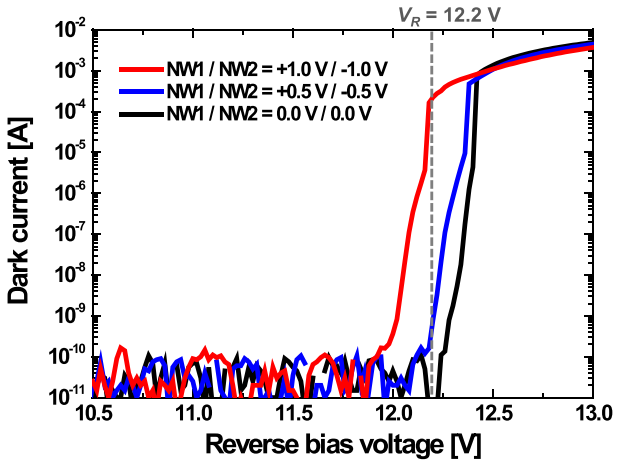

Fig. 4. Dark-current characteristics of the CMOS-APD with 0, 1, and 2 V different bias voltages applied to N-well.

distance between the junction and the NW2 port. However, the device could not operate with a NW2 bias voltage above −1.0 V because then the N-well/P-substrate junction reaches its threshold voltage. As can be seen in Fig. 3(b), the premature edge breakdown at the junction edge is well prevented by the STI GR. In addition, it is clearly seen that the P^+/N-well junction near the NW1 port has higher electric field due to the different voltages applied to NW1 and NW2. Although there is a variation in the electric field at the planar junction, high electric field over 5×10^5 V/cm is achieved all over the junction, which is enough to cause impact ionization in silicon and, consequently, provides large avalanche gain. With the carrier-acceleration technique, as shown by the electric field lines in Fig. 3(c), the CMOS-APD has lateral electric field components inside the N-well region, which can accelerate photogenerated holes in the charge-neutral N-well region.

In order to investigate the effective reverse bias voltage applied to the junction with the different bias voltages applied to N-well for the carrier-acceleration technique, dark-current characteristics are measured with three different conditions. Fig. 4 clearly shows that the breakdown occurs about 0.1 V and 0.25 V earlier with NW1/NW2 = +0.5 V/−0.5 V and NW1/NW2 = +1.0 V/−1.0 V, respectively, due to the higher electric field of the junction near the NW1 port as shown in Fig. 3(b). At the reverse bias voltage of 12.2 V, therefore, the CMOS-APD has high dark current with NW1 = +1.0 V while it still has low dark current with NW1 = +0.5 V.

To verify the photodetection-bandwidth enhancement by the carrier-acceleration technique, photodetection frequency responses are measured at the reverse bias voltage of 12.2 V, which is the optimal bias condition for the frequency response, with different bias voltages applied to N-well. The current-voltage characteristics, responsivity, avalanche gain, and noise characteristics of the P^+/N-well junction CMOS-APD without the carrier-acceleration technique can be found in [18]. For the measurements, 1 mW 850 nm light is injected into the CMOS-APD surface through a lensed fiber having 10 μm diameter. The 1 mW input optical power is used in

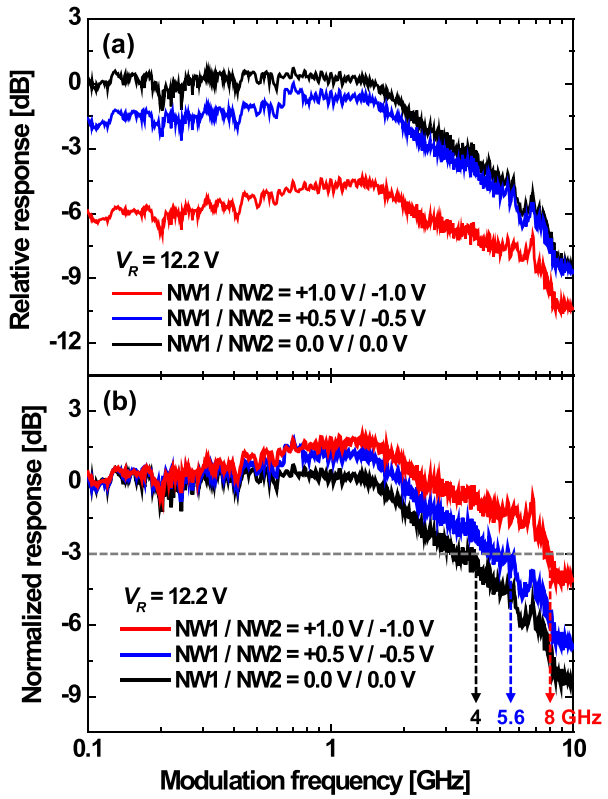

Fig. 5. (a) Relative and (b) normalized photodetection frequency responses of the CMOS-APD with 0, 1, and 2 V different bias voltages applied to N-well.

consideration of the sensitivity range of CMOS integrated optical receivers [6], [19]. A vector network analyzer is used to modulate the optical signal provided by a laser diode with a 20 GHz electro-optical modulator and detect output signals of the CMOS-APD. The measured frequency range is from 100 MHz to 13.5 GHz, and all measurements are done with on-wafer probing at room temperature. Fig. 5 shows measured relative and normalized photodetection frequency responses of the fabricated CMOS-APD for three different bias voltages applied to N-well. As shown in Fig. 5(a), the amount of photodetection response decreases with the increasing bias voltage applied to N-well. This is because the electric field nearby the NW2 port is decreased as shown in Fig. 3(b) and this results in the decrease of the effective ionization rate and, consequently, avalanche gain [17]. Using factor of two correction as Fig. 5(a) shows power measurement results, it shows the responsivity and avalanche gain are decreased by 15 % and 50 % with the carrier-acceleration technique where 1 V and 2 V different bias voltages are applied to N-well, respectively. On the other hand, as shown in Fig. 5(b), it can be clearly observed that the photodetection bandwidth is increased with the increase of the different bias voltage, and this improvement is attributed to the carrier acceleration by the extrinsic electric field. The photodetection bandwidth is improved upto 8 GHz with the 2 V different bias voltage applied to N-well, but it can be inappropriate because it has high dark current at the operation condition as shown in Fig. 4 due to higher electric field nearby the NW1 port. Whereas with the 1 V different bias voltage the proposed device doesn't suffer from the problem of high dark current

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED CMOS-APD WITH CARRIER-ACCELERATION TECHNIQUE AND PERFORMANCE COMPARISON WITH RECENTLY PUBLISHED SILICON APDS IN STANDARD CMOS TECHNOLOGY AT 850 nm WAVELENGTH

	This work	[20] 13'PTL	[15] 13'TED	[21] 13'JQE
Technology	0.25 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	40 nm CMOS
Structure	Multiple P^+/N-well APD	Multiple N^+/P-sub APD surrounded by DNW	P^+/N-well APD	P^+/N-well /P-sub ADPD*
GR	STI	STI	STI	STI
A	$10 \times 10\ \mu m^2$ (Square)	$50 \times 50\ \mu m^2$ (Octagonal)	$10 \times 10\ \mu m^2$ (Square)	$70 \times 70\ \mu m^2$ (Square)
V_R	12.2 V	11.45 V	10.25 V	8.41 V
R	0.2 A/W	0.05 A/W	0.48 A/W	0.84 A/W
BW	5.6 GHz	8.7 GHz	7.6 GHz	0.7 GHz

*ADPD: avalanche double photodiode
DNW: deep N-well, *GR*: guard ring, STI: shallow trench isolation, *A*: total active area, V_R: reverse bias voltage, *R*: responsivity, *BW*: bandwidth

and still achieves 40 % bandwidth enhancement compared to that without the carrier-acceleration technique.

The performance of the proposed CMOS-APD with the carrier-acceleration technique is summarized in Table I. In addition, it compares recently published results of silicon APDs in standard CMOS technology with our work. Compared to [20] and [21], our device shows 4 times better responsivity and 8 times higher photodetection bandwidth, respectively. Compared with our previous work [15], which is based on the same P^+/N-well structure in more advanced CMOS technology, the proposed device shows lower bandwidth mainly because of larger diffusion time due to deeper N-well in 0.25 μm process, but it is expected that higher bandwidth than 7.6 GHz is achieved if the proposed device is realized in the same CMOS technology.

IV. CONCLUSION

We present a photodetection-bandwidth-improved CMOS-APD based on the multiple P^+/N-well junction structure using the carrier-acceleration technique. The multiple structure reduces the lateral transit length of the photogenerated holes in the charge-neutral N-well region and increases the effect of carrier acceleration of the photogenerated holes in the charge-neutral N-well region with the extrinsic electric field. The proposed device performance is measured and analyzed with different bias voltages applied to N-well, and the bias voltage limitation and effect are identified. It is demonstrated that the proposed CMOS-APD with 1 V different bias voltage applied to N-well achieves 5.6 GHz photodetection bandwidth, which is 40 % bandwidth improvement over that without the carrier-acceleration technique.

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