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Low-power 850 nm optoelectronic integrated circuit receiver fabricated in 65 nm complementary metal–oxide semiconductor technology

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Abstract: The authors present a low-power 850 nm Si optoelectronic integrated circuit (OEIC) receiver fabricated in standard 65 nm complementary metal–oxide semiconductor (CMOS) technology. They analyse power consumption of previously reported CMOS OEIC receivers and determine the authors receiver architecture for low-power operation. Their OEIC receiver consists of a CMOS-compatible avalanche photodetector and electronic circuits that include an inverter-based transimpedance amplifier, a tunable equaliser and a post amplifier. With the fabricated OEIC receiver, they successfully demonstrate 8 Gb/s operation with a bit-error rate $<10^{-12}$ at incident optical power of −4.5 dBm. Their OEIC receiver consumes 5 mW with 1.2 V supply voltage. To the best of their knowledge, their OEIC receiver achieves the lowest energy efficiency among 850 nm CMOS OEIC receivers.

1 Introduction

For short-reach optical interconnect applications, various 850 nm optoelectronic integrated circuit (OEIC) receivers fabricated with standard complementary metal–oxide semiconductor (CMOS) technology have been actively investigated over the past decade [1–13]. Most of the previous works focus mainly on realisation of high-speed operations for multi-gigabit data transmission applications, and the achieved data rates have continuously increased over the years as shown in Fig. 1.

Typically, these receivers consist of a CMOS-compatible photodetector (CMOS-PD), a transimpedance amplifier (TIA) and a limiting amplifier (LA). Equalisers are included so that the limited CMOS-PD photodetection bandwidth can be compensated [4–7, 9]. Several different types of CMOS-PDs have been used including a lateral p-i-n PD [3], spatially modulated PDs [4–8, 12] and CMOS-compatible avalanche PDs (CMOS-APDs) based on P^+/N-well junction [9, 13]. Table 1 compares the structure and performance of CMOS-PDs that have been used inside CMOS OEIC receivers.

Previously reported CMOS OEIC receivers consume a large amount of power ranging from several tens to hundreds of milliwatts, which may limit the applicability of CMOS OEIC receivers for certain applications. In this paper, we present the results of our investigation in which we attempt to realise high-speed 850 nm CMOS OEIC receivers having as low-power consumption as possible. We analyse the power budget of previously reported receivers and find that, for 65 nm CMOS technology, a large amount of power can be saved by using inverter-based TIA rather than current-mode logic (CML) TIA. This paper is organised as follows. In Section 2, the power consumption of OEIC receivers is analysed. Section 3 describes building blocks of our CMOS OEIC receiver. Section 4 presents the measurement results and Section 5 gives the conclusion.

2 Design of low-power OEIC receiver

Table 2 shows the power consumption of each building block in two different 10 Gb/s OEIC receivers [8, 9]. The main reason for large power consumption in these receivers is implementation of key blocks in the CML structure, which allows higher and less noisy operation. Then, the question becomes which of these key building blocks can be realised with inverter-based circuits, which can greatly reduce power consumption [14–16], while maintaining high-speed operation.

With 65 nm CMOS technology, we find that TIA can be most easily implemented in the inverter-based structure using shunt-feedback configuration [17] achieving 3 dB bandwidth larger than 5 GHz. Limited bandwidth of CMOS-PD and TIA can be enhanced with a continuous-time linear equaliser (CTLE). However, designing a CTLE in the inverter structure is very challenging because of the large DC gain of inverters. Instead, we implement the CTLE with the CML structure as the CTLE power consumption is relatively small [18]. Realising a high-speed LA in the inverter structure is also difficult because of large DC gain and the offset

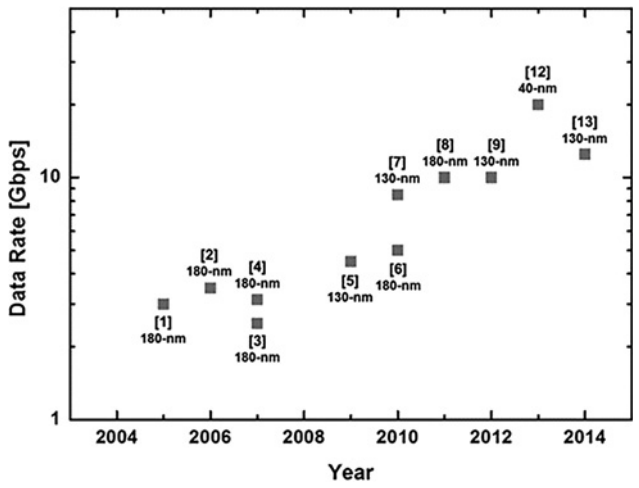

Fig. 1 *Data rates of 850 nm CMOS OEIC receivers*
Also shown are CMOS technologies used for OEIC receiver realisation

problem. Using biasing circuits that control input threshold voltage of the LA can reduce the offset problem [19], but this increases circuit complexity considerably and significantly limits the speed. Instead, we implement a post amplifier with the CML structure. It provides less voltage gain than LA, however, output swing of the post amplifier is large enough to drive a sensitive sense amplifier [17], which can be used for implementing the subsequent circuit block such as a clock and data recovery circuit.

Fig. 2 shows the simplified block diagram of our OEIC receiver. The limiter and the output buffer are included in our implementation so that the receiver performance can be measured with instruments that require a large signal swing level, but these would not be needed if subsequent circuit blocks are integrated together with the OEIC receiver [20]. With this in mind, we do not include the limiter and the output buffer for the power consumption consideration.

3 CMOS optoelectronic receiver

3.1 CMOS-compatible APD

Fig. 3 shows the simplified cross-section of the fabricated CMOS-APD. It is realised with a P^+/N-well junction which slow diffusion currents in P-substrate region can be excluded [21]. The PN junction should be carefully guarded so that the premature edge breakdown is prevented and large, uniform electric fields are achieved. For this, shallow trench isolation (STI) is used in our APD since the STI can provide much higher breakdown field than Si [22, 23]. The active area of CMOS-APD is about 10 μm × 10 μm for optical window. At reverse bias voltage (V_R) of 9.7 V, which results in the best bit-error rate (BER) performance of OEIC receiver, the CMOS-APD has responsivity and avalanche gain of about 60 mA/W and 14.4, respectively. The measured 3 dB photodetection bandwidth of the CMOS-APD is about 5 GHz with 50 Ω load. This bandwidth is mainly limited by the transit time of the photogenerated carriers. Further details for the CMOS-APD can be found in [9].

Table 2 Performance comparison of CMOS OEIC receivers

	[8]	[9]
receiver structure	meshed SML + TIA + LA (nine passive inductors)	APD + TIA + Equaliser (EQ) + LA
CMOS technology	180 nm CMOS	130 nm CMOS
data rate	10 Gb/s	10 Gb/s
total power consumption[a]	118 mW	66.8 mW
TIA	38 mW	13.3 mW
EQ	not used	15.1 mW
LA	80 mW	38.4 mW

[a]Excluding output buffer.

3.2 Inverter-based TIA

Fig. 4 shows the schematic diagram of the inverter-based TIA and additional circuits. The TIA is composed of an inverter and a feedback resistance (R_F) of 3 kΩ. A common-source amplifier is added at the TIA output as a level shifter with additional gain, and the degeneration technique provides bandwidth enhancement. About 1 V supply voltage is provided by an on-chip low-dropout regulator for supply noise immunity. In addition, an error amplifier and a transistor M_{N3} are used to eliminate DC offset because of PD dark currents, amplifier offset and DC component of the received signal [24]. The voltage difference between (+) and (−) nodes of the error amplifier is integrated, and the output voltage of the error amplifier controls the amount of the current flowing through M_{N3}. The estimated DC offset is about 73.5 mV for −4.5 dBm optical input power. For this estimation, APD responsivity of 0.07 A/W and R_F of 3 kΩ are used. With the error amplifier and the feedback loop, this DC offset can be entirely eliminated and the TIA input voltage can be maintained at $V_{DD}/2$. The power consumption for this block is about 1 mW.

Fig. 5 shows the simulated frequency response of the inverter-based TIA, and the result is compared with the CML-based TIA. For this simulation, an APD equivalent circuit model including transit time effect reported in [25] is used. The transimpedance gain is 68 dBΩ and the 3 dB bandwidth is about 2.6 GHz, which is <3.3 GHz for the

Table 1 Comparison of 850 nm CMOS-PDs

	[3]	[8]	[9]	[10]	[11]	[12]
technology	180 nm CMOS	180 nm CMOS	130 nm CMOS	90 nm CMOS	65 nm CMOS	40 nm CMOS
PD type	PIN PD	meshed SML PD	APD	SML PD	PD	meshed SML PD
layer structure	P^+/P-sub/N^+	N-well/P-sub	P^+/N-well	N-well/P-sub	N-well/P-sub	N-well/P-sub
size	50 μm × 50 μm	55 μm × 55 μm	10 μm × 10 μm	72 μm × 78 μm	60 μm × 60 μm	30 μm × 30 μm
responsivity	N/A	29 mA/W	100 mA/W	236 mA/W	160 mA/W	N/A
bandwidth	1.9 GHz	6.9 GHz	3.7 GHz	10 MHz	6 MHz	N/A
dark current	N/A	~a few nanoamperes	~a few nanoamperes	N/A	N/A	N/A
reverse bias voltage, V	6	13	9.7	1.3	0.5	14

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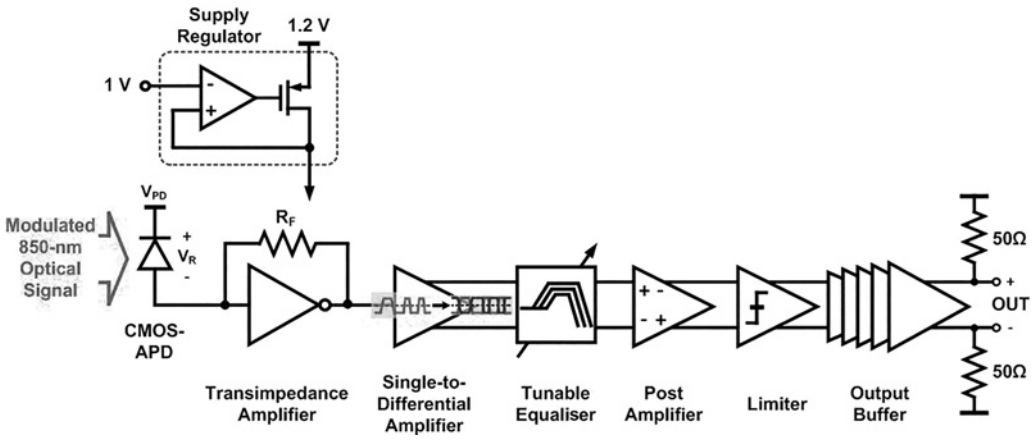

Fig. 2 *Simplified block diagram of the fabricated CMOS OEIC receiver*

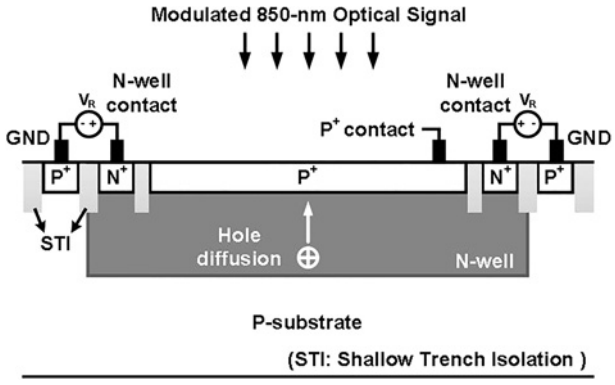

Fig. 3 *Cross-section of the fabricated CMOS-APD*

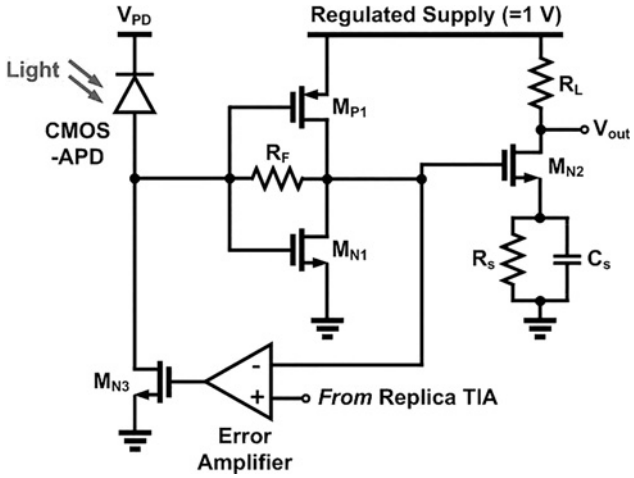

Fig. 4 *Schematic diagrams of inverter-based TIA and additional circuits*

CML-based TIA. As shown in the inset of Fig. 5, low cut-off frequency ($f_{L.-3\,dB}$) of our inverter-based TIA is designed to be about 10 kHz. The DC wander loss because of $f_{L.-3\,dB}$ can be estimated with the following equation [26]

$$\text{DC wander loss} = \frac{V_1}{V_0} \simeq e^{(-mT_b/\tau_1)}$$

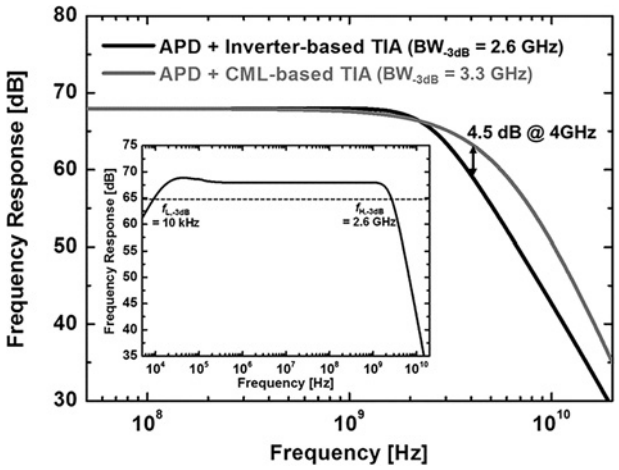

Fig. 5 *Simulated frequency response of CML- and inverter-based TIAs with APD equivalent circuit*

Inset shows the simulated frequency response of inverter-based TIA from 5 kHz to 20 GHz

where V_1 and V_0 represent the output voltage level without and with DC wander effect, respectively. m is the maximum run length, T_b is unit interval and τ_1 is the time constant given as $1/(2\pi f_{L.-3\,dB})$. With $f_{L.-3\,dB}$ of 10 kHz, our receiver is estimated to have DC wander loss of 0.002 dB for 8 Gb/s pseudorandom bit sequence (PRBS) $2^{31}-1$ input data.

Fig. 6*a* shows the simulated 8 Gb/s eye diagram at the output of TIA. As can be seen, the eye diagram is distorted and closed because of the limited bandwidth.

3.3 Tunable equaliser and post amplifier

Fig. 7 shows the schematic diagram of the CTLE for compensating the bandwidth limitation shown in Fig. 6*a*. The CTLE is designed in the differential configuration with capacitive degeneration and negative capacitance [18]. For achieving our target of 8 Gb/s operation, boosting gain of about 8 dB is required, and for this, two CTLEs are cascaded. The value of C_{NC} in negative capacitance can be controlled by a capacitor array from nominally zero to about 44 fF. At the optimal equalisation, the receiver bandwidth can be enhanced up to 4.35 GHz without any

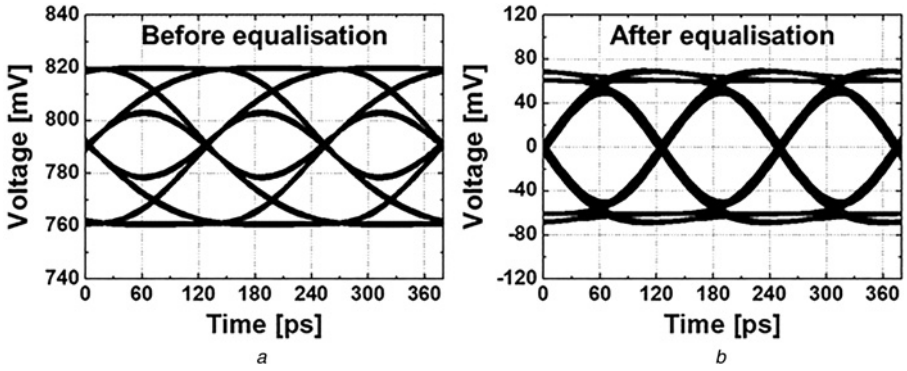

Fig. 6 *Simulated eye diagrams*

a Before equalisation
b After equalisation

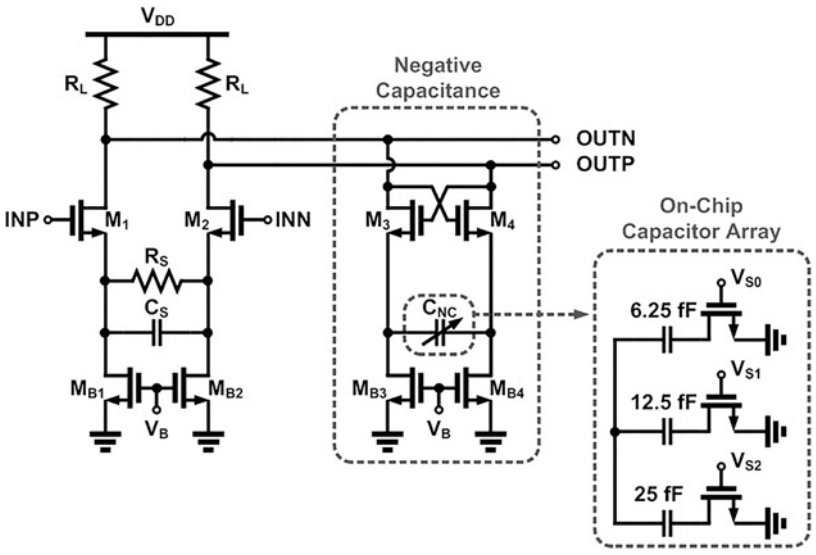

Fig. 7 *Schematic diagrams of CTLE*

peaking in response, and 8 Gb/s clean eye diagram can be achieved at the output of the CTLE as shown in Fig. 6*b*. The CTLE consumes 2.1 mW with 1.2 V supply voltage.

Fig. 8 shows the schematic diagram of the post amplifier. It consists of a two-stage differential amplifier with active feedback [27] and provides about 250 mV_{pp} required by the subsequent block. The post amplifier consumes 1.9 mW with 1.2 V supply voltage.

4 Measurement results

Fig. 9 shows the chip photograph of the fabricated OEIC receiver. The core chip area of the receiver is about 0.58 mm × 0.18 mm. The power consumption excluding limiter and output buffer is about 5 mW with 1.2 V supply voltage. To evaluate our OEIC receiver performance, its BER performance is measured with $2^{31} - 1$ PRBS optical data generated by an 850 nm laser diode modulated by an external electro-optic modulator. All experiments are done with on-wafer probing. The modulated optical signals are transmitted through multimode fibre (MMF) and injected into the OEIC receiver using a lensed fibre. The lensed fibre has the spot size of 10 μm that allows low-loss coupling between MMF and our APD.

Fig. 10 shows the measured photodetection frequency response of our OEIC receiver. Fig. 11 shows the measured BER performance as a function of incident optical power for 8 Gb/s optical data. The measured optical sensitivity for BER of 10^{-12} is −4.5 dBm. The inset in Fig. 11 shows the measured eye diagram. Table 3 compares performances of our optical receiver with previously reported 850 nm CMOS OEIC receivers. The FoM is calculated using the following definition [5] (see equation at the bottom of the page)

Although our receiver did not achieve the highest FoM, the power consumption is by far the lowest because of our inverter-based TIA, resulting in the smallest energy efficiency of 0.63 pJ/bit ever reported.

$$\mathrm{FoM} = \frac{\mathrm{bitrate[Gb/s]} \cdot \left|\log(\mathrm{BER})\right| \cdot \left|\mathrm{sensitivity[dBm]}\right| \cdot \mathrm{gain[dB\Omega]} \cdot \mathrm{PD\ diameter}^2[\mu\mathrm{m}^2]}{\mathrm{power[mW]} \cdot \mathrm{technology}^2[\mathrm{nm}^2]}$$

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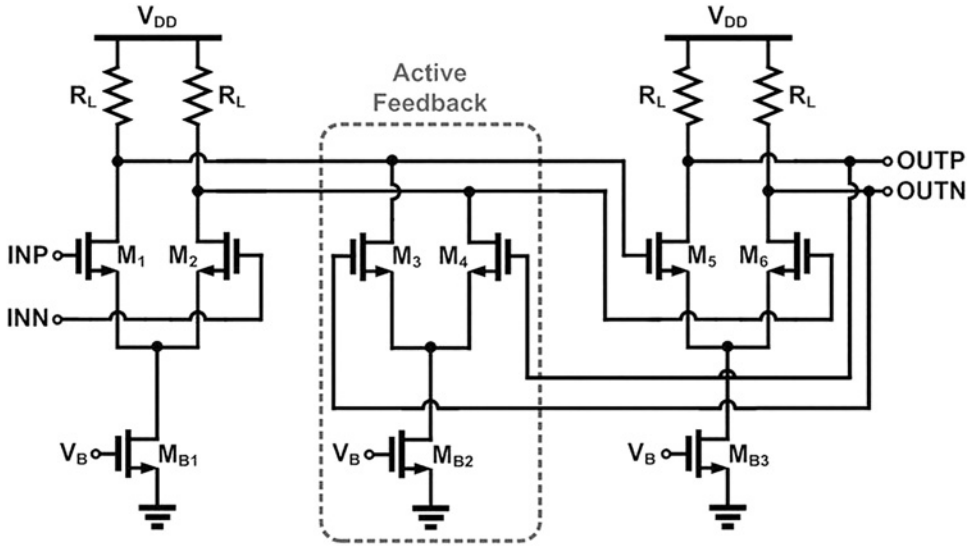

Fig. 8 *Schematic diagrams of post amplifier*

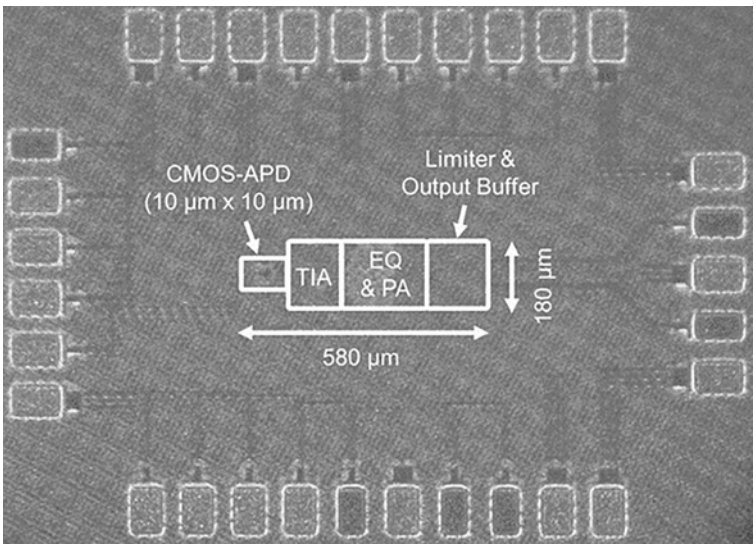

Fig. 9 *Chip photograph*

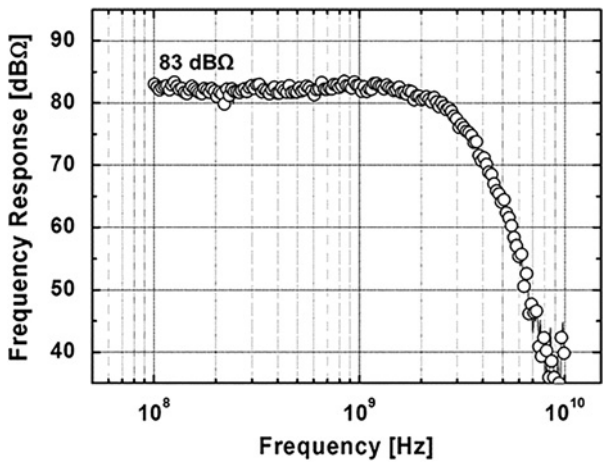

Fig. 10 *Measured photodetection frequency response of our OEIC receiver*

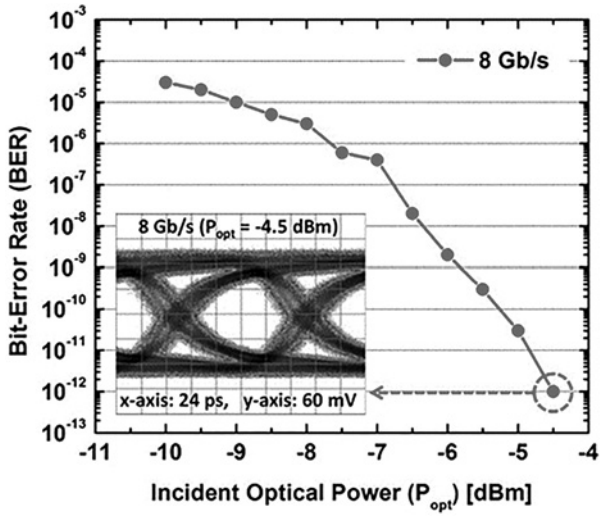

Fig. 11 *Measured BER performance as a function of incident optical power*

Inset shows the measured 8 Gb/s eye diagram

Table 3 Performance comparison of CMOS-PDs

	Bitrate, Gb/s	BER	Sensitivity, dBm	Gain, dBΩ	PD diameter, μm	Power, mW	Technology, nm	FoM	Energy efficiency, pJ/bit
this work	8	10^{-12}	−4.5	83	10	5	65	169.7	0.63
[5]	4.5	10^{-12}	−3.4	105	60	74.16	130	55.4	16.48
[6]	5	10^{-12}	−3	N/A	75	183	180	N/A	36.6
[7]	8.5	10^{-12}	−3.2	120	70	47	130	241.6	5.53
[8]	10	10^{-11}	−6	98	55	118	180	51.2	11.8
[9]	10	10^{-12}	−4	100	10	66.8	130	4.25	6.68
[12]	20	10^{-10}	+2.5	80	30	21	40	N/A	1.05

5 Conclusions

We present a low-power 850 nm OEIC receiver fabricated with standard 65 nm CMOS technology that can operate up to 8 Gb/s with 5 mW. The OEIC receiver achieves low-power operation by using an inverter-based TIA. The bandwidth limitation imposed by the CMOS-APD and TIA is compensated by CTLE. We believe that our OEIC receiver has a great potential for cost-effective and low-power 850 nm optical interconnect applications.

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