A 10-Gb/s Multiphase Clock and Data Recovery Circuit with a Rotational Bang-Bang Phase Detector

Dae-Hyun Kwon, Jinsoo Rhim, and Woo-Young Choi

Abstract—A multiphase clock and data recovery (CDR) circuit having a novel rotational bang-bang phase detector (RBBPD) is demonstrated. The proposed 1/4-rate RBBPD decides the locking point using a single clock phase among sequentially rotating 4 clock phases. With this, our RBBPD has significantly reduced power consumption and chip area. A prototype 10-Gb/s 1/4-rate CDR with RBBPD is successfully realized in 65-nm CMOS technology. The CDR consumes 5.5 mW from 1-V supply and the clock signal recovered from $2^{31}-1$ PRBS input data has 0.011-UI rms jitter.

Index Terms—Bang-bang phase detector, clock and data recovery, multiphase

I. INTRODUCTION

The clock and data recovery (CDR) circuit is one of the most critical building blocks that determine the overall transceiver performance in serial data communication systems. Recently, increasing demands for higher data-rate systems are making CDR design very challenging. Multiphase CDRs having bang-bang phase detectors (BBPD) are widely used for high-speed applications [1, 2] as they can avoid the speed bottleneck by utilizing sub-rate clocks and the binary nature of BBPD allows relatively easier implementation. However, the multiphase structure can consume a large amount of power and requires a large chip area. Previously, the
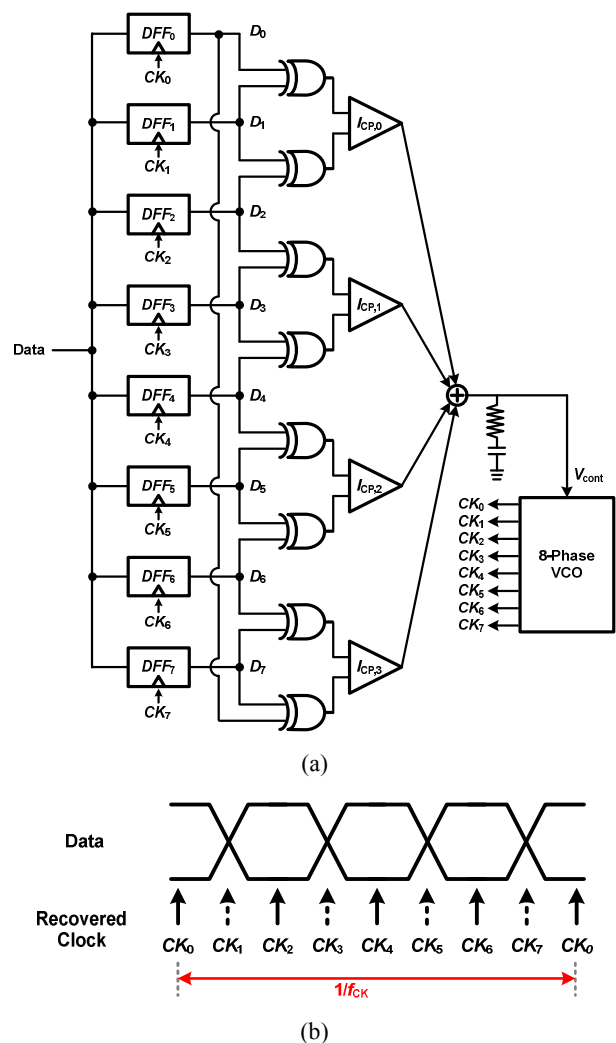
Fig. 1. (a) Conventional 1/4-rate BBPD CDR, (b) conventional BBPD operation.

charge steering latch has been used for the sampler resulting in dramatically reduced power consumption [3], but it requires two capacitors per one latch resulting in
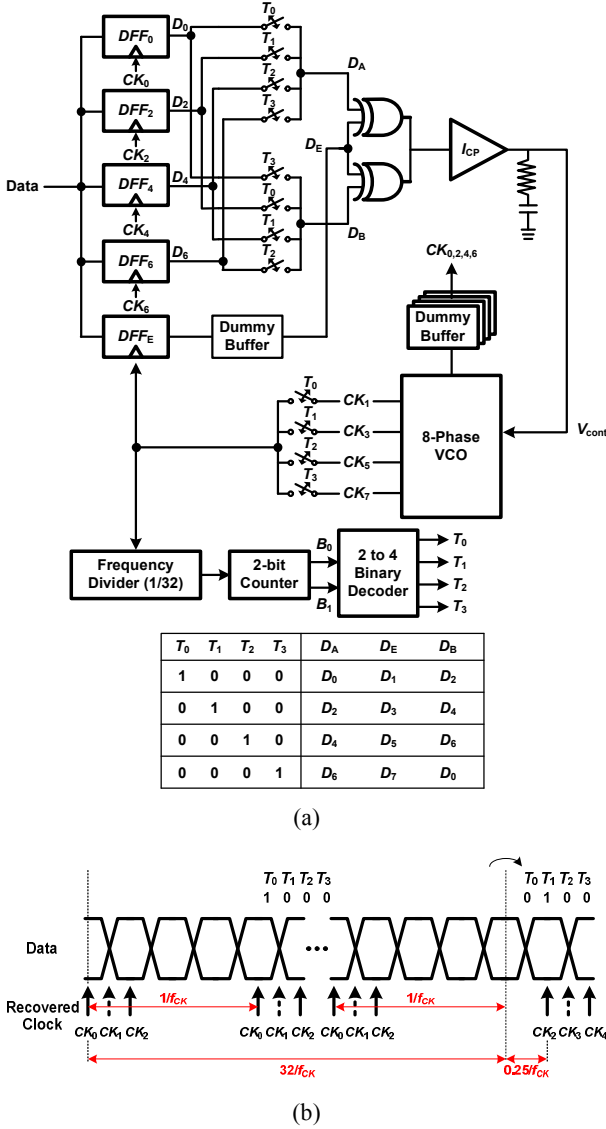
T_0	T_1	T_2	T_3	D_A	D_E	D_B
1	0	0	0	D_0	D_1	D_2
0	1	0	0	D_2	D_3	D_4
0	0	1	0	D_4	D_5	D_6
0	0	0	1	D_6	D_7	D_0

(a)

(b)

Fig. 2. (a) 1/4-rate RBBPD CDR, (b) RBBPD operation.

the relatively large chip area. The single edge-tracking method has been used for power and chip area reduction [4], but this requires 9b/10b encoding and a preamble, which cannot be used for all applications, in order to compensate jitter-tracking bandwidth degradation.

In this paper, we demonstrate a relatively simple technique of power and chip-area reduction for the multiphase CDR. Our technique is based on a novel rotational BBPD (RBBPD) which selects one edge-tracking clock among sequentially rotating 4 edge-tracking clocks.

This paper is organized as follows. In Section II, we explain our multiphase RBBPD CDR structure and its circuit implementation. Section III presents measurement
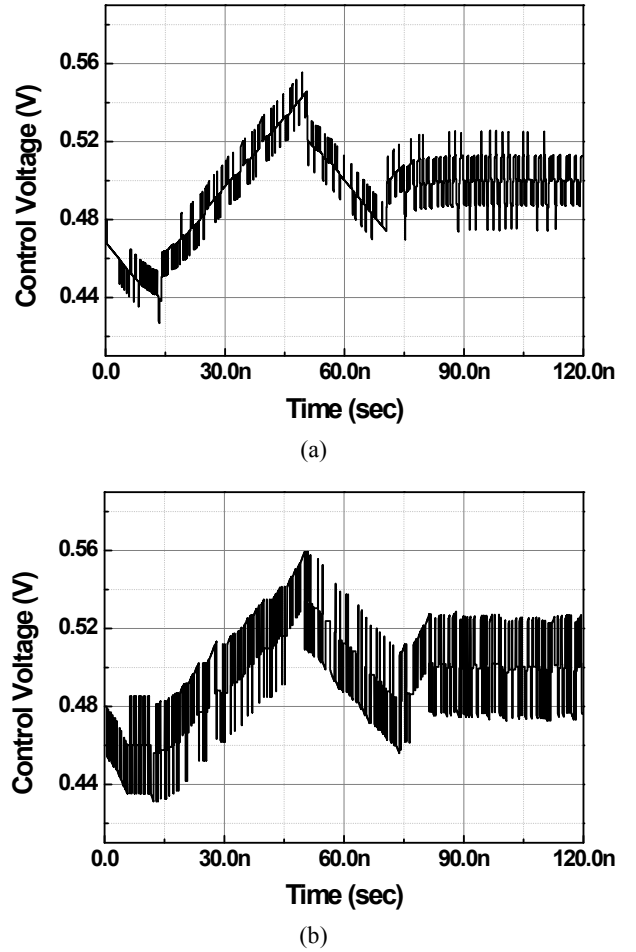

(a)

(b)

Fig. 3. Locking process of (a) BBPD, (b) RBBPD in behavioral simulation.

results of a prototype chip. Section VI gives the conclusion.

II. RBBPD STRUCTURE

Fig. 1(a) shows the structure of a typical 1/4-rate CDR [2] having 4 BBPDs and 4 charge pumps. Among 8 clock signals generated from VCO, 4 ($CK_{0,2,4,6}$) are used for data sampling producing D_0, D_2, D_4, D_6, and the rest ($CK_{1,3,5,7}$) for edge-tracking producing D_1, D_3, D_5, D_7 as shown in Fig. 1(b). Lead and lag signals produced by BBPDs are converted into currents by charge pumps and summed up and averaged in the loop filter.

Our RBBPD has only one BBPD as shown in Fig. 2(a). The edge-tracking signal is provided by DFF_E whose clock signal is selected from $CK_{1,3,5,7}$ with control bit $T_{0,1,2,3}$ and supplied to BBPD. Sampled data signals required for BBPD (D_A and D_B) are selected from
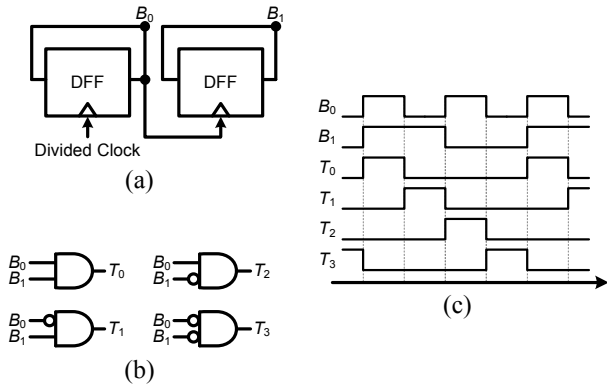
Fig. 4. (a) 2-bit counter, (b) 2-to-4 binary decoder, (c) timing diagram of the decoder.

$DFF_{0,2,4,6}$ output signals with $T_{0,1,2,3}$ so that correct combination of edge-tracking and data-sampling signals is achieved. The table in Fig. 2(a), shows the resulting BBPD input combinations for each $T_{0,1,2,3}$ setting. Since $T_{0,1,2,3}$ setting changes every 32 clock cycles, determined by the frequency divider, the data transition detection density of our RBBPD CDR is 1/4 of the conventional multiphase CDR as schematically shown in Fig. 2(b).

Compared to the conventional multiphase CDR, our RBBPD CDR can save 3 DFFs, 6 XORs, and 3 charge-pumps, and requires additional frequency divider, 2-bit counter and 2-to-4 binary decoder, as can be determined by comparing Fig. 1(a) and 2(a). Since the operating speed for additional blocks is much smaller than that for those saved blocked, our RBBPD CDR achieves reduction of the total power consumption as well as the chip area. Such saving in power and area can be achieved without any detrimental influence on CDR dynamics by rotating edge-tracking clocks and data-sampling signals at a higher frequency than the CDR bandwidth. In addition, our RBBPD CDR has the smaller sampling density since RBBPD samples data edges 4 times less frequently than in the conventional multiphase CDR. The influence of this difference can be easily mitigated by making the charge pump current four times larger.

Fig. 3(a) and (b) show the behavioral simulation results for the CDR control voltages when 10Gbps 2^{31}-1 PRBS data are introduced into the conventional multi-phase CDR and our RBBPD CDR, respectively. For the simulation, our RBBPD CDR has the charge pump current of 500 μA ($4xI_{CP}$), which is four times larger than the conventional CDR charge pump current (I_{CP}). The clock rotating frequency is 78.125 MHz, which is 1/32th
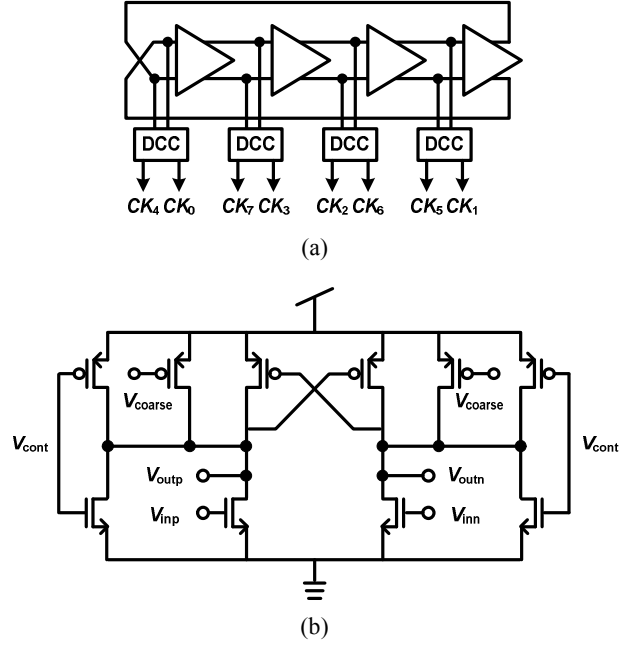

Fig. 5. (a) 8-phase VCO, (b) delay cell.

of the recovered clock frequency. As can be seen in the figures, locking dynamics for two types of CDRs are very similar. However, our RBBPD CDR shows larger dithering jitters because in our RBBPD CDR, the charge pump current dithers among $+4I_{CP}$, 0, and $-4I_{CP}$, whereas in conventional CDR, it dithers among $4I_{CP}$, $+2I_{CP}$, 0, $-2I_{CP}$, and $-4I_{CP}$, resulting in a smaller RMS value for the dithering jitter.

III. Measurement Results

A prototype 1/4-rate 10-Gb/s multiphase CDR with RBBPD is implemented in 65-nm CMOS technology. 4-to-1 multiplexers used for clock signal and sampled data selection are composed of 4 pass gates. Dummy buffers are added for VCO ($CK_{0,2,4,6}$) and DFF_E output signals in order to prevent delay skews as shown in Fig. 2(a). 2-bit counter (Fig. 4(a)) and 2-to-4 binary decoder (Fig. 4(b)) produce 4-bit digital code ($T_{0,1,2,3}$) for selecting the correct edge-tracking clock and sampled data outputs in synchronization with divided-by-32 clock signal. Fig. 4(c) shows the timing diagram for the counter and decoder output signals. Fig. 5 shows the structure of 8-phase VCO [7] with external coarse frequency tuning and duty cycle correctors which compensate duty cycle distortions caused by the pseudo differential delay cell. An off-chip resistor and a capacitor are used for the loop
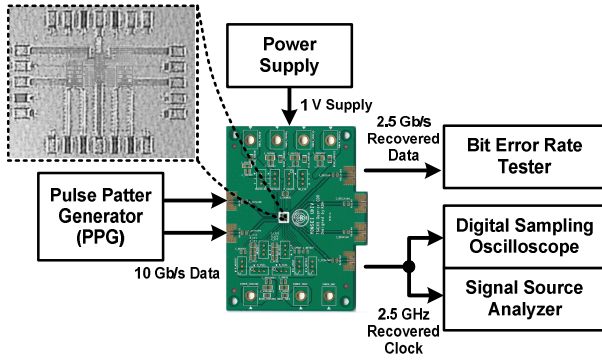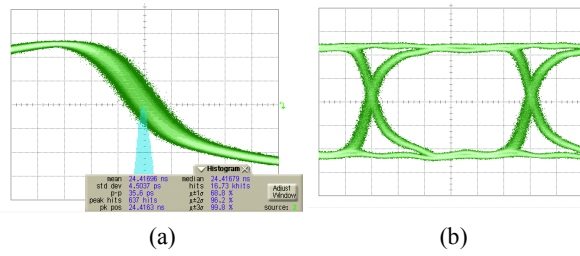
Fig. 6. Chip microphotograph and measurement setup.

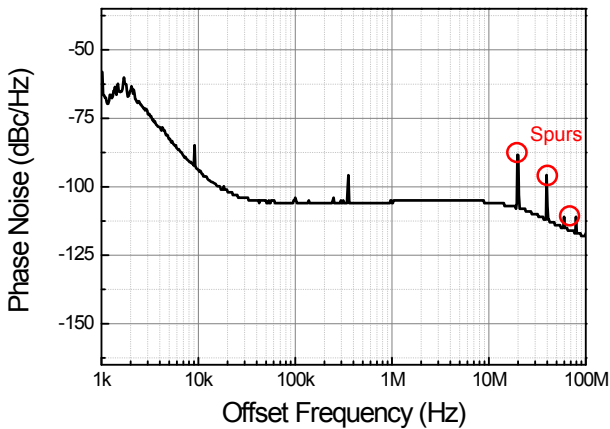**Fig. 7.** Eye diagrams of (a) recovered clock, (b) recovered data.

Fig. 8. Measured phase noise.

Fig. 9. Measured jitter tolerance at 10Gb/s.

Table 1. Performance comparison with multi-rate CDR

	[3]	[4]	[8]	This Work
Process (nm)	65	180	130	65
Supply (V)	1	1.8	1.2	1
Data Rate (f_b) (Gbps)	25	6.93	3.24/5.4	10
f_b/f_{Clk}	2	10	2	4
Power Consumption (mW)	4.97	26.2	138*	5.5
Recovered Clock RMS Jitter (mUI)	19.5	4.2	16.1	11.25
Power Efficiency (mW/Gbit/s)	0.199	3.4	19.3	0.55
Die area (mm^2)	0.039	0.14	1.1**	0.003

* including decoupling capacitors
** including 2:1 MUX and output buffers

filter implementation. Fig. 6 shows the chip microphotograph. CDR except the output buffers consumes 5.5 mW with 1-V supply and occupies 3610 μm^2. The fabricated chip is mounted on FR-4 printed circuit board and wire-bonded for measurement. Fig. 6 shows the measurement setup for evaluating CDR performance. A pulse patter generator (PPG) produces 10-Gb/s PRBS 2^{31}-1 data, and recovered clock and data are measured by a digital sampling scope and a signal source analyzer. The bit error rate tester (BERT) checks if the CDR produces any errors when jitters are injected into input data. Fig. 7 shows measured eye diagrams for recovered clock and data. The recovered clock has rms jitter of 11.25 mUI$_{rms}$.
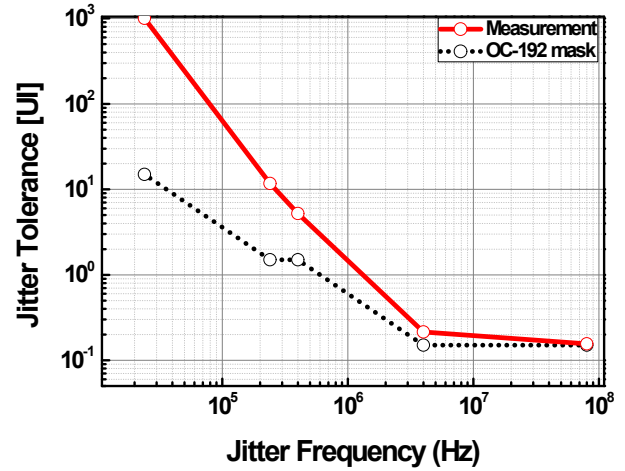
Fig. 8 shows the phase noise of the recovered clock. The spurs observed at 19.5 MHz and its harmonics are due to periodic switching in 4-to-1 multiplexers. Fig. 9 shows the result of jitter tolerance measurement for BER less than 10^{-12} with PRBS 2^{31}-1 input data. Although the amount of data edges our CDR samples in a given time interval is four times less than the conventional multiphase CDR, our CDR does not suffer from jitter tracking bandwidth degradation.

Our CDR has 3 DFFs, 6 XORs, and 3 charge pumps less than the conventional multiphase CDR, but requires additional frequency divider, 2 bit counter, and 2-to-4 binary decoder. When designed in 65-nm CMOS technology, 130 μW and 120 μm^2 are needed for DFF, 75 μW and 86 μm^2 for XOR, 500 μW and 432 μm^2 for charge pump, 70 μW and 190 μm^2 for frequency divider,

75 μW and 370 μm^2 for 2-bit counter and 2-to-4 binary decoder. With these, the conventional multiphase CDR would have power consumption of 6.26 mW and chip area of 4950 μm^2, which correspond to 13.8 % more power and 37.2 % more chip area compared to our RBBPD CDR.

The performance of our RBBPD CDR is compared with previously reported multiphase CDRs based on BBPDs in Table 1. As can be seen in the table, our RBBPD CDR occupies the smallest chip area and achieves relatively small power efficiency. The CDR reported in [3] can achieve the smallest power efficiency as it is based on LC-VCO, which consumes a very small amount of power but occupies a large chip area. Our RBBPD is compatible with any multiphase CDR architecture based on BBPDs.

IV. CONCLUSIONS

A 1/4-rate 10-Gb/s multiphase CDR with a novel RBBPD is demonstrated. Our RBBPD requires only one BBPD and one charge pump and, consequently, it has significantly reduced power consumption and chip area compared to the conventional 1/4-rate multiphase CDR. A prototype chip fabricated in 65-nm CMOS technology successfully demonstrates that our RBBPD operates properly.

ACKNOWLEDGMENTS

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