Effects of Parasitic Resistance on the Performance of Silicon Avalanche Photodetectors in Standard CMOS Technology

Myung-Jae Lee, *Member, IEEE*, and Woo-Young Choi, *Member, IEEE*

***Abstract*— We investigate the effects of parasitic resistance on the performance of silicon avalanche photodetectors (APDs) fabricated in the standard complementary metal–oxide–semiconductor (CMOS) technology. Two types of CMOS-APDs based on the P$^+$/N-well junction having two different parasitic resistances are realized, and their current–voltage characteristics, responsivities, avalanche gains, photodetection frequency responses, and electrical reflection coefficients are measured and compared. In addition, the effect of parasitic resistance on the photodetection bandwidth is analyzed with an equivalent circuit model. It is clearly demonstrated that the parasitic resistance has great effects on the gain and photodetection bandwidth of CMOS-APDs.**

***Index Terms*— Avalanche gain, avalanche photodetector (APD), avalanche photodiode, CMOS integrated circuits, equivalent circuit model, image sensor, inductive peaking, integrated circuit modeling, optical interconnect, parasitic resistance, photodetection bandwidth, photodiode, silicon photonics.**

I. Introduction

DEVELOPMENT and implementation of photonic devices in complementary metal-oxide-semiconductor (CMOS) technology have drawn considerable attention in recent years because they can provide monolithic integration of photonic devices with CMOS circuits for greatly enhanced functionality with a competitive price across a wide spectrum of applications. In particular, CMOS-compatible avalanche photodetectors (CMOS-APDs) are of great interest for several applications ranging from optical interconnects to image sensors [1]–[3]. Since the standard CMOS technology does not provide the optimal fabrication processes for APDs, there have been great research interests in improving and optimizing the performance of the APDs based on available processes in CMOS technology. Structures for PN junctions and guard rings as well as front-end-of-line (FEOL) design issues have been investigated [4]–[7]. However, there have been no reports on the effects of parasitic resistance, which heavily depends on back-end-of-line (BEOL) designs, on the performance of CMOS-APDs.

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M.-J. Lee is with the Faculty of Electrical Engineering, Delft University of Technology, Delft 2628 CD, The Netherlands (e-mail: fodlmj@gmail.com).

W.-Y. Choi is with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea (e-mail: wchoi@yonsei.ac.kr).

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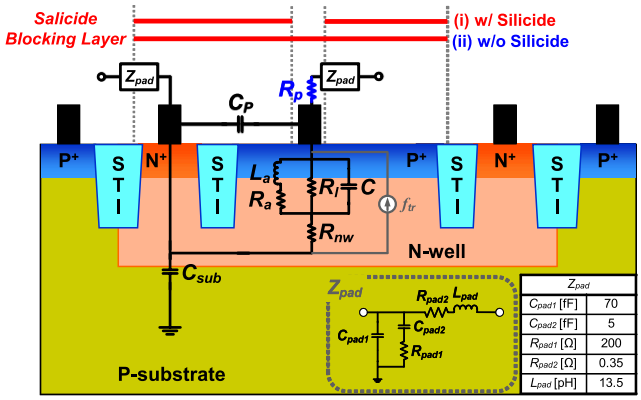

Fig. 1. CMOS-APDs with two types of salicide blocking designs and their equivalent circuit model with parasitic resistance, R_p, at the output P$^+$ port.

In this work, we investigate the effects of parasitic resistance on the performance of CMOS-APDs in terms of avalanche gain and photodetection bandwidth. CMOS-APDs with different values of parasitic resistances are realized by two different types of self-aligned silicide (salicide) processes in BEOL. Their current-voltage characteristics, responsivities, avalanche gains, photodetection frequency responses, and electrical reflection coefficients are measured and, from the measurement results, equivalent circuit models including parasitic resistance are developed for CMOS-APDs. With these, the effects of parasitic resistance on the CMOS-APD performance are identified. It is demonstrated that the CMOS-APD with optimized BEOL design has 43 % enhancement in avalanche gain and 63 % improvement in photodetection bandwidth.

II. Structure and Model of CMOS-APDs

Fig. 1 shows the CMOS-APD structure fabricated in 130-nm standard CMOS technology based on the P$^+$/N-well junction used in our investigation. Shallow trench isolation (STI) is used as a guard-ring structure, which has been demonstrated to provide a uniform electric field profile without premature edge breakdown, resulting in high responsivity [6]. To implement the optical window for CMOS-APDs in CMOS technology, the salicide process should be blocked. In order to investigate the effects of parasitic resistance on the CMOS-APD performance,

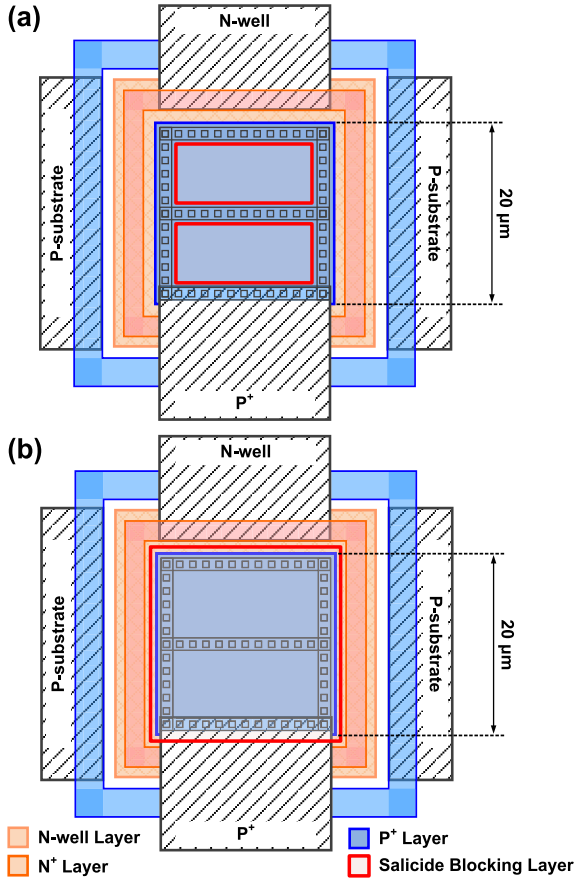

Fig. 2. Simplified CMOS-APD layouts (a) with silicide and (b) without silicide.

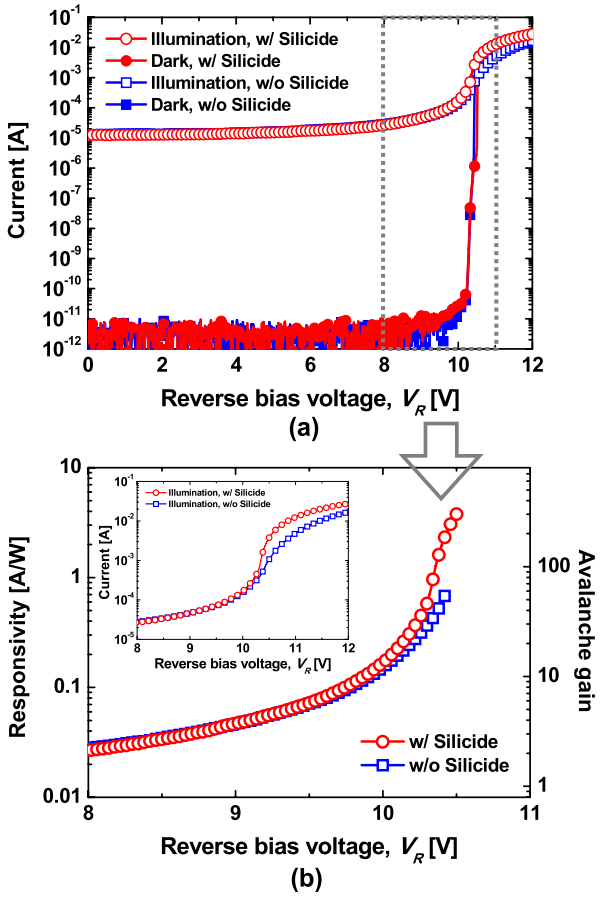

Fig. 3. (a) Current characteristics and (b) responsivity and avalanche gain of CMOS-APDs with and without silicide as a function of the reverse bias voltage. The inset shows magnified current-voltage characteristics.

two different types of CMOS-APDs both having 20×20-μm^2 optical window are realized with two different salicide blocking designs as shown in Fig. 2. In one design, the salicide blocking layer is used for all the optical-window area, resulting in increased parasitic resistance due to removal of the silicide below all contacts. In the other design, the salicide blocking layer is used only for the optical-window area but not for the electrodes so that the silicide below the contacts provides low parasitic resistance. With this design, however, optical loss can increase since there should be sufficient spacing between a contact and a salicide blocking layer in order to satisfy design rules. In this 130-nm standard CMOS technology, the minimum spacing between a contact and a salicide blocking layer is 0.2 μm, and therefore the optical-injection loss caused by this design is almost negligible for CMOS-APDs having five 0.16-μm wide electrode lines on 20-μm diameter optical window. Fig. 1 also shows a simplified equivalent circuit model for the CMOS-APDs based on our previous work [8], including parasitic resistance R_p.

III. Measurement Results and Analyses

For device characterizations, an 850-nm laser diode is used as an optical source. A lensed fiber with 20-μm spot diameter is used for injecting 1-mW light into the CMOS-APDs. Fig. 3 shows measured current-voltage characteristics as well as responsivity and avalanche gain of CMOS-APDs with and without silicide. The CMOS-APD with silicide has lower parasitic resistance than without silicide, and it has larger output currents at a given reverse bias voltage in the avalanche regime due to the smaller voltage drop caused by the parasitic resistance, resulting in higher responsivity and avalanche gain as shown in Fig. 3(b).

Fig. 4 shows the photodetection frequency responses with and without silicide at the reverse bias voltage of 10.25 V, which is the bias condition providing the optimal photodetection frequency response. For these measurements, an electro-optical modulator and a vector network analyzer are used with prior calibration of cables and RF adaptors. As shown in this figure, the CMOS-APD with silicide has higher response due to higher avalanche gain and it has 63% higher photodetection bandwidth. In order to clearly identify the origin of this bandwidth enhancement, equivalent circuit models are used for analyses in a similar manner done in [8]. Fig. 5 shows electrical reflection coefficients of the CMOS-APDs at the same bias condition. The CMOS-APD with silicide has an inductive component (the region above the x-axis), which also can be observed in [9]–[13], but the CMOS-APD without silicide does not show any inductive component.

The parameters of the equivalent circuit model are extracted from two-port S-parameter and photodetection frequency

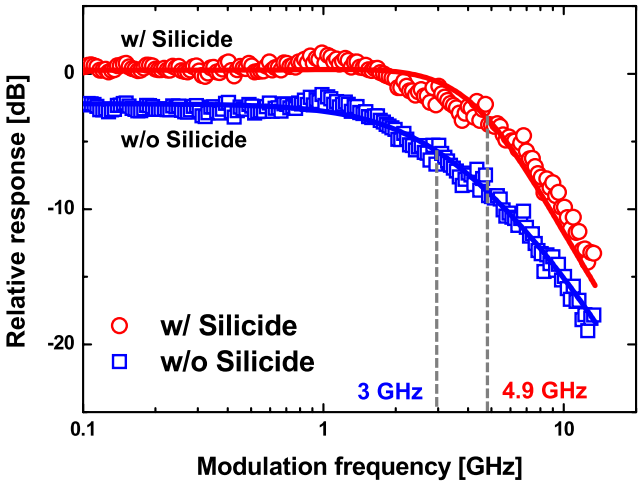

Fig. 4. Measured and simulated photodetection frequency responses of CMOS-APDs with and without silicide. Hollow shapes represent measured data and solid lines simulated results with the equivalent circuit model.

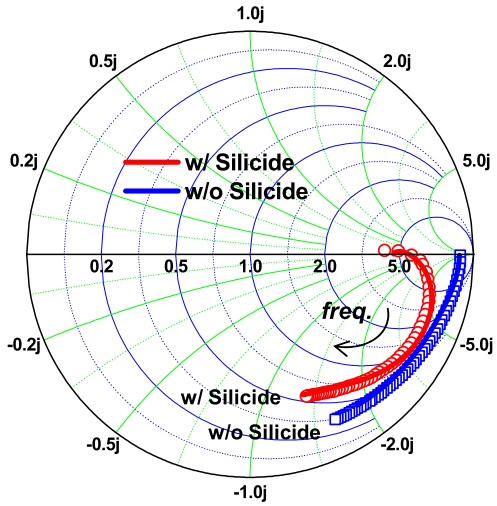

Fig. 5. Measured and simulated electrical reflection coefficients of CMOS-APDs with and without silicide. Hollow shapes represent measured data and solid lines simulated results with the equivalent circuit model.

TABLE I

EXTRACTED PARAMETERS OF THE EQUIVALENT CIRCUIT MODEL FOR CMOS-APDS WITH AND WITHOUT SILICIDE

	w/ Silicide	w/o Silicide
R_p [Ω]	0	30
C_p [fF]	60	
L_a [nH]	13	18
R_a [Ω]	120	2000
R_l [kΩ]	1.2	
C [fF]	140	
R_{nw} [Ω]	70	700
C_{sub} [fF]	45	
f_{tr} [GHz]	3	

response measurements, and the measured and simulated results show good agreement as shown in Fig. 4 and Fig. 5. The extracted parameter values for CMOS-APDs are given in Table I. The CMOS-APD without silicide has higher values

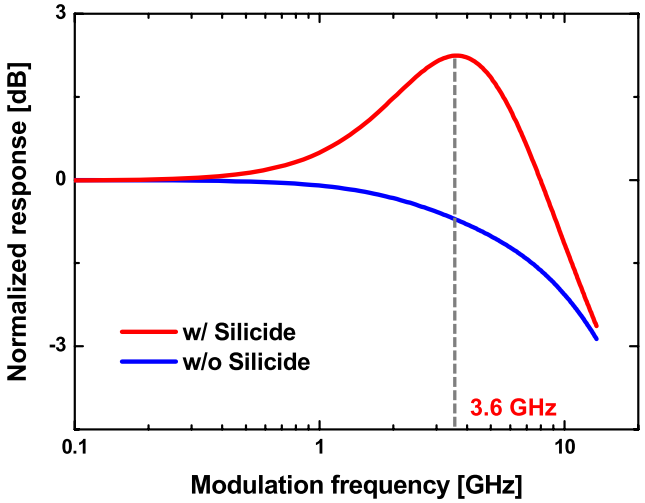

Fig. 6. Normalized photodetection frequency responses of CMOS-APDs without the photogenerated-carrier transit time.

for parasitic resistance, R_p. This provides a smaller effective voltage across the P^+/N-well junction and, consequently, the smaller electric field in the depletion and multiplication regions. This results in larger value for R_{nw} [14]. In addition, the decrease in the electric field reduces the phase delay provided by the avalanche process [14], resulting in increased R_a [15]. L_a also increases because the photocurrent is reduced by the voltage drop and it is inversely proportional to the photocurrent. Other parameters are the same for both CMOS-APDs.

To clarify the inductive-peaking effect for each CMOS-APD, simulation is done for both types of CMOS-APDs with the equivalent circuit having a frequency-independent current source (not including f_{tr} in the current source) or excluding the transit-time effect of photogenerated carriers, which is dominated by hole diffusion in N-well. With this simulation, photodetection frequency responses of CMOS-APDs including only CMOS-APD RLC components can be determined as shown in Fig. 6. It shows that the CMOS-APD without silicide shows no inductive peaking due to the high value of R_a in the avalanche regime caused by the high parasitic resistance, while the CMOS-APD with silicide shows clear inductive peaking at 3.6 GHz, which manifests itself as larger photodetection bandwidth as shown in Fig. 4.

IV. CONCLUSION

The aim of this work is to investigate the influence of parasitic resistance on CMOS-APD characteristics. We demonstrate that CMOS-APDs having smaller parasitic resistance due to the silicide below the contacts have higher avalanche gain and larger photodetection bandwidth. In addition, we analyze the effect of parasitic resistance on the photodetection bandwidth with the equivalent circuit model and provide the qualitative changes in model parameter values that different parasitic resistance values cause. This is the first report on effects of parasitic resistance caused by the BEOL design on the CMOS-APD performance, and the results

of our investigation should provide a very useful design guide for realizing optimal CMOS-APD devices.

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