A Low-Voltage PLL With a Supply-Noise Compensated Feedforward Ring VCO

Sung-Geun Kim, Jinsoo Rhim, *Student Member, IEEE*, Dae-Hyun Kwon, Min-Hyeong Kim, and Woo-Young Choi, *Member, IEEE*

***Abstract*—A low-voltage phase-locked-loop (PLL) circuit with a supply-noise-compensated feedforward ring voltage-controlled oscillator (FRVCO) is demonstrated. The oscillation frequency fluctuation due to supply noise is compensated by adjusting the ratio of driving strength in feedforward and direct paths in FRVCO. A prototype 400-MHz PLL circuit operating at 0.65 V is fabricated with 180-nm standard CMOS process. Measurement results show that supply-noise compensation is successfully achieved. Our PLL consumes only 242.1 μW.**

***Index Terms*—Feedforward ring voltage-controlled oscillator (FRVCO), low supply voltage, phase-locked loop (PLL), voltage-controlled oscillator (VCO) supply noise.**

I. Introduction

REDUCING power consumption and enhancing energy efficiency are key issues in integrated circuit (IC) design. Lowering the supply voltage is the most effective way to achieve these goals, and digital ICs operating at ultra-low voltages or near threshold have been reported [1], [2]. In addition, optimal design of mixed-signal circuits such as phase-locked loops (PLLs) or clock and data recovery circuits operating at low supply voltages are attracting a significant amount of research interests [3]–[7].

PLL design for low-voltage applications has many challenges and achieving supply-noise immunity is very important since supply-voltage fluctuation can more seriously degrade PLL performance at lower supply voltages. In particular, the voltage-controlled oscillator (VCO) is the most sensitive block to supply noise and can be the performance limiting factor for low-voltage PLL. Many circuit techniques that can reduce supply noise have been reported [8]–[10]. However, these are not suitable for low-voltage applications as they need additional transistors causing the voltage headroom problem [8], [9], or require current-mode logic (CML) [10], which is not applicable in low-voltage applications.

In this brief, we present 0.65-V 400-MHz PLL realized in 180-nm CMOS technology whose jitter performance under supply noise is greatly enhanced with a novel technique of supply-noise compensation. Our PLL is based on feedforward ring VCO (FRVCO) whose frequency fluctuation due to supply noise is effectively compensated by adjustment in the driving strength ratio between FRVCO direct and feedforward paths.

This brief is organized as follows. In Section II, the overall PLL architecture and building blocks are described, and details of the noise compensation technique are explained. Section III shows the measurement results, and the conclusion is in Section IV.

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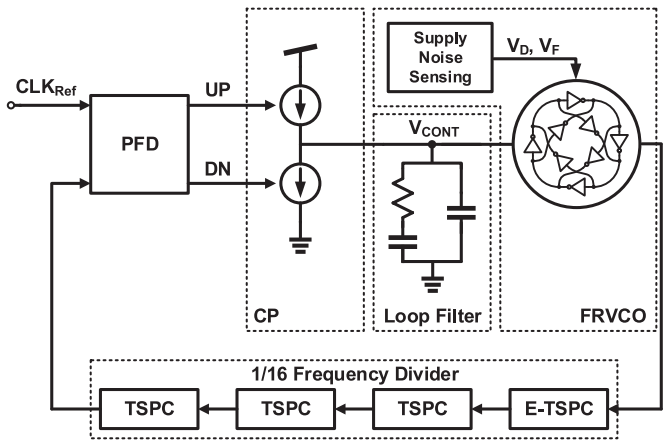

Fig. 1. PLL block diagram.

II. Circuit Implementation

Fig. 1 shows the block diagram of our PLL. For low-voltage operation, no more than three transistors are stacked in the entire circuit. The charge pump has a two-transistor-stacked gate-controlled structure, and the phase-frequency detector consists of conventional CMOS logic gates and D-flip flops (DFFs). The VCO has the feedforward structure with three different frequency tuning nodes. The supply-noise sensing block detects the amount of supply-voltage fluctuation and provides compensation signals to FRVCO. The divide-by-16 frequency divider consists of an extended true-single-phase-clock (TSPC) DFF and three TSPC DFFs for fast operation and low power consumption [11].

A. Four-Stage FRVCO

Fig. 2 shows the structure of the four-stage FRVCO used in our PLL. It has four stages so that it can provide quadrature

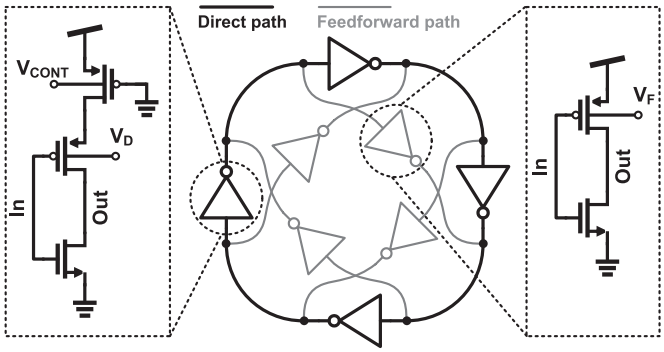

Fig. 2. Four-stage FRVCO.

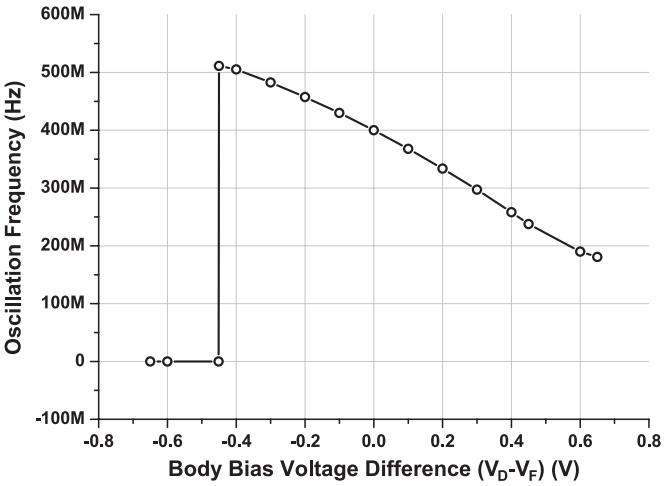

Fig. 3. Simulated FRVCO oscillation frequencies as a function of the body bias voltage difference centered to half of the supply voltage.

clocks required in many applications and consists of four PMOS-controlled current-starved CMOS inverters in the direct path and four basic CMOS inverters in the feedforward path. In current-starved CMOS inverters, the top PMOS body is connected to the loop filter for FRVCO frequency tuning. PMOS body bias control can be used without any latch-up problem due to the low supply voltage. In FRVCO, the driving strength ratio between the direct and the feedforward path is a key parameter for oscillation frequency determination. From the linear analysis of FRVCO reported in [12], it is known that the larger the direct path strength is relative to the feedforward path, the higher the oscillation frequency becomes as long as the oscillation condition is satisfied. In our PLL, the driving strength is controlled by the body bias voltages of PMOS transistors (V_D and V_F) in two different types of inverters as shown in Fig. 2.

Fig. 3 shows FRVCO oscillation frequencies as a function of the body bias voltage difference $(V_D - V_F)$ centered to 0.325 V, half of the supply voltage, simulated with 180-nm CMOS technology. For this simulation, $V_{\rm CONT}$ is fixed at 0.325 V. When the body bias voltage difference is less than -0.45 V, the oscillation condition is not satisfied, and FRVCO fails to oscillate. However, when it is larger than -0.45 V, stable oscillation is achieved, and its frequency goes down as the difference becomes larger.

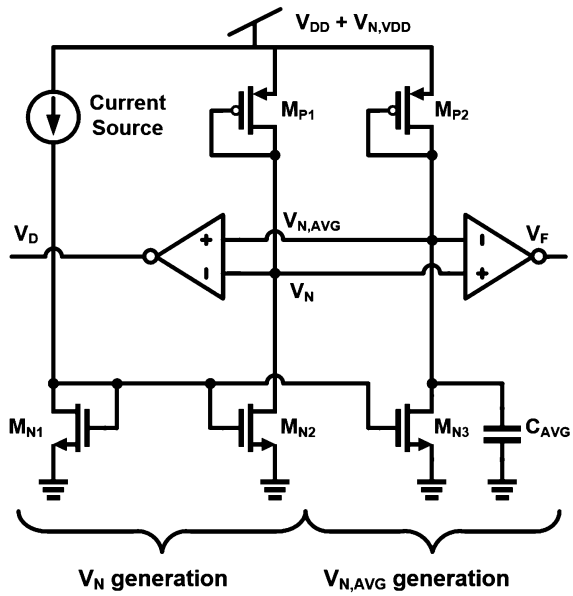

Fig. 4. Schematic of supply-noise sensing block.

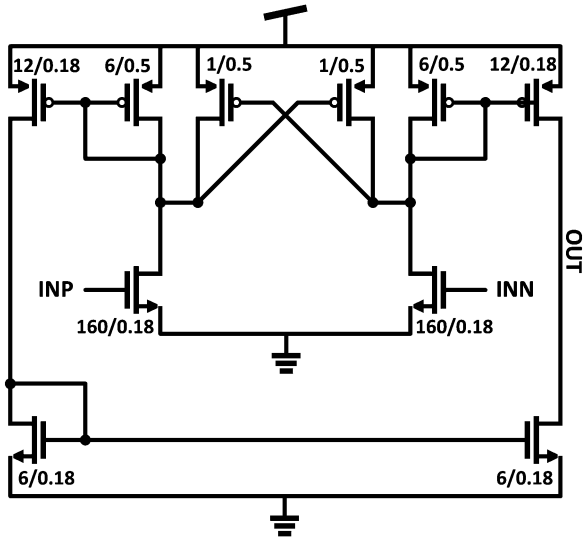

Fig. 5. Schematic of the inverting amplifier in the supply-noise sensing block.

B. Supply-Noise Sensing

Fig. 4 shows the schematic of the supply-noise sensing block. Any fluctuation in the supply voltage $V_{N,\rm VDD}$, produces V_N through voltage division between impedances of diode-connected PMOS M_{P1} and current-mirrored NMOS M_{N2}. $V_{N,\rm AVG}$, which is the time average of V_N, is also generated similarly but with an additional capacitor $C_{\rm AVG}$ in parallel with mirrored NMOS M_{N3}. The small signal ratio between V_N and $V_{N,\rm VDD}$ can be approximated as [13]

$$\frac{V_N}{V_{N,\rm VDD}} \approx 1 - \frac{g_{N2}}{g_{N1}}\frac{g_S}{g_{P1}} \tag{1}$$

where g_{N1}, g_{N2}, g_{P1}, and g_S represent the transconductance of M_{N1}, M_{N2}, and M_{P1}, and the current source, respectively. M_{P2} and M_{N3} are designed so that they are 100 times smaller than M_{P1} and M_{N2}, and the required value for CAVG can

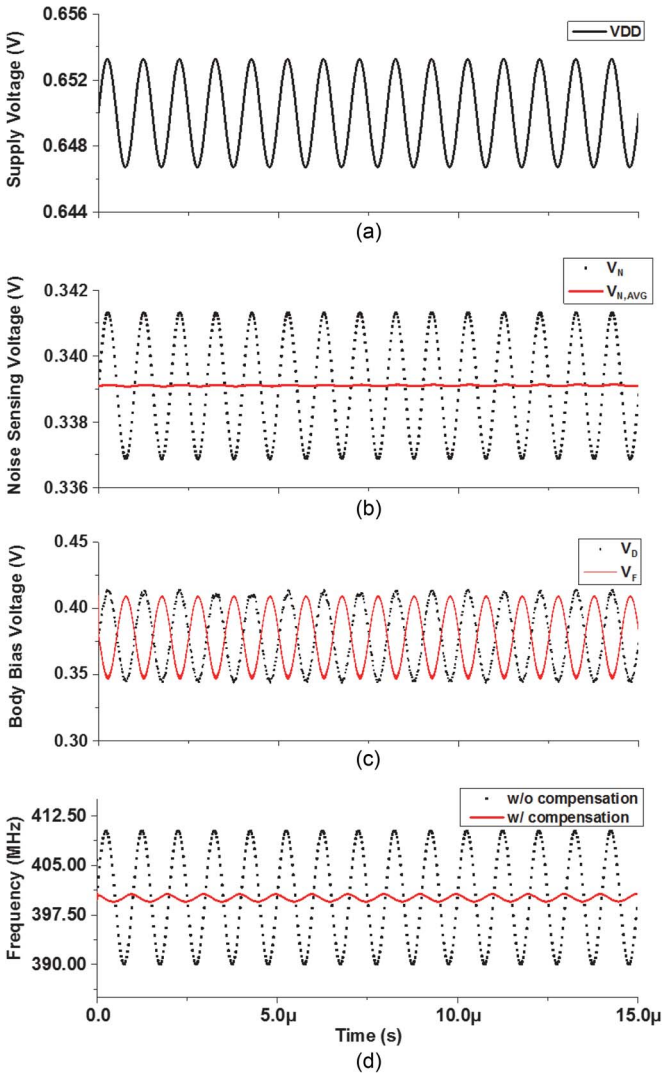

Fig. 6. Simulation results for V_N, (b) $V_{N,\mathrm{AVG}}$, V_D, (c) V_F, and (d) FRVCO oscillation frequency when (a) VDD varies sinusoidally.

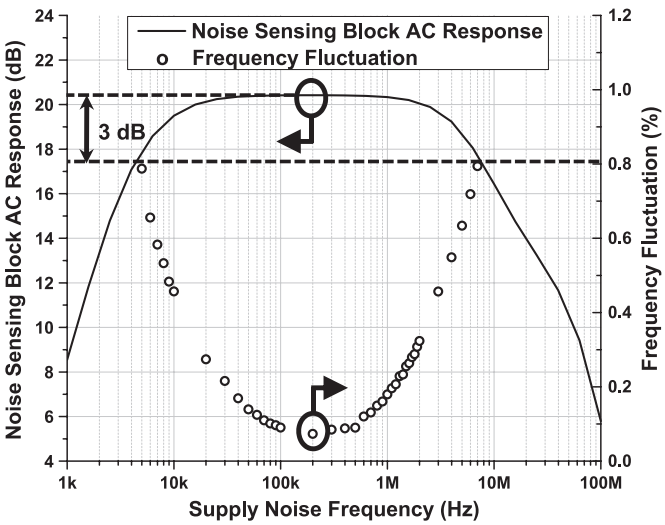

Fig. 7. Simulated ac response of noise sensing block and compensated frequency fluctuation with supply noise.

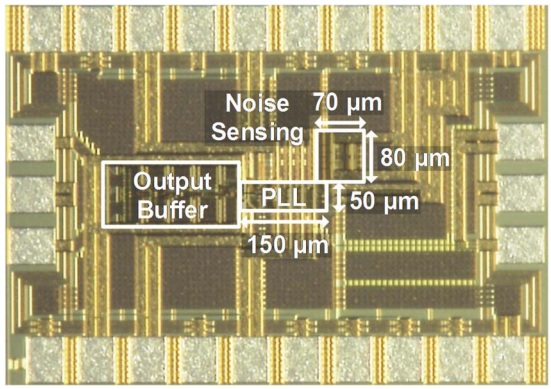

Fig. 8. Microphotograph of fabricated PLL circuit.

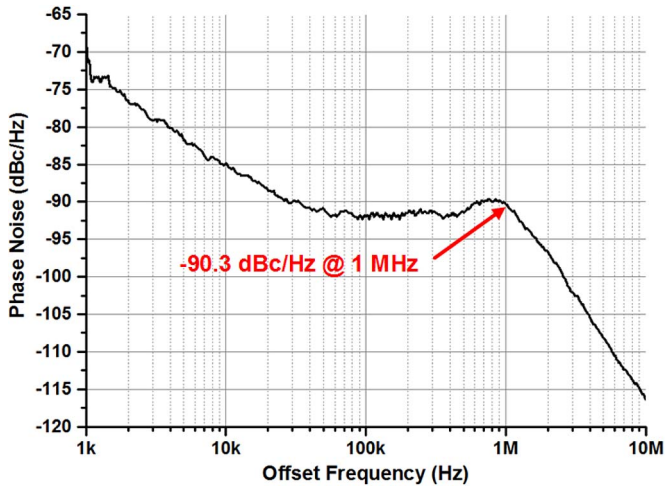

Fig. 9. Measured phase noise of PLL at 400 MHz without supply noise.

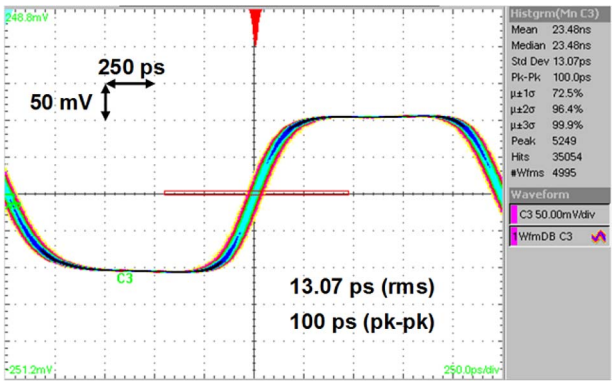

Fig. 10. Measured timing jitter of PLL at 400 MHz without supply noise.

be small (10 pF). Each of $V_N - V_{N,\mathrm{AVG}}$ and $V_{N,\mathrm{AVG}} - V_N$ is amplified by an inverting amplifier generating V_F and V_D, respectively. When $V_N > V_{N,\mathrm{AVG}}$, V_D is larger than V_F, causing reduction of FRVCO oscillation frequency. When $V_N V_{N,\mathrm{AVG}}$, the opposite happens.

Fig. 5 shows the schematic with transistor sizes for two identical inverting amplifiers used in the supply-noise sensing block. The amplifier gain A_V is designed so that the amount of oscillation frequency shift due to the difference in V_D and

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Performance Parameters	[3]	[4]	[5]	[6]	This work
Technology (nm) (Nominal Supply Voltage)	130 (1.2 V)	90 (1 V)	130 (1.2 V)	65 (1 V)	180 (1.8 V)
Supply Voltage (V)	0.5	0.5	0.5	0.4	0.65
Core Area (mm^2)*	0.04	0.12	0.0736	0.0081	0.0075 **
Output Freq. (GHz)	0.55	0.4	0.4	0.35	0.4
Phase Noise @ 1-MHz offset (dBc/Hz)	-95	-87	-91.5	-90	-90.3
RMS Jitter (ps)	8.01 (0.0044 UI)	9.62 (0.0038 UI)	5.5 (0.0022 UI)	30.8 (0.0108 UI)	13.1 (0.0052 UI)
Power (mW)	1.25	0.4	0.44	0.109	0.14 **
Power Efficiency (mW/GHz)	2.272	1	1.1	0.31	0.35 **

* Estimated without loop filter
** Without noise sensing block

V_F corresponds to the amount of frequency fluctuation due to supply noise, or

$$(V_D - V_F) \cdot K_{\mathrm{BIAS}} = V_{N,\mathrm{VDD}} \cdot K_{\mathrm{VDD}} \tag{2}$$

where K_{BIAS} is a proportionality coefficient that can be determined from the dependence of the oscillation frequency on the body bias voltage difference shown in Fig. 3. K_{VDD} is another proportionality coefficient that can be estimated determined by simulation. Since $V_F = -A_V \cdot (V_N - V_{N,\mathrm{AVG}})$ and $V_D = -A_V \cdot (V_{N,\mathrm{AVG}} - V_N)$, A_V can be expressed as

$$A_V = \frac{1}{2} \frac{K_{\mathrm{VDD}}}{K_{\mathrm{BIAS}}} \frac{V_{N,\mathrm{VDD}}}{(V_N - V_{N,\mathrm{AVG}})}. \tag{3}$$

The given equation is used for our design guide for the inverting amplifiers in the noise-sensing block. Since fabricated circuits inevitably suffer from process and temperature variation, requiring tuning of the amplifier gain, our circuits are designed so that the amplifier gain can be tuned by externally controlling the current source bias in the noise sensing block. In addition, its bandwidth is designed to exceed the PLL bandwidth in order not to affect PLL dynamics.

Fig. 6 shows transient simulation results for V_N, $V_{N,\mathrm{AVG}}$, V_D, V_F, and FRVCO oscillation frequency when the supply voltage sinusoidally varies +/−0.5% around 0.65 V at 1 MHz. For these simulations, V_{CONT} is fixed at 0.325 V. Simulation results show that V_N and $V_{N,\mathrm{AVG}}$ are properly sensed, and generated V_D and V_F successfully compensate FRVCO oscillation frequency against supply voltage fluctuation.

The performance of the supply-noise sensing block is limited in the high frequency by the bandwidth of the inverting amplifier and in the low frequency by C_{AVG}. Fig. 7 shows the simulated frequency response of the supply-noise sensing block and the compensated oscillation frequency fluctuation in percentage under sinusoidal supply noise. Here, the compensated oscillation frequency fluctuation is defined as $(f, \max - f, \min)/f$ without supply voltage fluctuation, where $f, \max$ and $f, \min$ are the largest and the smallest oscillation frequency with supply voltage fluctuation. Our noise sensing block is designed to have bandpass characteristics peaked at 200 kHz since the optimal PLL bandwidth based on the noise simulation of PLL building blocks is estimated to be 200 KHz. As shown in Fig. 7, the frequency fluctuation is less than 0.8% when the supply-noise frequency is within 3-dB bandwidth of the supply-noise sensing block frequency response. In PLL, VCO has bandpass filtering characteristics against supply noise. Consequently, as long as the noise sensing bandwidth covers the PLL bandwidth, the supply-noise sensing block should operate properly.

III. MEASUREMENT RESULTS

A prototype PLL circuit is fabricated in 180-nm standard CMOS technology. Fig. 8 shows the microphotograph of the fabricated chip. The core chip area is 0.0075 mm^2, excluding output buffers and the supply-noise sensing block. The fabricated chip is mounted and wire-bonded on FR4 PCB for measurement. The external loop filter is implemented so that our PLL has the best jitter performance. The resulting bandwidth of 0.8 MHz is different from the simulated bandwidth of 200 kHz used for our design. This discrepancy is due to inaccuracies in our noise modeling of PLL blocks.

For our measurement, the amplifier gain is externally tuned once and maintained at the same tuning condition through the measurement. Fig. 9 shows the measured phase noise, and Fig. 10 shows timing jitter of our PLL at 0.65-V supply voltage without any supply noise. The phase noise is −90.3 dBc/Hz at 1-MHz offset and rms and peak-to-peak jitter are 13.07 and 100 ps, respectively. Table I shows the performance summary of our PLL as well as comparison with other low-voltage PLL circuits previously reported. Our PLL has the smallest chip size and lower power consumption/efficient than most of low-power PLLs reported. Although our PLL has slightly higher power consumption/efficiency than PLL reported in [6], it has much better jitter performance. Although two PLLs have similar phase noise at 1-MHz offset, our PLL has much lower phase noise between 5-kHz to 1-MHz offset, achieving better jitter performance.

To verify the supply-noise compensation capability of our PLL, 6.5-mV (1% of supply voltage) peak-to-peak sinusoidal signal ranging from 0.1 to 1.5 MHz is added to the supply voltage through a bias tee. The measured PLL jitters are shown

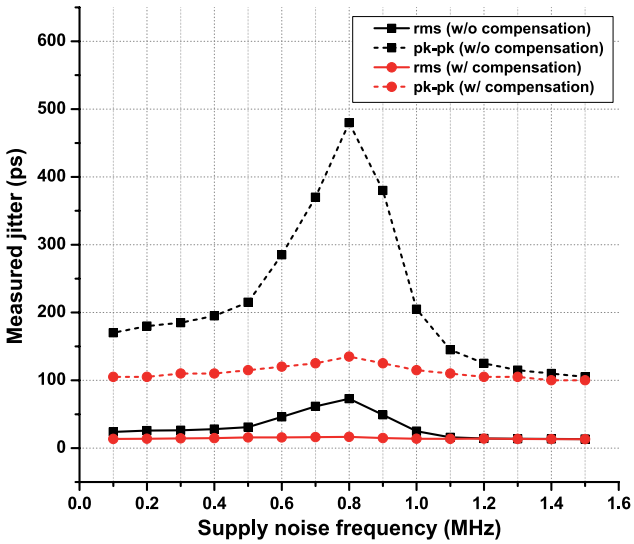

Fig. 11. Measured jitter versus supply noise frequency.

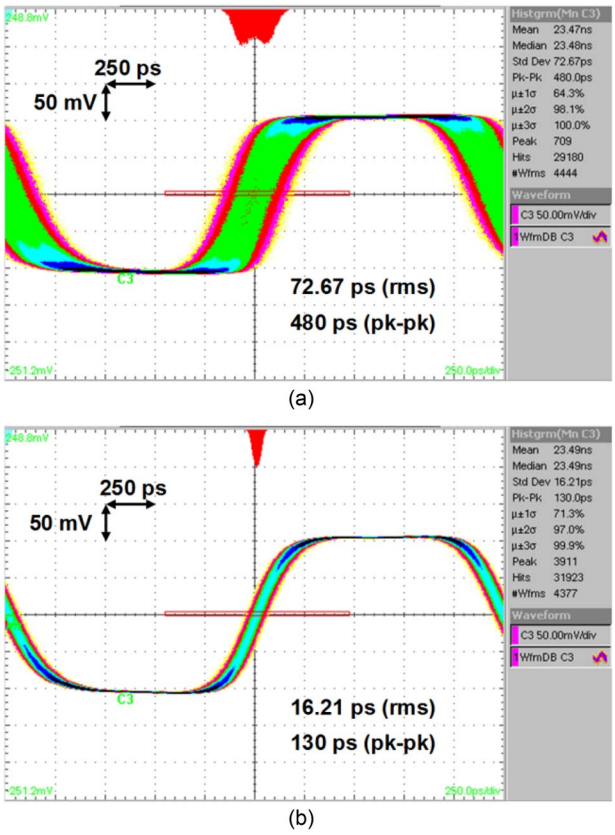

Fig. 12. Measured jitter for PLL with 0.8-MHz sinusoidal noise frequency: (a) without compensation; (b) with compensation.

in Fig. 11. Without any noise compensation, the jitter peaks at 0.8 MHz, which is the loop bandwidth of PLL set by external loop filter, but it is much reduced with compensation. Fig. 12 shows eye diagram of output clock with and without noise compensation under 0.8-MHz supply noise. RMS and peak-to-peak jitter performance is improved from 72.67 (0.029-UI) to 16.21 ps (0.0065-UI) and from 480 to 130 ps, respectively. When there is no supply noise, the operation of the supply-noise sensing block does not influence jitter performance. The supply-noise sensing block occupies 0.0056 mm^2 and consumes 102 μW.

IV. Conclusion

A low-voltage PLL with a novel supply-noise compensation scheme is demonstrated. Oscillation frequency fluctuation due to supply noise is compensated by adjustment in the driving strength ratio between FRVCO direct and feedforward paths. A prototype 400-MHz 0.65-V PLL realized in 180-nm standard CMOS successfully achieves low power consumption and supply noise compensation.

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