A 25-Gb/s Monolithic Optical Receiver With Improved Sensitivity and Energy Efficiency

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***Abstract*— A high-performance integrated optical receiver is realized in photonic BiCMOS technology. The receiver includes waveguide type Ge photodetector (PD), transimpedance amplifier, single-to-differential converter, postamplifier, and output buffer, all of which are monolithically implemented on a Si wafer. It achieves bit-error rate (BER) of 10^{-12} for 25-Gb/s $2^{31}-1$ PRBS at the incident optical power of −10 dBm with energy efficiency of 1.5 pJ/b. In addition, with the help of the accurate Ge-PD circuit model, the simulated optical receiver eye diagrams and BER performances accurately predict the measured results.**

***Index Terms*— Equivalent circuit model, Ge photodetector, optical receiver, Si photonics, transimpedance amplifier.**

I. Introduction

THE bandwidth requirements for chip-to-chip, board-to-board, and system-to-system interconnects are continuously increasing and there are urgent needs for high-speed, small-size, power-efficient, and cost-effective optical interconnect solutions that can satisfy such bandwidth requirements. Optical interconnect solutions based on Si photonics are a promising solution as they can fully utilize such advantages as cost-effectiveness and easier integration with electronics, which the mature Si fabrication technology readily provides. In particular, monolithic integration of photonic devices with electronic circuits on Si platform can be very powerful solution. There have been several reports for optical transmitters, receivers, and other circuits realized with photonic-electronic integration [1]–[5].

Monolithically integrated optical receivers have been realized based on IHP's photonic BiCMOS technology for 25-Gb/s operation with −15-dBm sensitivity for 10^{-3} bit-error rate (BER) and energy efficiency of 2.3 pJ/bit [1] and 40 Gb/s with −3-dBm sensitivity for 2.5×10^{-11} BER and energy efficiency of 6.9 pJ/bit [3]. Although these results are impressive, for several optical interconnect applications, better receiver sensitivity and energy efficiency are needed. In order to achieve this, we establish a more accurate Ge-PD circuit model and used it for design optimization of the optical receiver. With the accurate Ge-PD circuit model, amplifiers in the optical receiver can be designed with optimally necessary gain and bandwidth resulting in better noise and energy performances. Furthermore, we demonstrate that measured optical receiver performance agree very well with simulation results, which we believe is the required step for realizing high-performance and cost-effective photonic-electronic integrated circuits including Ge PDs with high degree of integration.

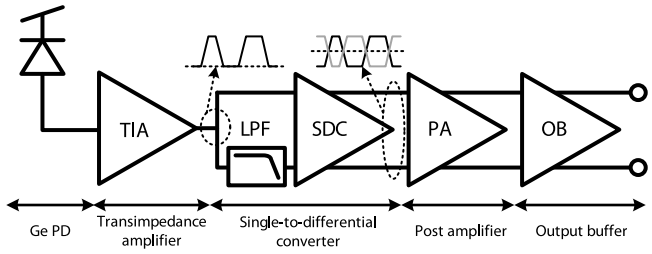

Fig. 1. Block diagram of the realized monolithic optical receiver.

II. Monolithic Optical Receiver

Fig. 1 shows the block diagram of our 25-Gb/s integrated optical receiver. It includes on a single platform the first generation Ge PD developed at IHP [6], [7], a transimpedance amplifier (TIA), a single-to-differential converter (SDC), a post amplifier (PA) and an output buffer (OB) based on IHP's 0.25-μm SiGe BiCMOS technology which provides photonic device integration and electronic circuit having f_T and f_{max} of 190 GHz [6]. By establishing the accurate Ge-PD circuit model ahead of receiver circuit design, optimized sensitivity and energy efficiency can be achieved.

A. Ge-Photodetector Equivalent Circuit Model

Fig. 2(a) shows the cross-section of the waveguide Ge PD integrated in our optical receiver. It is based on a lateral PIN structure having 3-μm width and 20-μm length. Fig. 2(b) shows the measured dark current and photo current with −3-dBm incident optical power. The responsivity of Ge PD is 0.6 A/W and the photodetection 3-dB bandwidth with 50-Ω load is 25 GHz. Fig. 3(a) shows its equivalent circuit model containing two current sources, which provides better agreement with measurement results [8]. Fig. 3(b) graphically shows the frequency response of I_{drift} and I_{diff}, which respectively represent photo-generated carriers undergoing drift and diffusion with corresponding 3-dB frequency

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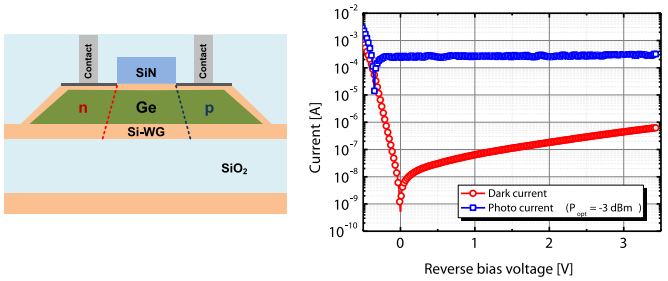


Fig. 2. (a) Structure and (b) measured current characteristics of the integrated Ge PD.

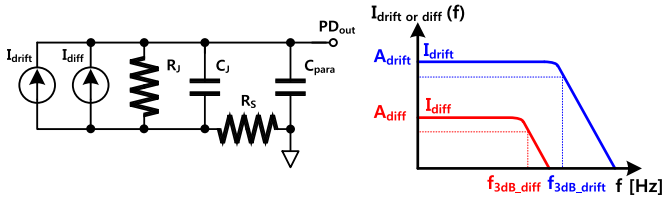


Fig. 3. (a) Equivalent circuit model of the Ge PD and (b) frequency response of photogenerated current.

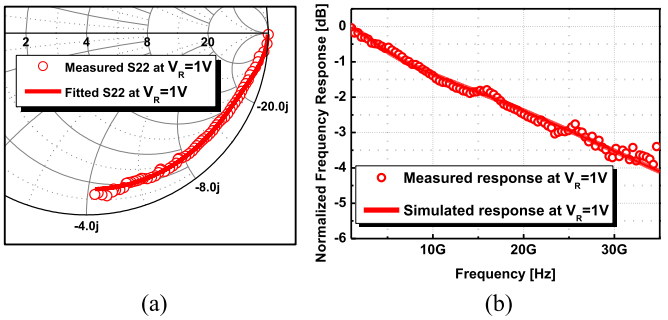


Fig. 4. Measured and simulated (a) S22 and (b) photo-detection frequency response.

TABLE I

EXTRACTED NUMERICAL VALUES FOR Ge-PD CIRCUIT MODEL

Passive elements	C_J	7 fF	I_{drift} & I_{diff}	f_{3dB_drift}	34 GHz
	R_S	90 Ω		A_{drift}	85.6 %
	R_J	100 kΩ		f_{3dB_diff}	4.7 GHz
	C_{para}	2.3 fF		A_{diff}	14.4 %

f_{3dB_drift} and f_{3dB_diff}. A_{drift} and A_{diff} respectively represent the percentage of photogenerated carriers that undergo drift and diffusion. The model also contains passive elements representing junction capacitance (C_J), junction resistance (R_J), series resistance (R_S) and parasitic capacitance (C_{para}). Details for extracting numerical values for all these parameters can be found in [8]. The extracted numerical values at reverse bias voltage (V_R) of 1 V are given in Table I. Fig. 4(a) and (b) show the measured electrical reflection coefficients and photodetection frequency responses, respectively as well as simulated results with our Ge-PD circuit model.

B. Optical Receiver Circuit

Fig. 5 shows schematic diagrams for TIA, SDC and PA. For our TIA, the regulated cascode configuration is used to achieve a large gain-bandwidth product. Furthermore, with accurate circuit model of Ge-PD, TIA can achieve maximum gain with the required bandwidth for SNR optimization. In order to eliminate DC offset in the TIA output, SDC containing an on-chip low-pass filter and the DC delivering circuit is used. The low cut-off frequency is set to 2 MHz to avoid any DC-wander problem. PA amplifies SDC output signals for achieving 200 mV peak-to-peak with −10-dBm input power. The PA is composed of active feedback and emitter followers. An output buffer is used for driving 50-Ω load for measurement.

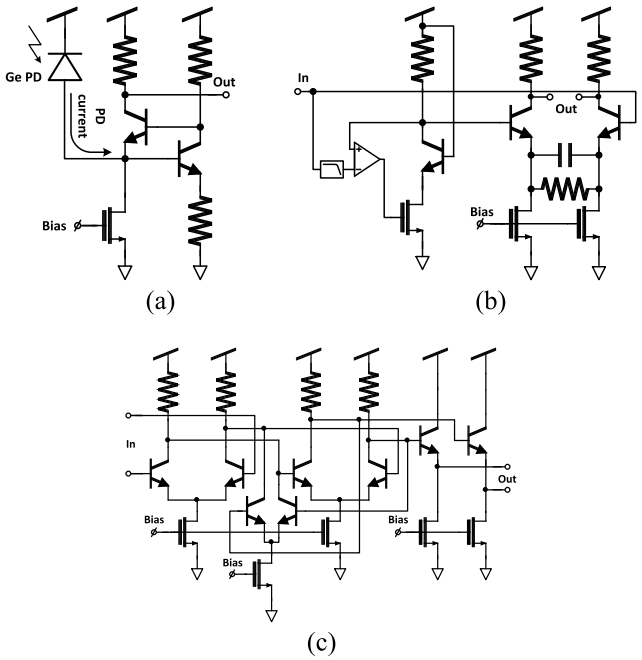


Fig. 5. Schematic diagrams of the (a) TIA, (b) SDC and (c) PA.

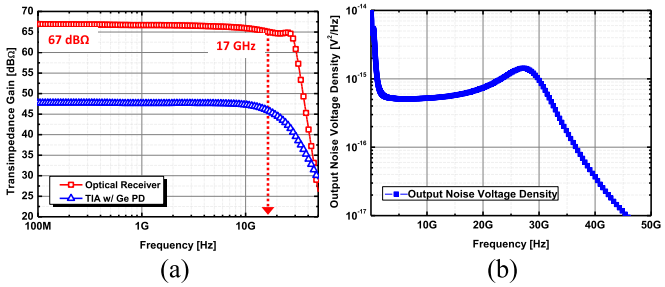
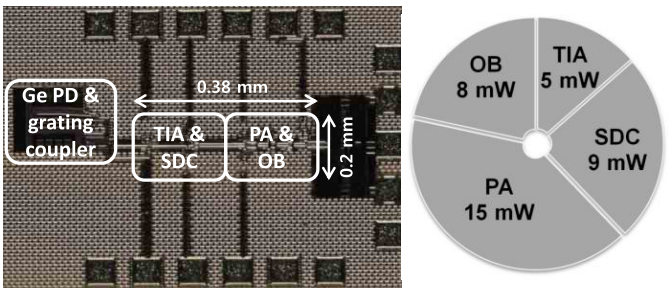


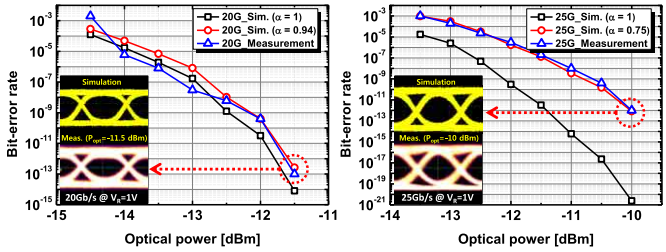
Fig. 6. Simulated (a) photo-detection frequency response and (b) output noise voltage density of the designed optical receiver with the Ge-PD circuit model.

Fig. 6(a) shows the simulated frequency responses for TIA with Ge-PD circuit model and the entire optical receiver. As shown in the figure, TIA provides transimpedance gain of 48 dBΩ and 3-dB bandwidth of 20 GHz including the Ge-PD circuit model. The entire optical receiver has transimpedance gain of 67 dBΩ and 3-dB bandwidth of 17 GHz resulting in SDC and PA after TIA. Fig. 6(b) shows the simulated output noise voltage density of the optical receiver circuit. The integrated output noise voltage from 10 MHz to 50 GHz is 29.3 μV_{rms}^2, which corresponds to input referred noise current of 4.91 μA_{rms}.



(a) (b)

Fig. 7. (a) Microphotograph and (b) power consumption breakdown of the fabricated monolithic optical receiver.



(a) (b)

Fig. 8. Simulated and measured BER performances with and without α for (a) 20- and (b) 25-Gb/s data. Insets are the eye diagrams at selected BER points

III. Measurement Results

Fig. 7 shows the microphotograph of the fabricated optical receiver. Its core size is 0.38×0.2 mm^2, and it consumes 37 mW with 2.5-V supply voltage including the output buffer. Dotted data in Fig. 8(a) and (b) shows the measured BER at V_R of 1 V and the solid lines are fitted with the BER estimation given as [9]

$$\text{BER} = \frac{1}{2} erfc\left(\frac{\alpha \cdot \text{SNR}}{2\sqrt{2}}\right), \tag{1}$$

where SNR is the signal-to-noise ratio and α represents penalties due to non-idealities caused by the transmitter and electrical cables used in the measurement and bandwidth penalty [10]. α is estimated as 0.94 for 20 Gb/s and 0.75 for 25 Gb/s by fitting Eq. (1) to the measured data. The estimated value for alpha is smaller for 25 Gb/s than 20 Gb/s due to higher bandwidth penalty at 25 Gb/s.

For the noise value, only the circuit noise determined from circuit simulation is considered since the Ge-PD noise is much smaller. For 20-Gb/s operation, BER of 10^{-13} is achieved for $2^{31} - 1$ PRBS input with incident power of -11.5 dBm and, for 25-Gb/s operation, BER of 10^{-12} is achieved with incident optical power of -10 dBm. Insets of Fig. 8 show 20- and 25-Gb/s simulated and measured eye diagrams at selected BER values. The simulations are done with simulated input-referred noise and Ge-PD circuit model [11]. As shown in the figure, simulated and measured results for BER performances and eye diagrams are well matched.

Table II shows the performance comparison of our optical receiver with previously reported 25-Gb/s monolithically integrated optical receivers containing waveguide Ge PD. As shown in the table, our optical receiver achieves higher sensitivity and better energy efficiency. Furthermore small foot print of 0.38×0.2 mm^2 can be achieved without using on-chip inductors.

TABLE II

Performance Comparison of the Reported 25-Gb/s Optical Receivers Monolithically Integrated With Ge PD

	[1]	[2]	[4]	This work
Technology	Photonic BiCMOS	130 nm SOI CMOS	90 nm CMOS	Photonic BiCMOS
Gain (dBΩ)	71	67	-	67
Data rate (Gb/s)	25	25	25	25
BER	10^{-9}	10^{-12}	10^{-12}	10^{-12}
Sensitivity (dBm)	-4.5	-6	-6	-10
Output swing (mV)	200	200	-	200
Power (mW)	57	48	-	37
Efficiency (pJ/bit)	2.28	1.92	-	1.5

IV. Conclusion

A 25-Gb/s monolithic optical receiver containing a Ge PD is realized with IHP's photonic BiCMOS technology. With an accurate Ge-PD equivalent circuit model and careful design, our optical receiver achieves much improved performances with sensitivity of -10 dBm for 25-Gb/s $2^{31} - 1$ PRBS data detection and energy efficiency of 1.5 pJ/bit. In addition, we demonstrate that simulated BER performances and eye diagrams well match the measurement results.

References

[1] D. Knoll *et al.*, "Monolithically integrated 25 Gbit/sec receiver for 1.55 μm in photonic BiCMOS technology," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, Mar. 2014, pp. 1–3.

[2] J. F. Buckwalter, X. Zheng, G. Li, K. Raj, and A. V. Krishnamoorthy, "A monolithic 25-Gb/s transceiver with photonic ring modulators and Ge detectors in a 130-nm CMOS SOI process," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1309–1322, Jun. 2012.

[3] A. Awny *et al.*, "A 40 Gb/s monolithically integrated linear photonic receiver in a 0.25 μm BiCMOS SiGe: C technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 7, pp. 469–471, Jul. 2015.

[4] S. Assefa *et al.*, "Monolithically integrated silicon nanophotonics receiver in 90 nm CMOS technology node," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, Mar. 2013, pp. 1–3.

[5] G.-D. Kim *et al.*, "Silicon photonic temperature sensor employing a ring resonator manufactured using a standard CMOS process," *Opt. Exp.*, vol. 18, no. 21, pp. 22215–22221, 2010.

[6] L. Zimmermann *et al.*, "BiCMOS silicon photonics platform," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, 2015, paper Th4E.5.

[7] S. Lischke, D. Knoll, and L. Zimmermann, "Monolithic integration of high bandwidth waveguide coupled Ge photodiode in a photonic BiCMOS process," *Proc. SPIE*, vol. 9390, pp. 93900F-1–93900F-5, Mar. 2015.

[8] J.-M. Lee, S.-H. Cho, and W.-Y. Choi, "An equivalent circuit model for a Ge waveguide photodetector on Si," *IEEE Photon. Technol. Lett.*, vol. 28, no. 21, pp. 2435–2438, Nov. 1, 2016.

[9] P. Müller and Y. Leblebici, *CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications*. New York, NY, USA: Springer, 2007.

[10] X. Chen, J. Hurley, and M.-J. Li, "Bandwidth measurement of multimode fibers using system level bit error rate testing," *Opt. Exp.*, vol. 19, no. 11, pp. 10613–10618, 2011.

[11] J.-S. Youn, M.-J. Lee, K.-Y. Park, H. Rücker, and W.-Y. Choi, "SNR characteristics of 850-nm OEIC receiver with a silicon avalanche photodetector," *Opt. Express.*, vol. 22, no. 1, pp. 900–907, Jan. 2014.