A 32-Gb/s PAM-4 Quarter-Rate Clock and Data Recovery Circuit With an Input Slew-Rate Tolerant Selective Transition Detector

Dae-Hyun Kwon, Minkyu Kim, Sung-Geun Kim, and Woo-Young Choi

***Abstract*—We present a 32-Gb/s PAM-4 quarter-rate clock and data recovery (CDR) circuit having a newly proposed selective transition detector (STD). The STD allows phase detection of PAM-4 data in a simple manner by eliminating middle transition and majority voting with simple logic gates. In addition, using the edge-rotating technique with quarter-rate CDR operation, our CDR achieves power consumption and chip area reduction. A prototype 32-Gb/s quarter-rate PAM-4 CDR circuit is realized with 28-nm CMOS technology. The CDR circuit consumes 32 mW with 1.2-V supply and the recovered clock signal has 0.0136-UI rms jitter.**

***Index Terms*—Bang-bang phase detector, clock and data recovery (CDR), high speed serial link, multiphase, PAM-4 receiver.**

I. Introduction

With the required amount of data transmission for many applications continuously increasing, the use of multiple data levels has become an efficient solution for increasing transmission throughput without increasing the clock frequency. In particular, PAM-4 signaling is now widely considered for many electrical and optical wireline applications due to its enhanced spectral efficiency [1], [2].

However, with PAM-4 signaling, the clock and data recovery (CDR) circuit becomes complicated since the phase detector should be able to determine correct phase information from various transitions among multiple data levels [3], [4].

For the bang-bang phase detector (BBPD) operation on PAM-4 data, received data are first sampled with clock signals (CK_{D0}, CK_{D1} for data sampling and CK_E for edge sampling) and compared with three different reference voltages (V_H, V_M, V_L). The comparator outputs are then processed with three different pairs of XOR gates for producing UP_H/DN_H, UP_M/DN_M, and UP_L/DN_L signals for up/down information for each level as shown in Fig. 1(a). They subsequently go through additional processing for the middle transition (00 ⇔ 10 or 01 ⇔ 11) elimination and majority voting before final UP and DN signals are produced, as shown in Fig. 1(b). The middle transition causes non-uniform jitter distribution [3] as graphically shown in Fig. 1(c). In particular, the amount of non-uniform jitter depends on the input data slew-rate. PAM-4 transmitters often employ the pre-emphasis technique with the control of the current ratio [1], [5] or output impedance [6], for enhancing transmission bandwidth and/or distance, resulting in slew-rate changes. With such PAM-4 transmitters, optimal design of CDR would be very difficult.

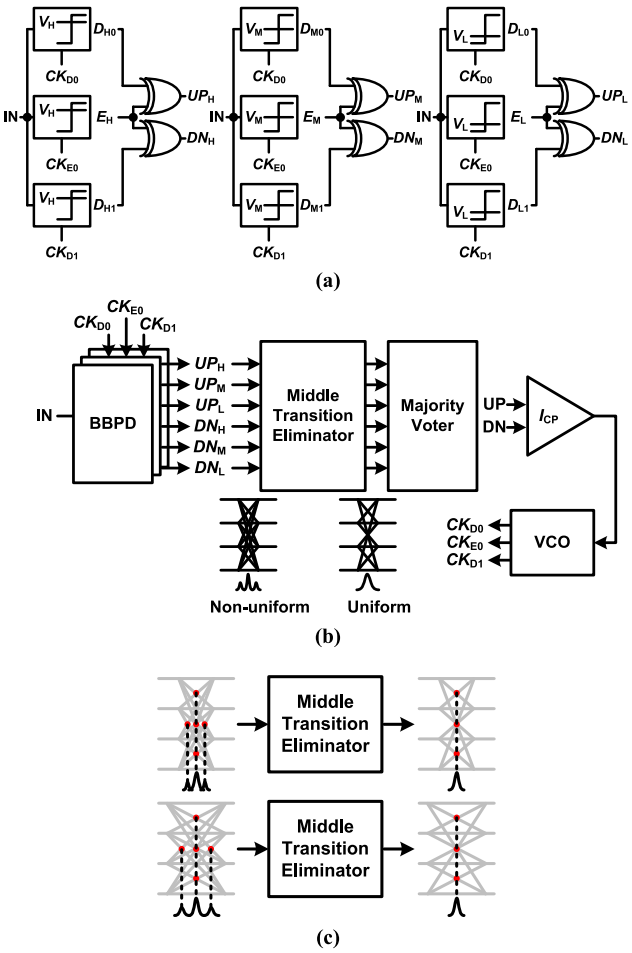

Fig. 1. (a) Conventional BBPD for PAM-4 input signals (b) CDR block diagram having middle transition eliminator and majority voter for multiple UP/DN signals (c) non-uniform jitter distribution according to input slew-rate.

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For middle transition elimination, logic gates are used for PAM-4 data gray-coded in the transmitter [3]. The logic gates also perform majority voting so that the number of outputs from comparators having different reference voltages can be reduced. In [4], both middle transition elimination and majority voting are done in the digital domain. However, performing these operations in the digital filter can result in the latency problem.

We propose a novel PAM-4 phase detector structure in which a newly proposed selective transition detector (STD) simultaneously performs elimination of the middle transition and majority voting with simple logic gates. In addition, we use the rotating phase detection scheme [7], [8] for realizing a quarter-rate PAM-4 BBPD for achieving reduction both in power consumption and chip area.

This brief is organized as follows. In Section II, the structure of our PAM-4 CDR including the novel STD and the edge-rotating technique is explained. Section III gives details of circuit implementation for key building blocks. Section IV discusses measurement results of our prototype chip. Section V gives the conclusion.

II. PAM-4 CDR Architecture

A. Selective Transition Detector

Fig. 2 shows the numbers of possible UP and DN signals produced for each of three different types of PAM-4 data transitions (minor, middle, and major) as a function of $\Delta\theta$ representing the phase difference between edge sampling clock and data transition. For minor transitions corresponding to 00 $\Leftrightarrow$ 01, 01 $\Leftrightarrow$ 10, or 10 $\Leftrightarrow$ 11 transitions, only one of three UP signals ($UP_{\rm H}$, $UP_{\rm M}$, $UP_{\rm L}$) becomes high when $\Delta\theta > 0$ and only one of DN signals ($DN_{\rm H}$, $DN_{\rm M}$, $DN_{\rm L}$) becomes high when $\Delta\theta < 0$, which are the same as the usual BBPD characteristics. For the middle transitions corresponding to 00 $\Leftrightarrow$ 10 or 01 $\Leftrightarrow$ 11, two among three UP signals become high when $\Delta\theta > \theta_1$ and two among three DN signals become high when $\Delta\theta < -\theta_1$. However, there is one UP signal and one DN signal when $-\theta_1 < \Delta\theta < \theta_1$. For major transition that correspond to 00 $\Leftrightarrow$ 11, there are three UP signals when $\Delta\theta > \theta_2$ and three DN signals when $\Delta\theta < -\theta_2$, but two UP signals and one DN signal when $0 < \Delta\theta < \theta_2$, and one UP signal and two DN signals when $-\theta_2 < \Delta\theta < 0$.

The middle transition information can be eliminated by taking three-input XOR operation, which produces high value when the odd number of inputs are high, on $UP_{\rm H}$, $UP_{\rm M}$, $UP_{\rm L}$ producing $UP_{\rm XOR}$, and on $DN_{\rm H}$, $DN_{\rm M}$, $DN_{\rm L}$ producing $DN_{\rm XOR}$. As shown in Fig. 3(a), for minor transitions, $UP_{\rm XOR}$ and $DN_{\rm XOR}$ contain same characteristics as the conventional BBPD. However, for middle transitions, both of $UP_{\rm XOR}$ and $DN_{\rm XOR}$ are high only when $-\theta_1 < \Delta\theta < \theta_1$, thus providing no UP or DN transition information, or 'Hold' status and achieving middle transition information elimination. However, for major transitions, $UP_{\rm XOR}$ and $DN_{\rm XOR}$ do not correspond to the desired characteristics. In $0 < \Delta\theta < \theta_2$, although the $UP_{\rm XOR}$ should be high, it becomes low, and $DN_{\rm XOR}$ becomes low when $-\theta_2 < \Delta\theta < 0$. This can be corrected with $UP_{\rm OR}$ and $DN_{\rm OR}$, which are produced with 3-input OR operation on $UP_{\rm H}$, $UP_{\rm M}$, $UP_{\rm L}$ and $DN_{\rm H}$, $DN_{\rm M}$, $DN_{\rm L}$, respectively. All PAM-4 signal transition information can be obtained with proper logic combinations of $UP_{\rm XOR}$, $UP_{\rm OR}$, $DN_{\rm XOR}$, and $DN_{\rm OR}$ logic values, as described in Table I. Some transitions that do not occur are not included in Table I. Those combinations in Table I can be implemented with a Karnaugh map and can be expressed as,

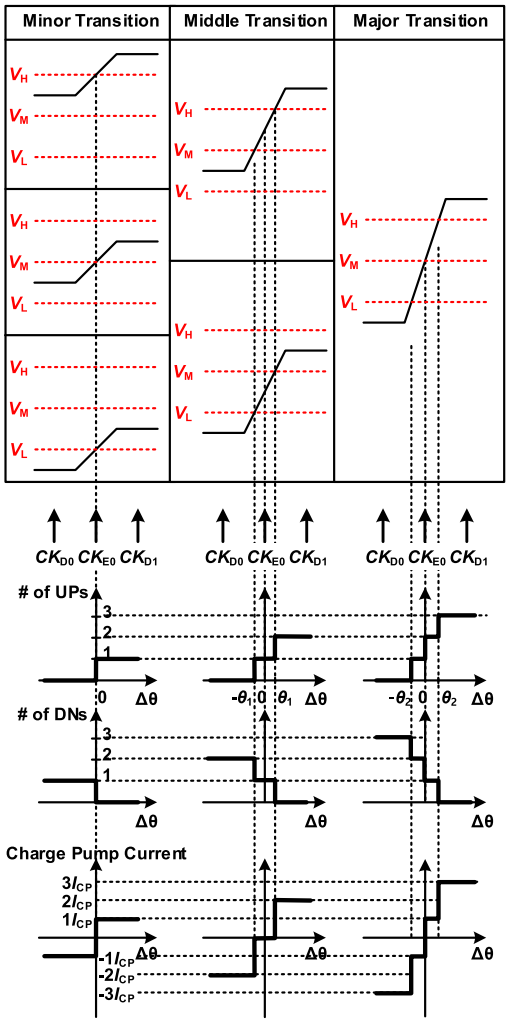

Fig. 2. UP/DN numbers for PAM-4 Transitions.

$$\mathrm{UP} = UP_{\rm XOR} \cdot \overline{DN_{\rm OR}} + UP_{\rm OR} \cdot DN_{\rm XOR} \quad (1)$$

$$\mathrm{DN} = UP_{\rm XOR} \cdot DN_{\rm OR} + \overline{UP_{\rm OR}} \cdot DN_{\rm XOR} \quad (2)$$

As shown in Fig. 3(b) and (c), final UP/DN signals produced by STD show same characteristics as BBPD regardless of transition types. In our design, in order to minimize delay mismatches, identical logic gate structures composed of 2-input NAND gates are used for producing $UP_{\rm XOR}$, $UP_{\rm OR}$, $DN_{\rm OR}$ and $DN_{\rm XOR}$ signals.

In order to compare the operation of our STD with a conventional BBPD, behavior-level simulations are performed with PAM-4 data having 9 mUI rms jitter. The BBPD structure shown in Fig. 1(a) with and without STD is used for simulation with an ideal charge pump having 50μA. Fig. 4 shows the simulation results when PAM-4 input data have three different input slew rates. $T_{\rm T}$ is the input data rise/ fall time, and $T_{\rm D}$ represents one UI. As shown in Fig. 4, our STD produces the desired characteristics regardless of input slew rate variations, whereas the PD characteristics of the conventional structure show significant changes when input slew-rate changes.

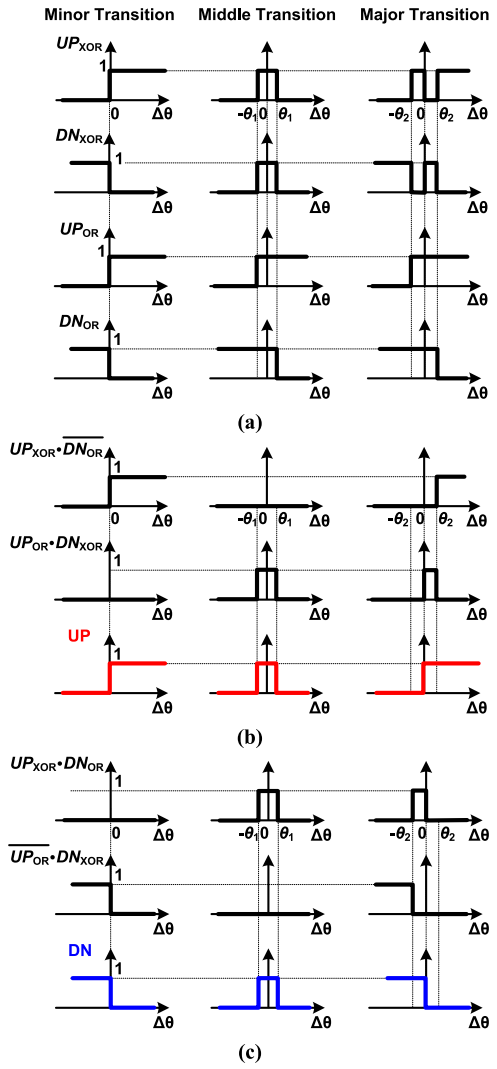

Fig. 3. (a) Output of 3-input XOR and OR for different transitions, (b) UP operation, and (c) DN operation.

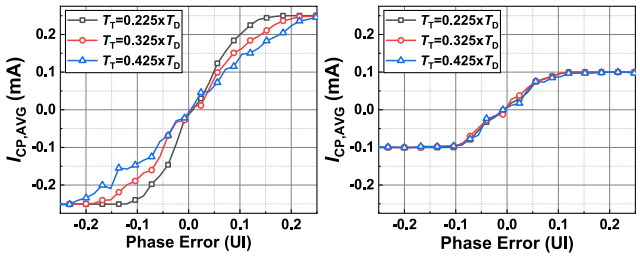

Fig. 4. Ideal simulation of (a) conventional phase detector gain with variations of input slew-rate, and (b) phase detector having a STD with variations of input slew-rate.

B. Edge-Rotating Technique

Although our STD can be used for any type of CDR, our CDR is implemented in the quarter rate so that the burden of buffering high-speed signals can be reduced and a simple ring-type VCO, which occupies much less chip area than LC VCO, can be used. Furthermore, in order to further reduce the complexity of the CDR, we use the edge-rotating technique [7] in which the locking point is determined with a single clock phase among sequentially rotating phases. Fig. 5 shows the generation of rotational signal, and the timing operation of

TABLE I
PAM SIGNAL TRANSITION STATE ACCORDING TO $UP_{XOR}UP_{OR}DN_{XOR}DN_{OR}$

$UP_{XOR}UP_{OR}DN_{XOR}DN_{OR}$	Transitions	Status
0 0 0 0	No transition	Hold
0 0 0 1	# of DNs = 2 (Middle Transition)	Hold
0 0 1 1	# of DNs = 1 or 3 (Minor or Major Transition)	DN
0 1 0 0	# of UPs = 2 (Middle Transition)	Hold
0 1 1 1	# of UPs = 2 # of DNs = 1 (Major Transition)	UP
1 1 0 0	# of UPs = 1 or 3 (Minor or Major Transition)	UP
1 1 0 1	# of DNs = 2 # of UPs = 1 (Major Transition)	DN
1 1 1 1	# of DNs = 1 # of UPs = 1 (Middle Transition)	Hold

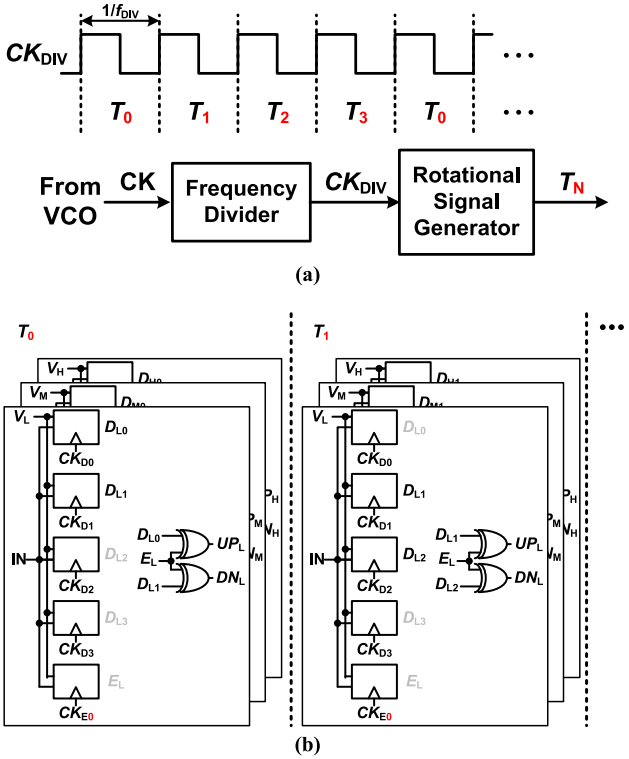

Fig. 5. (a) Generation of rotational signal, and (b) timing operations of edge-rotating BBPD.

CDR employing the edge-rotating technique. The dividing ratio of 16 is used in our design in order to make sure the rotation speed is larger than the CDR loop bandwidth and no CDR performance degradation is caused by the edge rotation [8].

One of edge-sampling clocks ($CK_{E0\text{-}3}$) is selected and used for sampling according to $T_{0\text{-}3}$, which rotates in synchronization with the divided clock (CK_{DIV}). Data sampling clocks ($CK_{D0\text{-}3}$) are continuously supplied to recover data without

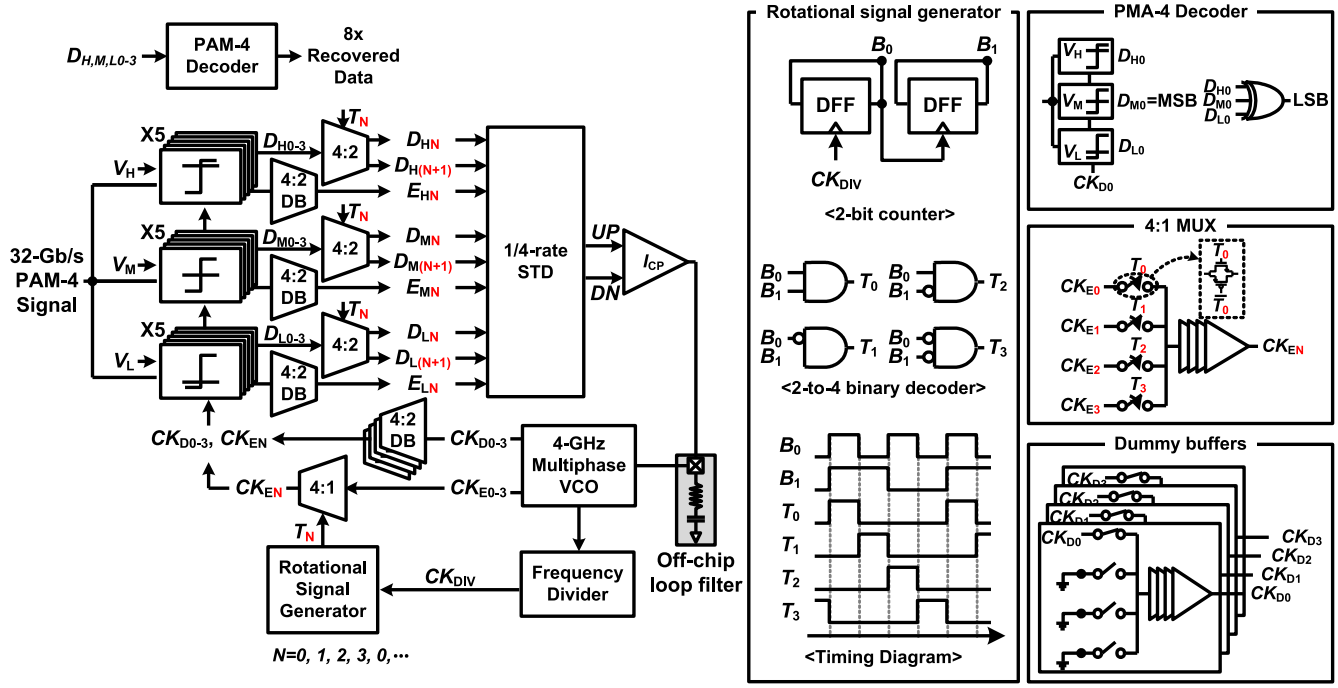

Fig. 6. Block diagram of proposed PAM-4 CDR.

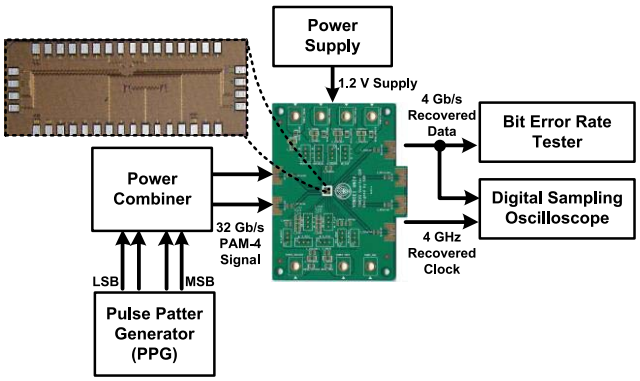

Fig. 7. Chip microphotograph and measurement setup.

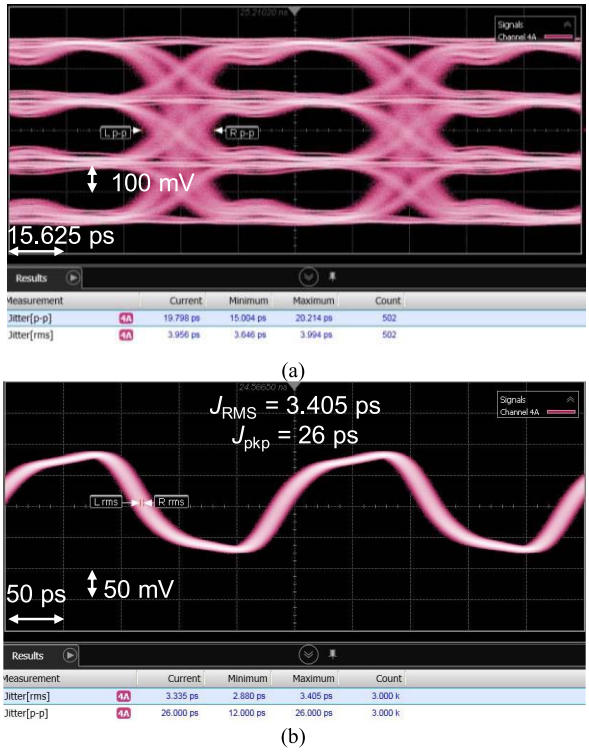

Fig. 8. Eye-diagrams of (a) PAM-4 input, and (b) recovered clock.

loss. Compared with conventional multi-phase PAM-4 CDR, our CDR with the edge-rotation scheme can save 9 comparators and 3 clock buffers. With this, our CDR has 39 % less power consumption and 18 % less chip-area when designed in 28-nm CMOS, even though it requires addition of a frequency divider, a rotational signal generator, a 4:1 MUX and 3 4:2 MUXs as shown in Fig. 6.

III. Circuit Implementation

Fig. 6 shows the block diagram of our quarter-rate edge-rotating PAM-4 CDR with the STD. It is composed of 15 comparators, three 4:2 MUXs, one of 4:1 MUX, frequency divider, rotational signal generator, charge pump, multiphase VCO and 1/4-rate STD. The reference voltages (V_H, V_M, and V_L) for comparators are externally provided. The charge pump has the structure given in [9]. The loop filter is implemented off-chip. The Lee-Kim delay cell [10] is used for producing multiphase clocks. The divided-by-16 clock signal is used for generating rotating signals.

4:1 MUXs for rotating edge-sampling clocks are designed with the structure shown in Fig. 6. 4:1 dummy buffers (DB) having the same structures are also used to minimize the phase skew between data-sampling and edge-sampling clocks. These schemes are also used for 4:2 MUXs and 4:2 DBs for BBPD outputs to minimize the skew between sampled data by CK_{EN} and $CK_{D0\text{-}3}$.

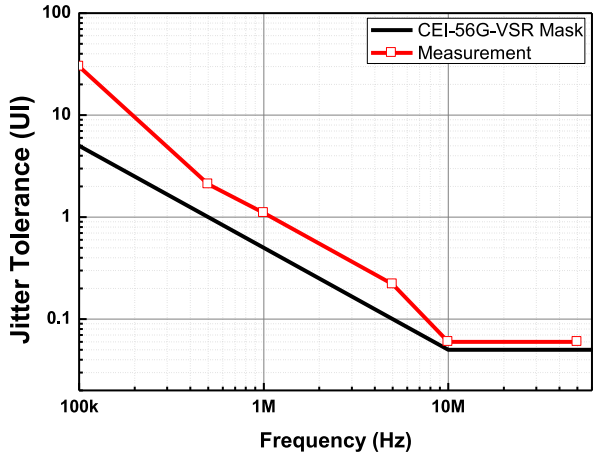

Fig. 9. Measured jitter tolerance.

TABLE II
PAM-4 CDR PERFORMANCE COMPARISON

	[4]	[11]	This work
Data Rate (Gb/s)	**22**	**54.1-56.8**	**32**
Receiver Clock jitter	**J_{rms}=1.64 ps J_{pkp}=13.3 ps @ 1.4 GHz**	**J_{rms}=0.53 ps J_{pkp}=2 ps @ 28 GHz**	**J_{rms}=3.8 ps J_{pkp}=22.2 ps @ 4 GHz**
Power consumption (mW)	**228***	**180**	**32**
Power efficiency (mW/Gbit/s)	**10.4**	**3.2**	**1**
Chip Area (mm^2)	**1**	**1.6**	**0.022**
Technology	**90 nm SOI CMOS**	**40nm CMOS**	**28 nm CMOS**

* Includes PRBS checker

As shown in the Fig. 6, a 2-bit counter and a 2-to-4 binary decoder generate 4-bit digital codes (T_0, T_1, T_2, T_3) for selecting the correct edge-tracking clock and sampled data outputs in synchronization with divided-by-16 clock signal.

PAM-4 decoder recovers PAM-4 signal into deserialized 8 lanes. As shown in Fig. 6, the recovered and deserialized MSB can be produced by sharing the sampler used in BBPD, and the LSB is produced by 3-input XORs using BBPD outputs (D_{H0}, D_{M0}, D_{L0}) when the sampling clock is CK_{D0}.

IV. Measurement Results

A prototype quarter-rate 32-Gb/s PAM-4 CDR with the STD is implemented in 28-nm CMOS technology. The chip microphotograph and the measurement setup are shown in Fig. 7. The circuit consumes 32 mW at 1.2-V supply voltage and occupies 0.022 mm^2 excluding output buffers. The chip is mounted on a FR-4 printed circuit board and wire-bonded for measurement. A 2-channel pulse pattern generator (PPG) produces two 16-Gb/s PRBS 2^7-1 data sequences for MSB and LSB, which are combined with a power combiner and introduced to our CDR. The recovered deserialized NRZ data and clock signals are measured by a digital sampling scope and the bit error rate is measured by a BERT. No error was observed in any of 8 lanes while 4 x 10^{12} bits were transmitted.

Fig. 8 shows the eye-diagram of input PAM-4 data and the recovered clock signals. No error was observed while 4 x 10^{12} bits were transmitting and the recovered clock has rms jitter of 0.0136 UI, which is mostly due to ring-type VCO used in our CDR.

Fig. 9 shows the result of the jitter tolerance measurement for BER less than 10^{-12} with PRBS 2^7-1 input data. Our CDR satisfies the jitter tolerance mask for CEI-56G-VSR.

The performance of our CDR is compared in Table II with those of previously reported PAM-4 CDRs. As can be seen in the table, our CDR has smaller power consumption and chip area. Our CDR shows worse jitter performance for the recovered clock. This is primary due to the ring-type VCO that we used. An external clock is used in [4] and LC VCO is used in [11], both of which should provide much better jitter performance for the recovered clock signal.

V. Conclusion

A quarter-rate 32-Gb/s PAM-4 CDR having a novel phase detector structure, STD, is demonstrated. The STD produces the desired UP/DN signals very efficiently. In addition, the edge-rotating technique reduces power consumption and chip area. A prototype CDR realized in 28-nm CMOS technology successfully demonstrates.

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References

[1] H. Ju, M.-C. Choi, G.-S. Jeong, W. Bae, and D.-K. Jeong, "A 28 Gb/s 1.6 pJ/b PAM-4 transmitter using fractionally spaced 3-tap FFE and G_m-regulated resistive-feedback driver," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 12, pp. 1377–1381, Dec. 2017.

[2] X. Song and D. Dove, *Opportunities for PAM4 Modulation*, IEEE 802.3 400GbE Study Group. [Online]. Available: www.ieee802.org

[3] J. L. Zerbe *et al.*, "Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2121–2130, Dec. 2003.

[4] T. Toifl *et al.*, "A 22-Gb/s PAM-4 receiver in 90-nm CMOS SOI technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 954–965, Apr. 2006.

[5] A. Nazemi *et al.*, "3.4 a 36Gb/s PAM4 transmitter using an 8b 18GS/S DAC in 28nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Paper*, vol. 58, 2015, pp. 58–59.

[6] B. Hu *et al.*, "A capacitor-DAC-based technique for pre-emphasis-enabled multilevel transmitters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 9, pp. 1012–1016, Sep. 2017.

[7] H. Li *et al.*, "A 0.8V, 560fJ/bit, 14Gb/s injection-locked receiver with input duty-cycle distortion tolerable edge-rotating 5/4X sub-rate CDR in 65nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Paper*, Honolulu, HI, USA, 2014, pp. 1–2.

[8] D.-H. Kwon, Y.-S. Park, and W.-Y. Choi, "A clock and data recovery circuit with programmable multi-level phase detector characteristics and a built-in jitter monitor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1472–1480, Jun. 2015.

[9] J. S. Lee, W. K. Jin, D. M. Choi, G. S. Lee, and S. Kim, "A wide range PLL for 64x speed CD-ROMS & 10X speed DVD-ROMS," *IEEE Trans. Consum. Electron.*, vol. 46, no. 3, pp. 487–493, Aug. 2000.

[10] J. Lee and B. Kim, "A low-noise fast-lock phase-locked loop with adaptive bandwidth control," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 430–438, Aug. 2000.

[11] J. Lee, P.-C. Chiang, P.-J. Peng, L.-Y. Chen, and C.-C. Weng, "Design of 56 Gb/s NRZ and PAM4 SerDes transceivers in CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2061–2073, Sep. 2015.