Equivalent Circuit Model for CMOS-Compatible Avalanche Photodetectors

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Equivalent Circuit Model for CMOS-Compatible Avalanche Photodetectors

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This certifies that the master's thesis of Myung-Jae Lee is approved.

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Abstract

Equivalent Circuit Model for CMOS-Compatible Avalanche Photodetectors

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An equivalent circuit model for CMOS-compatible avalanche photodetectors (CMOS-APDs) is developed. CMOS-APDs have an inductive component as well as a capacitive component in an avalanche region. It is expected that these inductive and capacitive components can cause resonance which results in rf peaking in photodetection frequency response. Using the equivalent circuit model, the bandwidth enhancement caused by the rf-peaking effect is explained obviously.

The CMOS-APDs model based on the physical structure is proposed

and the model includes the inductive component for avalanche delay. Considering the photodetection response, CMOS-APDs are limited by not only the RC time and transit time, but also diffusion time constant, and thus a dual current source model should be used for time delay of photogenerated carriers.

To investigate characteristics of the fabricated CMOS-APD, current-voltage characteristics and avalanche gain are studied on an experimental basis. Reflection coefficients are measured at P^+ port, using a vector network analyzer (VNA) with on-wafer calibrations. And then parameters of the CMOS-APD are extracted by fitting the modeling results to the corresponding measured data. It makes clear the inductive component of the device and inverse proportion between the inductance and the bias current. Furthermore, the measured photodetection frequency response of the CMOS-APD is fitted using the dual current source model at different bias conditions. The 3-dB bandwidth increases considerably up to 3.83 GHz due to the rf-peaking effect in photodetection frequency response.

Using the equivalent circuit model, the bandwidth enhancement due to the rf-peaking effect is explained well by the inductance of the avalanche region. The dependence of rf-peaking frequency in the photodetection frequency response on bias currents is clearly explained

by the relationship between the extracted inductance and the bias current. And it is expected that the developed model can support the analysis of CMOS-APDs operation.

Keywords: CMOS, avalanche photodetector, equivalent circuit model, dual current source model, rf peaking

Ⅰ. Introduction

The receivers for the long distance optical communications are realized with expensive technologies such as InGaAs-InP heterojunction bipolar transistors (HBTs)-based photoreceiver [1], [2] and InP high-electron mobility transistors (HEMTs)-based photoreceiver [3], [4] in general. The reasons for validity of these expensive systems are long distance links and a lot of users per channel. That is, the cost per length of the fiber and the cost per user are low [5].

The receivers should not be expensive for short and medium distance optical communications, ranging from centimeters up to hundreds of meters, like a small number of users per link. Local-area networks (LANs), fiber-to-the-home, board-to-board optical interconnections, and chip-to-chip optical interconnections are examples of these communications [6], [7].

850 nm optical communications have already been widely used for short distance applications because high-speed and low-cost vertical-cavity surface-emitting lasers (VCSELs) as optical transmitter [8], [9] and multi-mode fibers (MMFs) as optical medium are easily available. Si monolithic integrated optical receivers with standard CMOS technology are as good as VCSELs and MMFs because standard

CMOS technology has the advantages of low fabrication cost and high-volume production.

CMOS-compatible photodetectors (CMOS-PDs) can provide cost-effective solutions for 850 nm optical access networks because integrated optical receivers including photodetectors and electronic circuits can be realized with mature CMOS technology. Therefore, the number of investigations on optical receivers with photodetectors integrated in CMOS process is increasing steadily. However, CMOS-PDs have the inherent drawback of low responsivity on account of the low absorption coefficient of Si at 850 nm and the narrow depletion region formed by P^+/N-well and N-well/P-substrate junctions. Moreover, CMOS-PDs have small bandwidth owing to slow diffusive carriers [10]. To overcome these disadvantages, avalanche photodetectors (APDs) are very attractive because of their internal gain. In addition, it is reported that CMOS-compatible avalanche photodetectors (CMOS-APDs) have the inductive component as well as the capacitive component in the avalanche region [11]. It is expected that these inductive and capacitive components can cause resonance which results in rf peaking in photodetection frequency response.

In this thesis, therefore, an equivalent circuit model of CMOS-APDs based on the physical structure is introduced. The model includes the

inductive component for avalanche delay in the avalanche region and dual current sources for time delay of photogenerated carriers. By performing the measurements and parameter extraction of the equivalent circuit components with impedance characteristics and photodetection frequency responses at several bias conditions, rf-peaking frequency dependent on the bias current is clearly examined.

Ⅱ. Characteristics of the Avalanche Region

There are two time delays which cause the current to lag behind the voltage. One is the avalanche delay by reason of the finite build-up time of the avalanche current. The other is the transit time delay because of the finite time for carriers to cross the drift region. In 1958, Read proposed a diode structure which consists of a highly localized avalanche region at one side of a depletion region [12]. The one-sided abrupt P-N junction diode which gives an approximation to the Read diode is proposed by M. Gilden and M. E. Hines [13]. Fig. 1 shows cross-section of the one-sided abrupt junction diode and electric-field distribution. In this case, the P^+ region is highly doped and the avalanche region is confined to the narrow region near the highest electric-field. In the depletion region, the outside of the avalanche region is called the drift region. Fig. 2 shows the model of the Read diode which consists of the avalanche, drift, and inactive region. The avalanche region is assumed to be thin so that space charge and signal delay can be ignored. In the drift region, no carriers are generated and all carriers enter the drift region from the avalanche region. At this time, the carriers transit at their saturation velocity. The inactive region acts as a parasitic resistance. $\tilde{I}_a$ is the ac conduction current in the

avalanche region and $\tilde{I}_c$ is the ac conduction current in the drift region. $\tilde{I}_c$ propagates as an unattenuated wave with only phase change owing to the assumption of a saturated drift velocity v_s. The displacement current, $\tilde{I}_d$, is related to the ac electric-field $\tilde{E}(x)$. To be considered the avalanche region, Gilden and Hines evinced that the ac component of the avalanche conduction current can be approximated from the equation,

$$\tilde{I}_a = \frac{2\alpha' x_a I_0 \tilde{E}_a}{j\omega\tau_a} \tag{1}$$

and the displacement current in the avalanche region is simply given by [13], [14]

$$\tilde{I}_{ad} = j\omega\varepsilon_s \tilde{E}_a A. \tag{2}$$

where

$\alpha' \equiv \partial\alpha/\partial E$

α	ionization coefficient
x_a	width of the avalanche region
I_0	bias current
$\tilde{E}_a$	small-signal quantity of ac electric-field
$\tau_a = x_a/v_s$	transit time in the avalanche region
ε_s	semiconductor permittivity
A	cross-section area

The above two equations are the two elements of the total current in the avalanche region. For a given electric-field, the avalanche conduction current varies inversely with ω like an inductor and the displacement current in the avalanche region varies directly with ω like a capacitor. Therefore, the avalanche region operates as an LC parallel resonant circuit. The equivalent circuit of the avalanche region is shown in Fig. 3. The inductance and capacitance of the avalanche region are

$$L_a = \frac{\tau_a}{2\alpha' I_0}, \tag{3}$$

$$C_a = \frac{\varepsilon_s A}{x_a}. \tag{4}$$

The inductance of the avalanche region, L_a, is inversely proportional to the bias current, I_0.

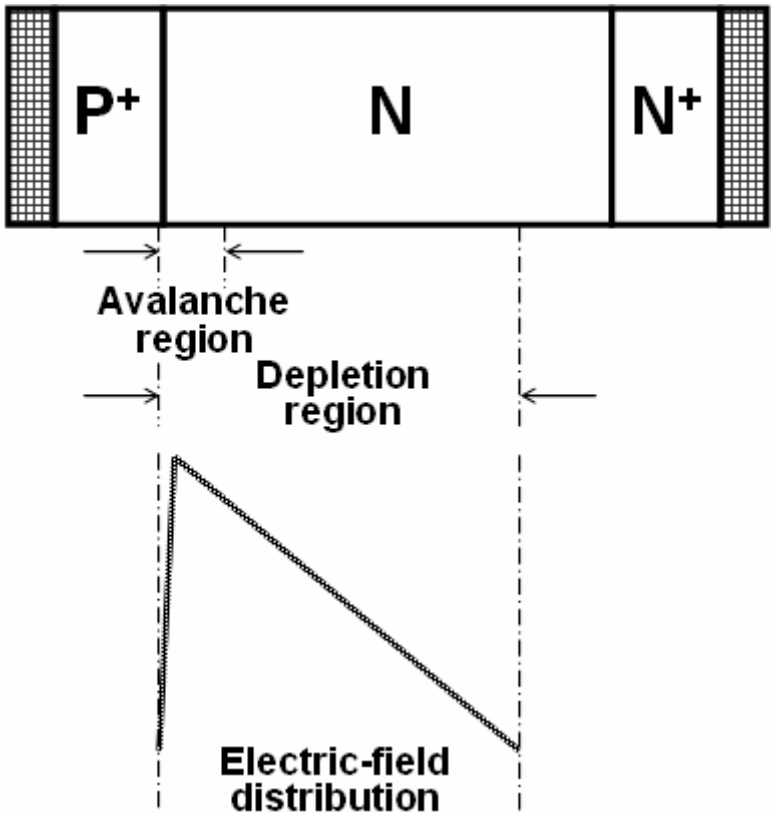


Fig. 1. Cross-section of the one-sided abrupt junction diode with electric-field distribution.

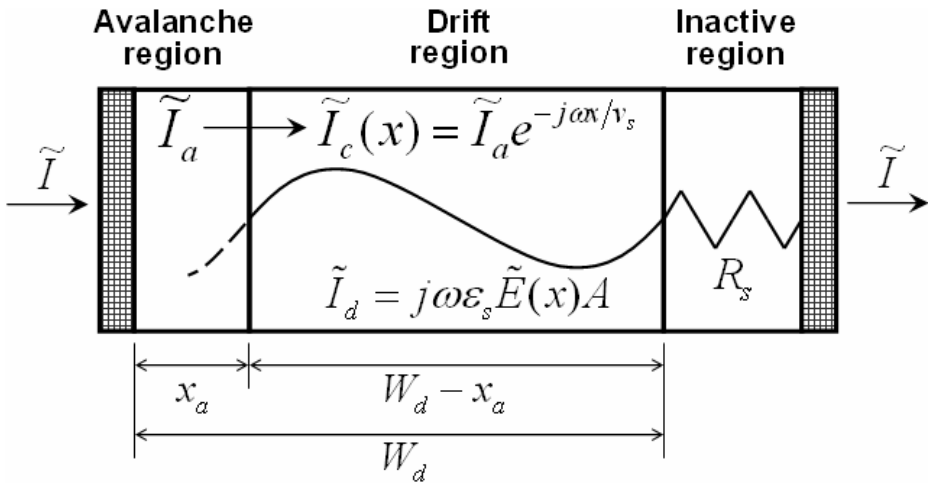


Fig. 2. Model of the Read diode. '~' indicates small-signal ac quantities.

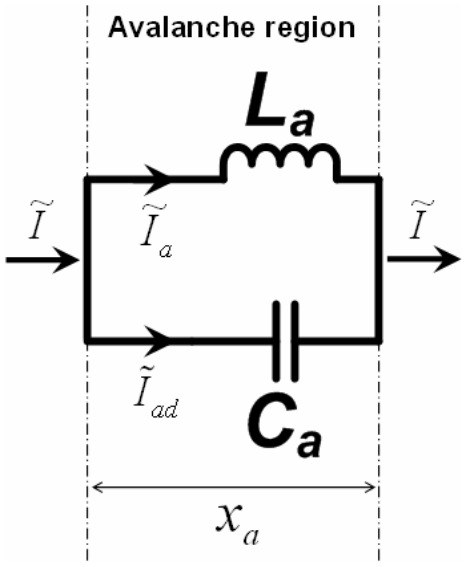


Fig. 3. Equivalent circuit for the avalanche region.

Ⅲ. Carrier Time Constants of the CMOS-APD

For one-sided abrupt P^+/N-well junction, the avalanche breakdown voltage, V_B, is calculated as functions of the critical field, E_c, and the donor concentration, N_D [14].

$$V_B = \frac{E_c W}{2} = \frac{\varepsilon_s E_c^2}{2q}\left(N_D\right)^{-1} . \tag{5}$$

And E_c is calculated as function of N_D [14]. From equation (5), N_D is about 1.5×10^{17} cm^{-3} when V_B is about 10 V. At sufficiently large fields, the drift velocity approaches a saturation velocity, v_s, which is 10^7 cm/s for Si at 300 K. If it is assumed that the acceptor concentration, N_A, is 1×10^{19} cm^{-3}, the depletion width for P^+/N-well junction is about 0.3×10^{-4} cm, where the built-in potential $V_{bi}\approx0.945$ V. It is presumed that the width of the avalanche region is nearly a third of the depletion width. Therefore, the transit time constant in the P^+/N-well depletion region is about 3 ps and 1.8 ps without and with the avalanche process, respectively.

Like the preceding, it is assumed that the P-substrate concentration is 1×10^{15} cm^{-3}, the depletion width for N-well/P-substrate junction is about 0.98×10^{-4} cm, where $V_{bi}\approx0.726$ V. The N-well depth is around 1×10^{-4} cm and the P^{+} depth is around 0.144×10^{-4} cm when gate length is 0.18 μm [15]. The length of undepleted region of N-well is approximately equal to 0.55×10^{-4} cm and the diffusion coefficient for holes in the undepleted region is obtained by the Einstein relationship, $D_p\approx7.77$ cm^2/sec. Thus, the diffusion time constant is about 160 ps.

The avalanche build-up time is estimated roughly a few picoseconds, where N is a constant varying from 1/3 to 2, k is the ionization coefficient ratio varying from 1 to 10^{-3} [16].

For more information, refer to the Appendix B, which shows significant equations of the P-N junction diode.

Ⅳ. Structure and Model of CMOS-APDs

A CMOS-APD was fabricated using 0.18 μm standard CMOS process as shown in Fig. 4. There are two types of P-N junctions, which are P^+/N-well junction and N-well/P-substrate junction. The vertical P^+/N-well junction is only used in order to exclude the slow diffusion currents in the substrate region that limit high speed operation [17]. Besides, multifinger electrodes with 0.5 μm spacing are employed on the active area for the exclusion of the lateral diffusion path. The active area of the CMOS-APD is about 30×30 μm^2 and the optical window is formed by blocking the salicide in the process of the fabrication.

In contrast to low bias conditions as shown in Fig. 5, when the CMOS-APDs operate in sufficient high bias conditions which are satisfied with the avalanche process, the avalanche region is modeled as a shunt combination of an inductor and a capacitor as in IMPact ionization Avalanche Transit-Time (IMPATT) diodes [14]. Fig. 6 shows CMOS-APDs model based on the physical structure. In this model, L_a is inductance of the avalanche region and C represents total depletion region capacitance between the P^+ region and N-well region. For considering the dissipative effect due to the finite reverse saturation current and field-dependent velocity, series and parallel resistors, R_a

and R_l, of the inductor are included in the equivalent circuit model [18]. The resistances of R_d and R_s are caused by the drift and inactive regions in the low doped N-well, respectively [13], [14]. In Fig. 6, the P-N junction between the N-well and P-substrate is modeled by R_{well}, C_{sub1}, R_{sub}, and C_{sub2} [19]. Due to the layout effect of multifinger electrodes and interconnect lines, C_p, L_p, and R_p are included to account for parasitic. An equivalent circuit model corresponding to the physical structure is shown in Fig. 7, where Pad is the shielded pad to block signal coupling into Si substrate. The details of the pad model will be discussed in the next chapter.

Considering the photodetection response, CMOS-APDs has an optical input port in distinction from just electrical characterization of the device. Consequently, in view of a modeling of photodiodes, the model is divided into two parts. One is an optical to electrical conversion part, which describes the generation of carriers and the carrier transport. The other is an electrical equivalent circuit model part, which represents the resistance-capacitance (RC) time [20]. Therefore, in order to characterize the photodetection response of the CMOS-APD, photogenerated current is also modeled and their time constants should be included in the current source model as shown in Fig. 8. Since the photodetection frequency response of the CMOS-APD is limited by not

only the RC time and transit time, but also diffusion time constant [21], the current source model is considered both the high-speed holes generated in depletion region and the low-speed holes generated in charge neutral region or N-well/P-substrate depletion region. Hence, the equivalent circuit model is added by dual current sources which contain time delay constants as shown in Fig. 9 [22].

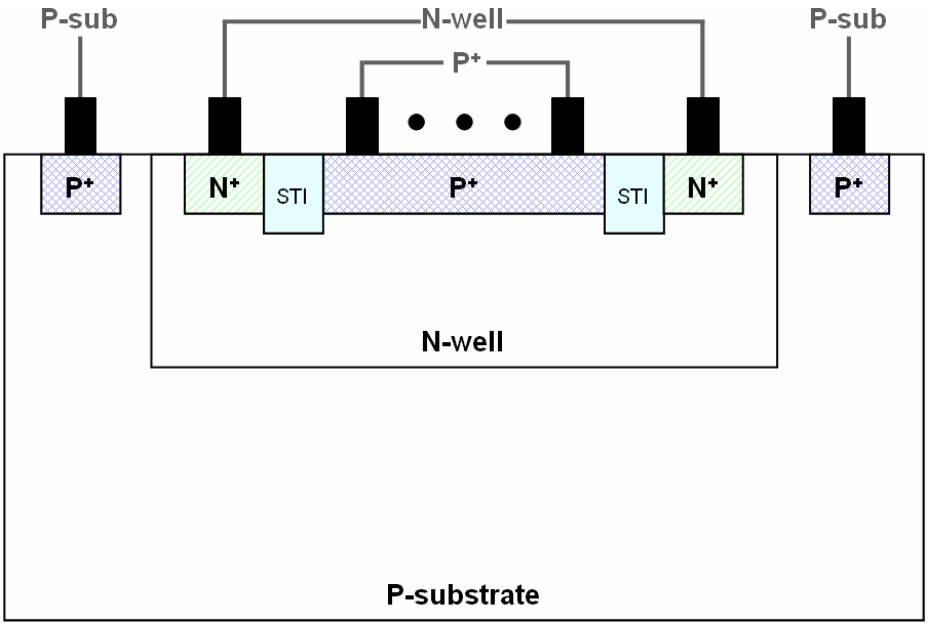


Fig. 4. Cross-section of the fabricated CMOS-APD.

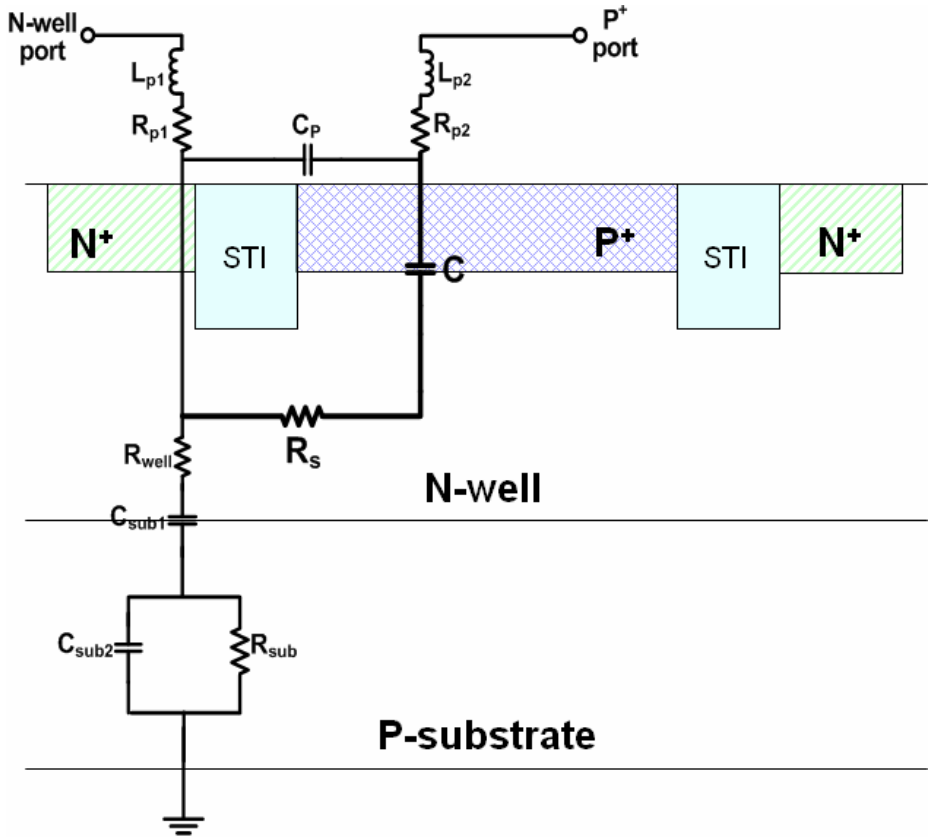


Fig. 5. CMOS-PDs model based on the physical structure.

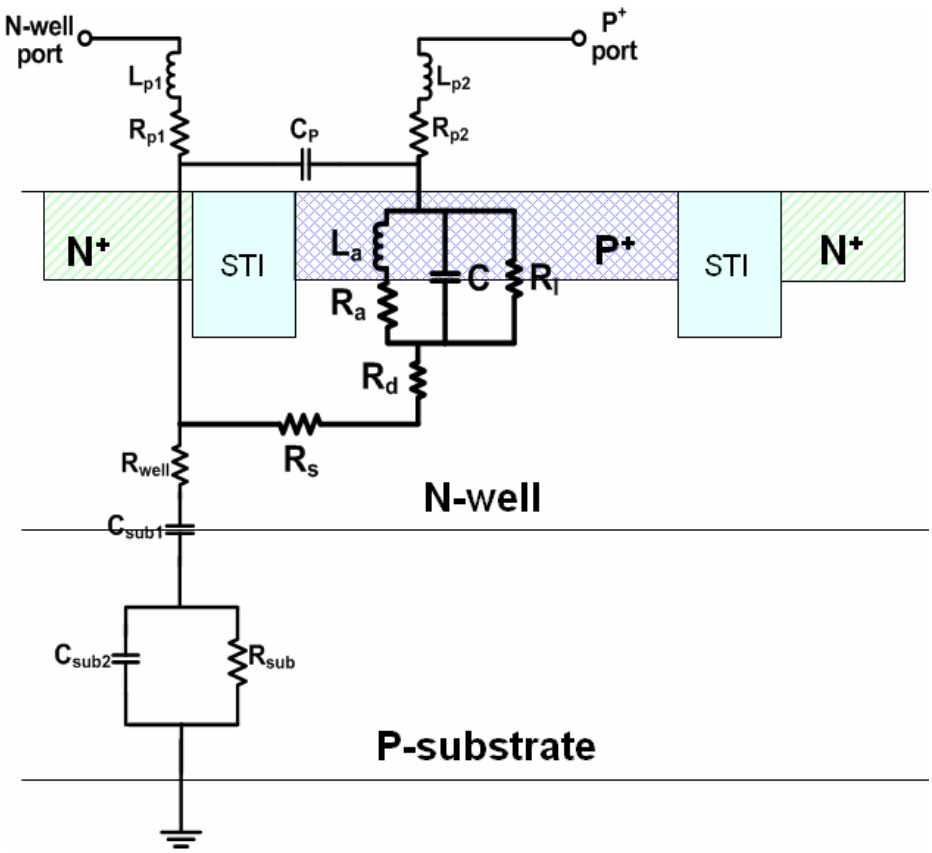


Fig. 6. CMOS-APDs model based on the physical structure.

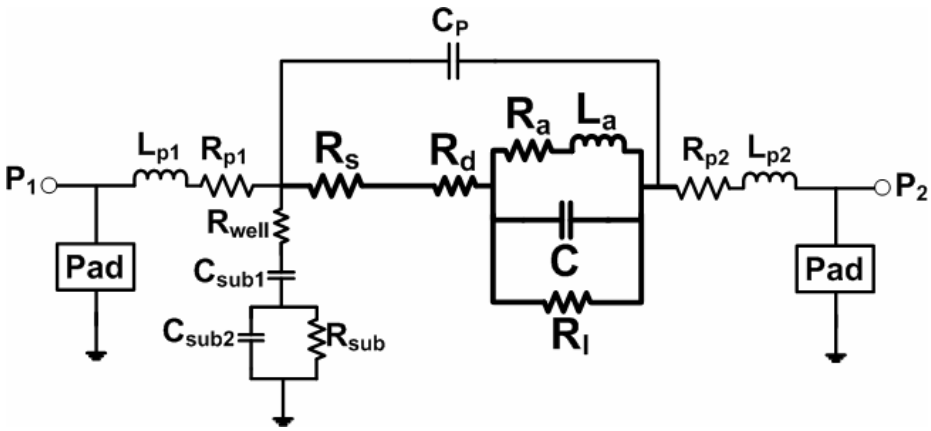


Fig. 7. Equivalent circuit model of CMOS-APDs including pads.

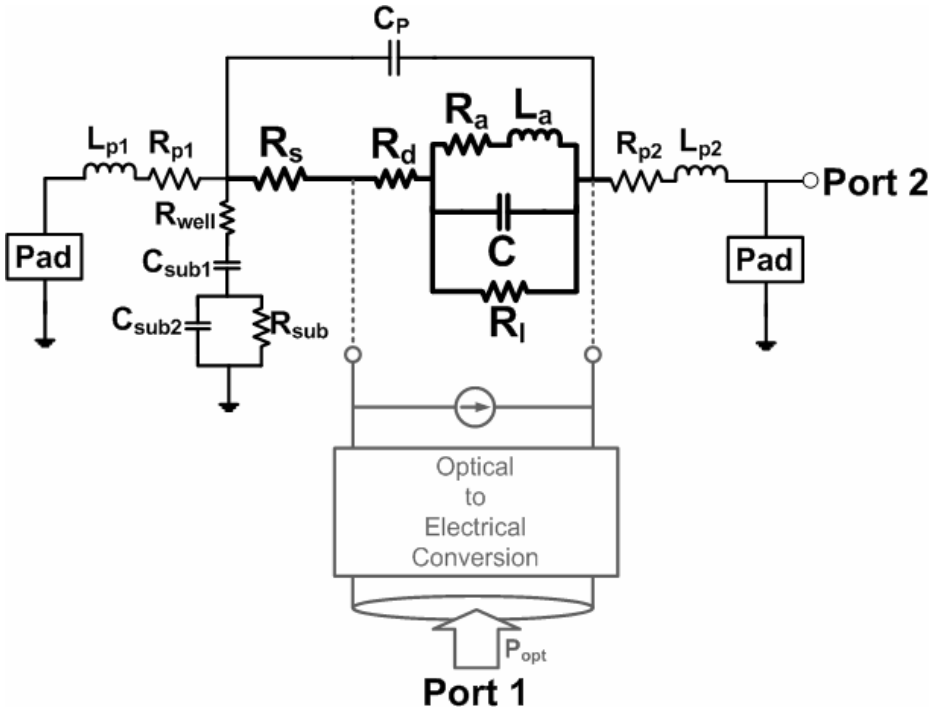


Fig. 8. Equivalent circuit model of CMOS-APDs including pads and an optical to electrical conversion part.

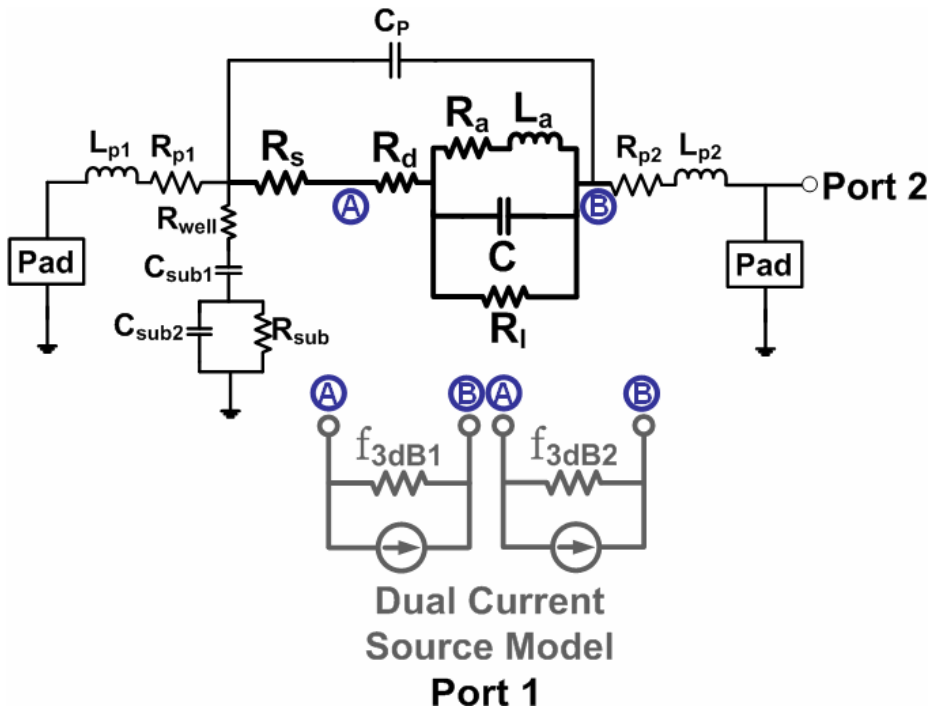


Fig. 9. Equivalent circuit model including pads and the dual current source model.

Ⅴ. Measurements and Analysis

The experimental setups for electrical and optical characterization of the CMOS-APD are shown in Fig. 10 and Fig. 11, respectively. Two-port s-parameters and photodetection frequency responses were measured at different bias conditions using a VNA for the frequency range from 50 MHz to 13.5 GHz. The VNA measures vector ratio of the transmitted and reflected energy to the incident energy on the Device under Test (DUT). In experiments, measurement cables from the VNA are connected to pads of the DUT using RF ground-signal-ground (GSG) probes. 850 nm wavelength optical signals were generated by a laser diode, and then entered the polarization controller and a 20 GHz electro-optic modulator in order. The optical coupling was executed using a multimode lensed-fiber and biases of the CMOS-APD were supplied by a semiconductor parameter analyzer. All measurements were done on wafer.

Fig. 12 shows the die microphotograph of the CMOS-APD, which includes GSG pads. The pad size is 75×75 μm^2 and the pad pitch is 150 μm.

Current-voltage characteristics of the CMOS-APD under dark and illumination conditions are shown in Fig. 13. The incident optical

power is 1 mW. The fabricated CMOS-APD has avalanche breakdown voltage of 10.25 V. Fig. 14 shows the photocurrent and avalanche gain as a function of applied reverse voltage when 1 mW optical signal is illuminated to the CMOS-APD. The photocurrent is defined by subtracting the dark current from the photodetected current of the CMOS-APD. Maximum responsivity of 0.417 A/W and avalanche gain of 162 are observed from the avalanche process, which is attributed to the increased carrier concentration. Avalanche gain is determined by the ratio of photocurrents between a given bias voltage and 1 V.

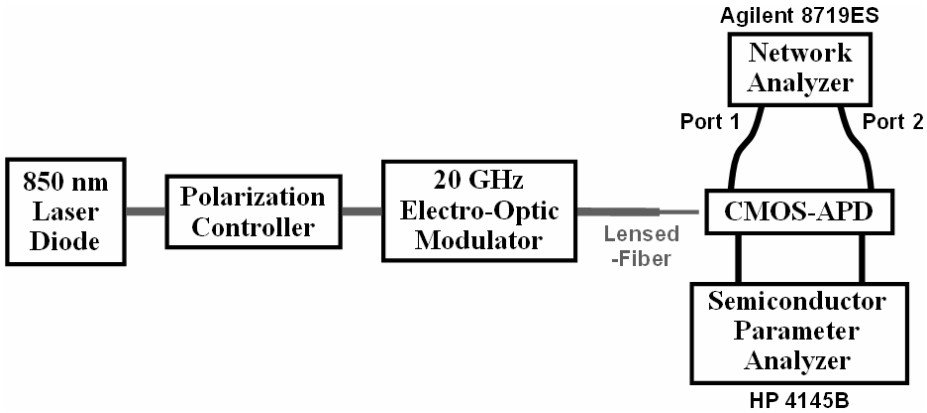


Fig. 10. Experimental setup for electrical characterization of the on-wafer CMOS-APD.

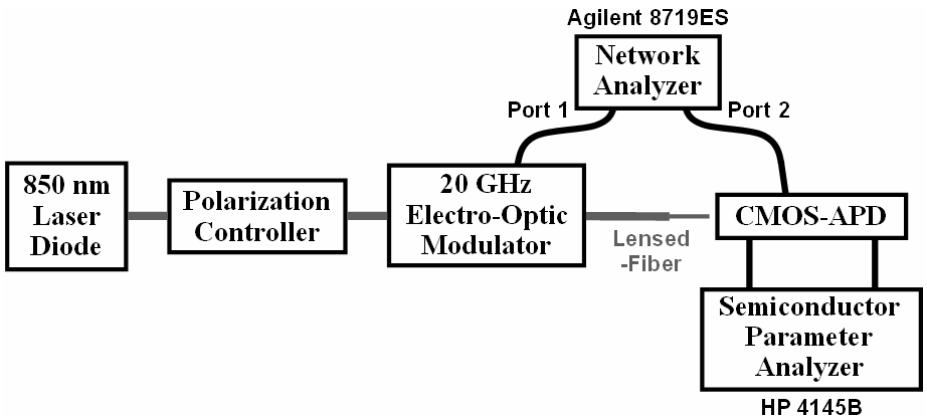


Fig. 11. Experimental setup for optical characterization of the on-wafer CMOS-APD.

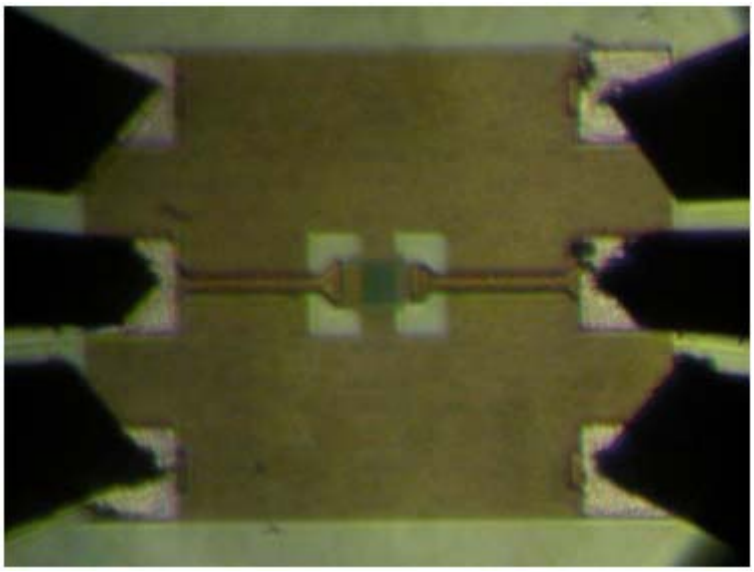


Fig. 12. Micrograph of the fabricated CMOS-APD. On-wafer probes connect GSG pads of the die for biasing and measuring.

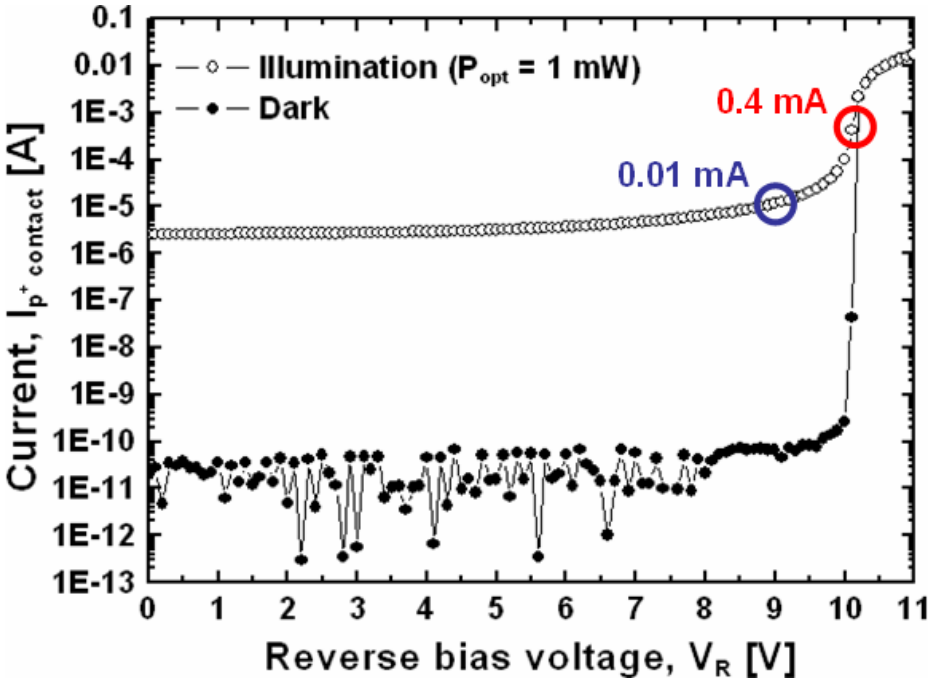


Fig. 13. I-V characteristics of the CMOS-APD under dark and illumination, 1 mW optical signal, conditions.

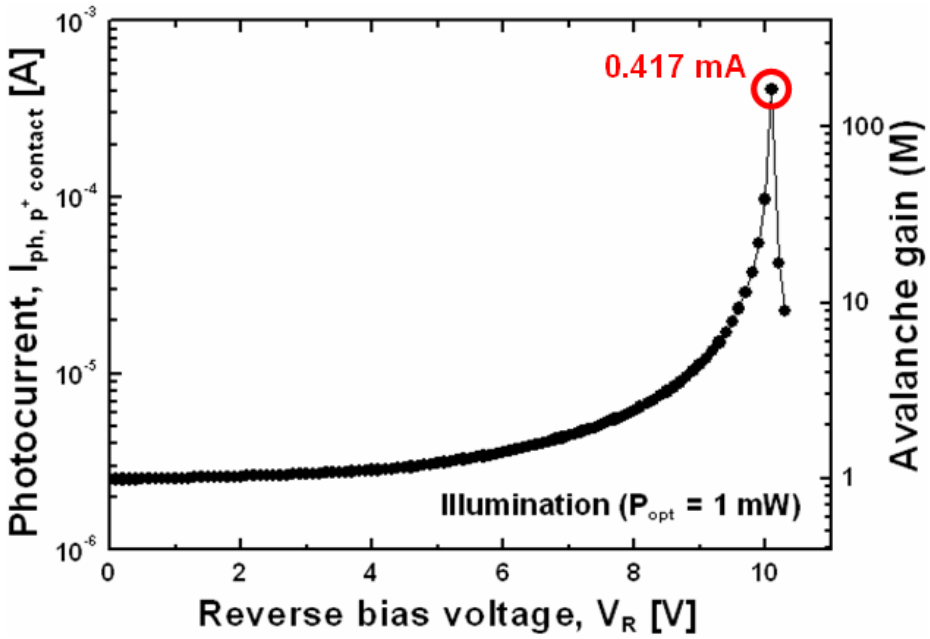


Fig. 14. Photocurrent and avalanche gain of the CMOS-APD.

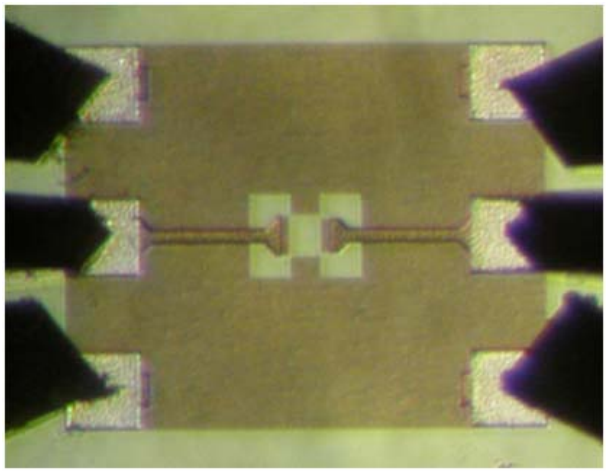
A. Electrical Characteristics of CMOS-APDs

To investigate the impedance characteristics of the CMOS-APD, electrical reflection coefficients of the device were measured from 50 MHz to 13.5 GHz using the VNA with on-wafer calibrations. For accurate parameter extraction of intrinsic components, the open-short deembedding method was used [23] because the parasitic effects of the pads and interconnect lines can be deembedded with an open and short two-step deembedding procedure. Fig. 15 shows the open and short structures for deembedding of the CMOS-APD. These structures were fabricated with the CMOS-APD on the same substrate. The pad signal is open called the open structure and the pad signal is connected with ground called the short structure. The reflection coefficients of the open and short structures were measured, and then the parasitic values of the pads and interconnect lines are extracted. The fitted results to measured data are shown in Fig. 16 and an equivalent circuit model of the shielded pad and interconnect lines is shown in Fig. 17. Table 1 shows extracted parameters of the shielded pad and interconnect lines.

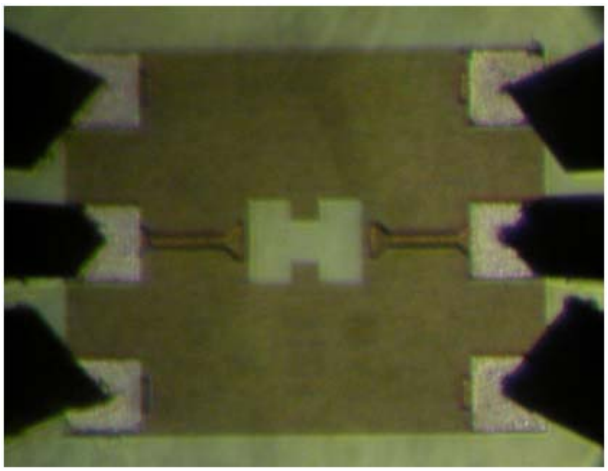
Fig. 18 shows the measured and fitted reflection coefficients of the CMOS-APD at P^+ port on Smith chart at three different bias currents, I_0 = 0.01, 0.3, and 0.4 mA, under 1 mW optical illumination. The

modeling results agree well with the measured data, it is concluded that the proposed model can describe before and after avalanche. Table 2 shows the extracted parameters of intrinsic components at five different bias currents. It is clearly verified that the CMOS-APD has the inductive component in the avalanche region at the bias current near the avalanche breakdown, which is about I_0 = 0.4 mA. Table 3 shows the inductance values of the avalanche region and the inductance-bias current product values at four different bias currents. As shown in Fig. 19, the extracted inductance values are inversely proportional to the bias current in accordance with the equation (3) as explained by chapter Ⅱ. Equation (3) shows that the product of inductance and bias current has a constant value and it can be obtained as $4.2\times10^{-12}\ V\cdot s$ using extracted parameters. Compared with the calculated inductance-bias current product, $L_a \times I_0 = \tau_a \big/ 2\alpha' \approx 4.3\times10^{-12}\ V\cdot s$, where $x_a \approx 0.13\times10^{-4}\ cm$, $v_s \approx 10^7\ cm/s$, and $\alpha' \approx 0.3\ V^{-1}$ [14], it is concluded that the extracted parameters are reasonable and the proposed model is valid in all the operating bias conditions.

The extrinsic parameters related to N-well/P-substrate junction and parasitic components are independent on the bias currents. The extracted values are shown in Table 5 (see Appendix A).



(a)



(b)

Fig. 15. (a) Open and (b) short structures for deembedding of the CMOS-APD.

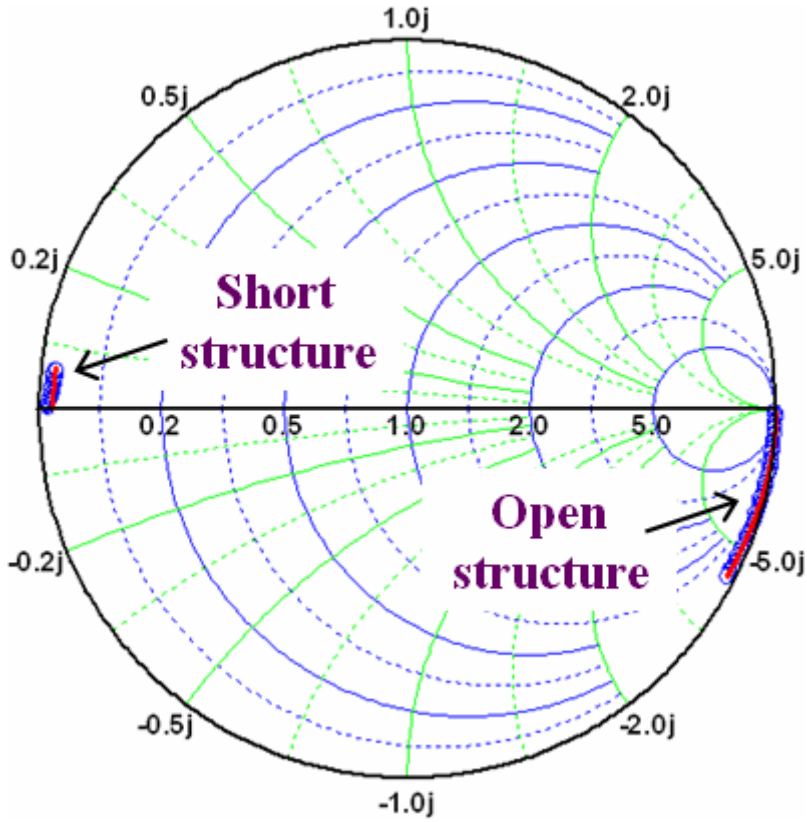


Fig. 16. Fitted results to measured data (from 50 MHz to 13.5 GHz). Hollow circles are measured data and solid lines are modeling results.

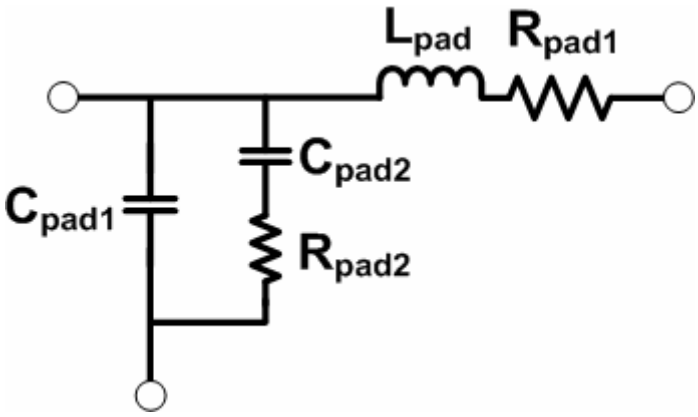


Fig. 17. Equivalent circuit model of the shielded pad and interconnect lines.

Table 1. Extracted parameters of the shielded pad and interconnect lines.

C_{pad1} [fF]	55
C_{pad2} [fF]	5
L_{pad} [pH]	35
R_{pad1} [Ω]	1
R_{pad2} [Ω]	2.5 k

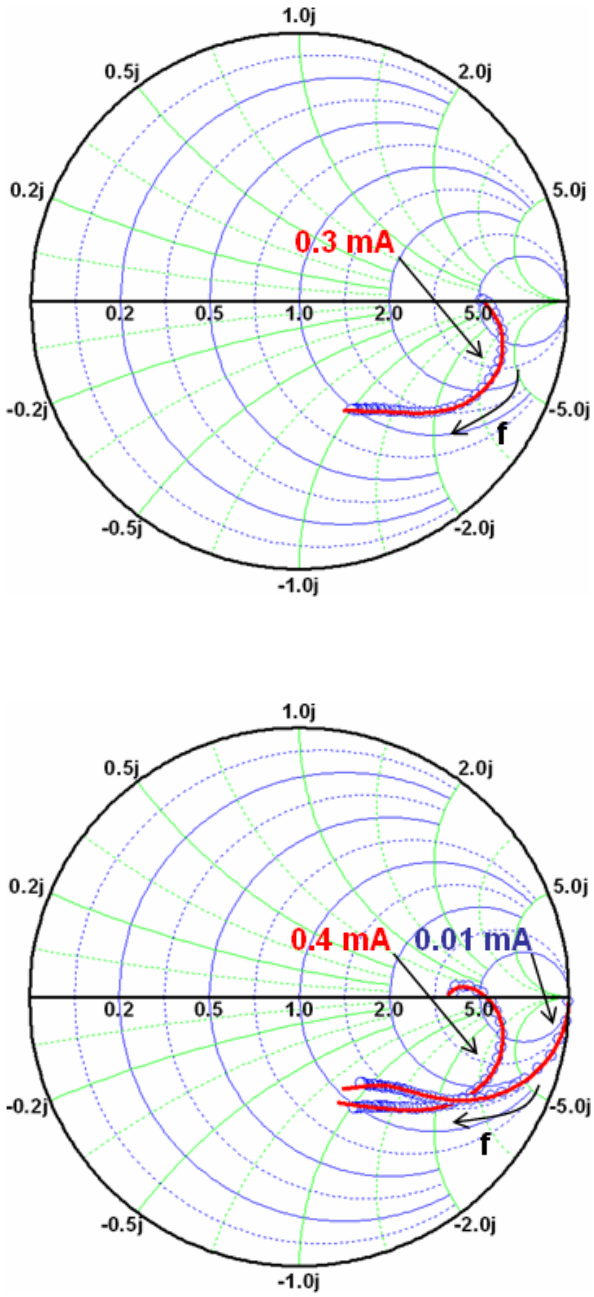


Fig. 18. Measured and fitted reflection coefficients of P^+ port (from 50 MHz to 13.5 GHz). Hollow circles represent measured data and solid lines indicate modeling results.

Table 2. Intrinsic components values

of the equivalent circuit model of the CMOS-APD.

	0.01 mA	0.3 mA	0.4 mA	0.5 mA	0.6 mA
L_a [nH]	—	14	10.5	8.4	7
R_a [Ω]	—	130	49	27	21
C [fF]	390	190	190	190	190
R_d [Ω]	—	4.16	4.16	4.16	4.16
R_l [Ω]	—	900	540	430	400
R_s [Ω]	43	74	41	32	16

Table 3. Inductance values of the avalanche region

and the inductance-bias current product values.

Bias current [mA]	Inductance [nH]	$L_a \times I_0$ [V·s]
0.3	**14**	4.2×10^{-12}
0.4	**10.5**	4.2×10^{-12}
0.5	**8.4**	4.2×10^{-12}
0.6	**7**	4.2×10^{-12}

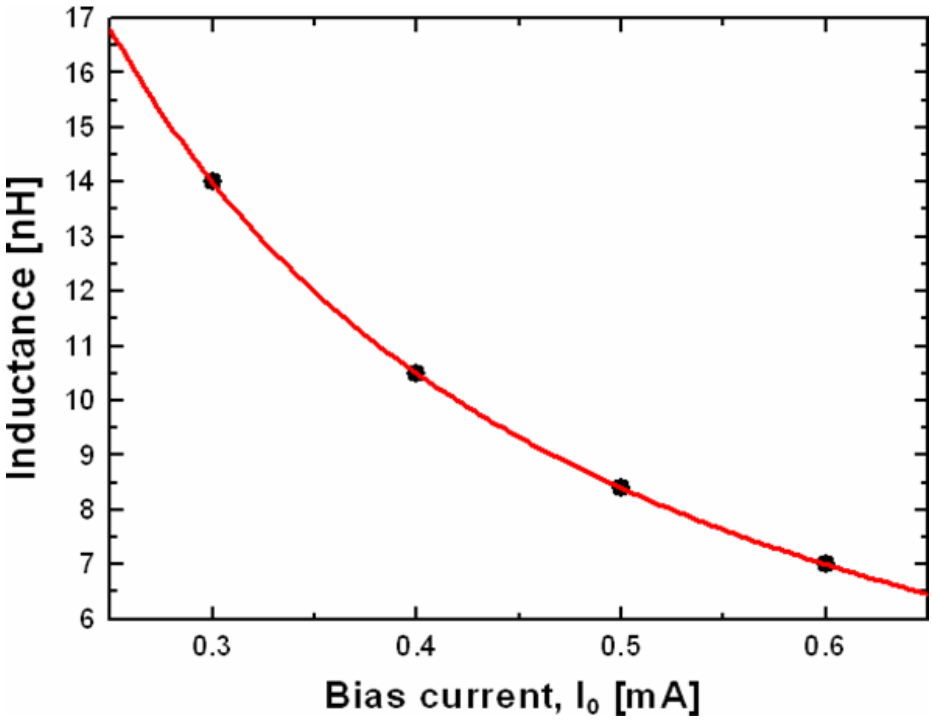


Fig. 19. Inductance values as a function of the bias current of the CMOS-APD.

B. Optical Characteristics of CMOS-APDs

When optical signals are illuminated to the CMOS-APDs, a part of photons pass through the P^+/N-well depletion region and then are absorbed in the charge neutral region or the N-well/P-substrate depletion region due to large optical penetration depth of about 14 ㎛ at 850 nm in Si. The photogenerated holes in the charge neutral region or the N-well/P-substrate depletion region can diffuse into the P^+/N-well depletion region and limit high-speed operation of the CMOS-APD as shown in Fig. 20. Therefore, the dual current source model should be used for the considering both high-speed holes generated in the P^+/N-well depletion region and the low-speed holes generated in charge neutral region or N-well/P-substrate depletion region. The former has the transit time constant only, but the latter has both the transit and diffusion time constant. As explained by chapter Ⅲ, the transit time constant in the P^+/N-well depletion region is about 3 ps and the diffusion time constant is about 160 ps. Hence, the 3-dB bandwidth of high-speed holes and low-speed holes are about 50 GHz and 1 GHz, respectively. When the avalanche occurs, the avalanche build-up time is added as shown in Fig. 21. Therefore the current source ① has the transit time and avalanche build-up time constant. And the current

source ② has the transit time, diffusion time, and avalanche build-up time constant. Table 4 shows extracted parameters of the dual current source model. Because the avalanche build-up time is a few picoseconds and the transit time decreases of about 1.2 ps with the avalanche process, there is not much difference without and with the avalanche process. The f_{3dB} of current source ② decreased at I_0 = 0.4 and 0.5 mA due to the space charge effect [24]. The relative portion of dual current sources is determined by considering current contribution of each photogenerated carriers.

Fig. 22 shows the measured and fitted photodetection frequency response of the CMOS-APD using the dual current source model at four different bias currents, I_0 = 0.01, 0.3, 0.4, and 0.5 mA, under 1 mW optical illumination. This figure clearly shows the occurrence of the rf peaking caused by the inductive component in the avalanche region. In addition, the rf-peaking frequency increases as the bias current increases, and this can be explained by dependence of the inductance value on the bias current. As shown in Fig. 19, the inductance is inversely proportional to the bias current and the rf-peaking frequency is inversely proportional to the square root of the inductance due to the LC resonating condition, consequently the rf-peaking frequency is proportional to the square root of the bias current.

With the help of the rf-peaking effect, the 3-dB bandwidth is increased from 1.03 to 3.83 GHz when the bias current is increased from 0.01 to 0.4 mA.

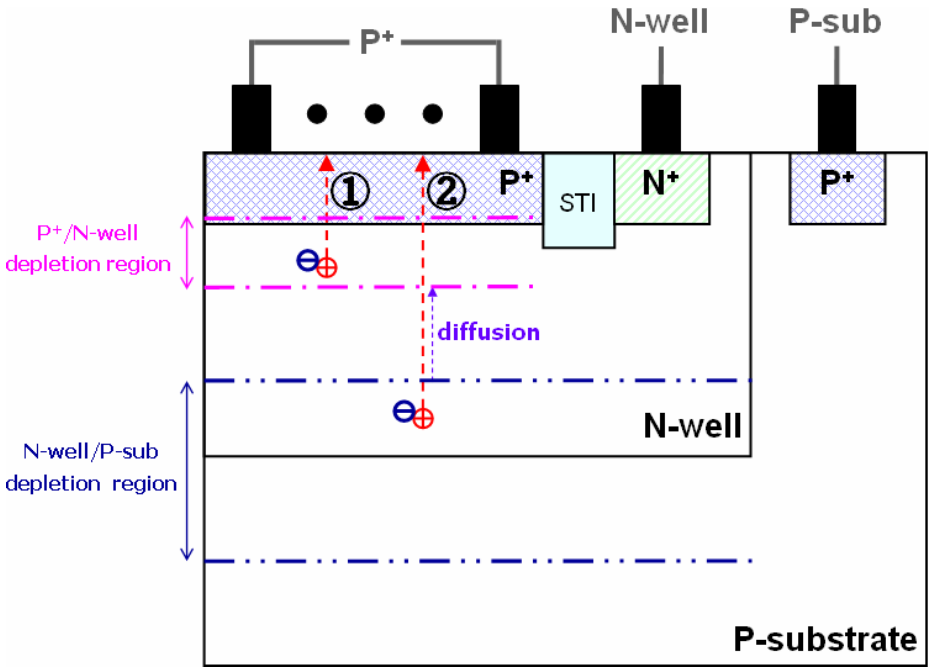


Fig. 20. Dual current sources without the avalanche process.

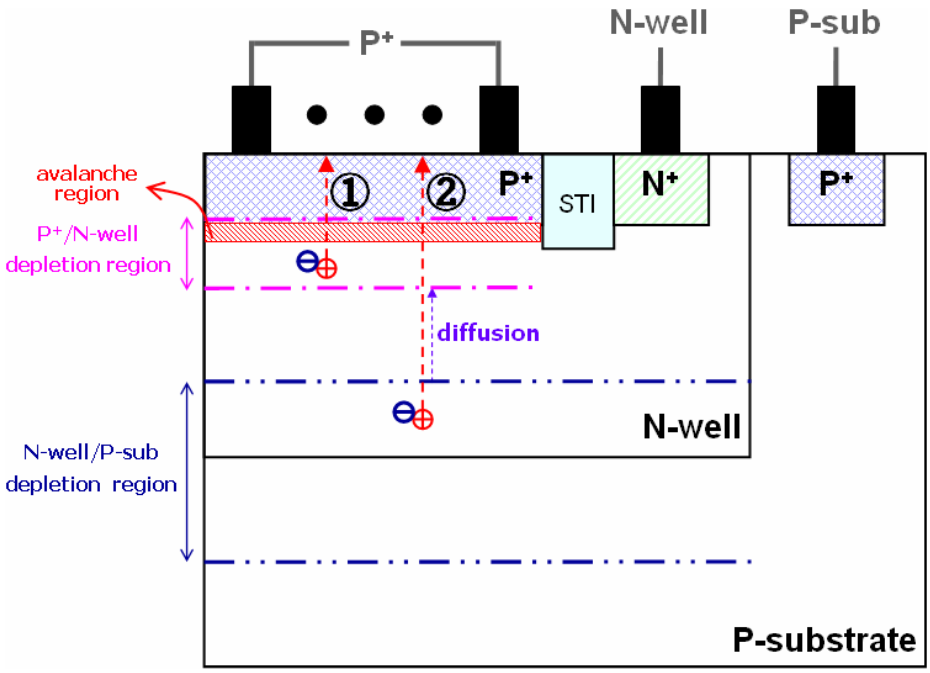


Fig. 21. Dual current sources with the avalanche process.

Table 4. Extracted parameters of the dual current source model.

	0.01 mA	0.3 mA	0.4 mA	0.5 mA
$f_{3dB①}$ [GHz]	51.3	22.7	22.7	22.7
portion of current source ①	0.7	0.01	0.01	0.01
$f_{3dB②}$ [GHz]	1.3	1.2	0.9	0.9
portion of current source ②	0.3	0.99	0.99	0.99

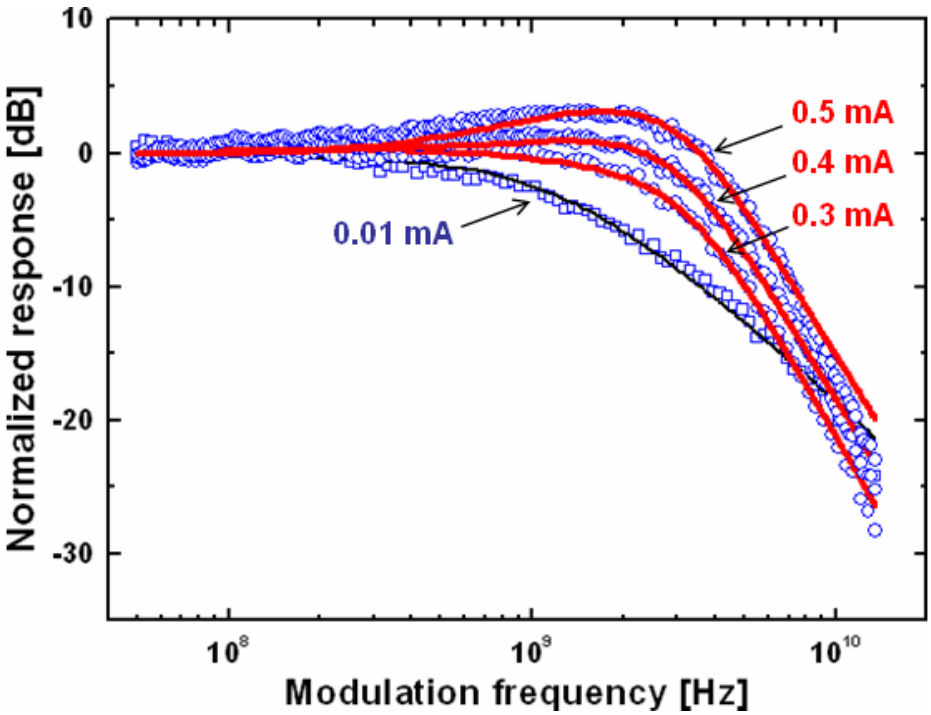


Fig. 22. Measured and fitted photodetection frequency responses of the CMOS-APD. Symbols represent measured data and solid lines indicate modeling results.

Ⅵ. Conclusion

In this thesis, an equivalent circuit model for Si APDs fabricated in 0.18 μm standard CMOS process is developed. The physical origin of rf peaking which enhances the bandwidth in the CMOS-APD is clarified by the inductive component in the avalanche region using the equivalent circuit model.

First of all, CMOS-APDs model based on the physical structure is introduced. The proposed model includes the inductive component for avalanche delay in the avalanche region. Furthermore, the equivalent circuit model is added by dual current sources which contain time delay constants because the photodetection frequency response of the CMOS-APD is limited by not only the RC time and transit time, but also diffusion time constant.

To characterize the fabricated CMOS-APD, I-V characteristics is experimentally studied under dark and illumination conditions. Moreover the photocurrent and avalanche gain are experimentally investigated. Using the equivalent circuit model, the parameter extraction is performed by investigation the impedance characteristics at the different bias conditions. The inductance, which causes the rf-peaking effect, dependence on the bias current is experimentally and

theoretically examined. In addition, the photodetection frequency response is measured and fitted at the different bias conditions and the physical origin of the rf-peaking frequency dependent on the bias current is clarified by the extracted inductance values. With the help of the rf-peaking effect, the 3-dB bandwidth is increased significantly up to 3.83 GHz.

From the results, it is expected that the CMOS-APDs can be utilized for low-cost and large-bandwidth integrated optical receivers with the help of mature CMOS technology and the rf-peaking effect.

Appendixes

A. Extrinsic Components Values of the CMOS-APD

Table 5. Extrinsic components values

of the equivalent circuit model of the CMOS-APD.

	0.01 mA	0.3 mA	0.4 mA	0.5 mA	0.6 mA
R_{well} [Ω]	30	30	30	30	30
C_{sub1} [fF]	300	300	300	300	300
C_{sub2} [fF]	200	200	200	200	200
R_{sub} [Ω]	280	280	280	280	280
R_{p1} [Ω]	10	10	10	10	10
R_{p2} [Ω]	22	22	22	22	22
L_{p1} [nH]	0.1	0.1	0.1	0.1	0.1
L_{p2} [nH]	0.1	0.1	0.1	0.1	0.1
C_p [fF]	210	210	210	210	210

B. Significant Equation Summary of the P-N Junction Diode

The following equations are referred to the [14], [16], [25], and [26].

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2} \right)$$ built-in potential

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D} \right) V_{bi}}$$ depletion width of the step junction P-N diode

$$W = \sqrt{\frac{2\varepsilon_s \left(V_{bi} - V_R \right)}{qN_D}}$$ depletion width for a one-sided abrupt P^+/N-well junction under reverse bias conditions

$$\frac{D_n}{\mu_n} = \frac{kT}{q}$$ Einstein relationship for electrons

$\frac{D_p}{\mu_p} = \frac{kT}{q}$	Einstein relationship for holes
$D_n = \left(\frac{kT}{q}\right)\mu_n$	diffusion coefficient for electrons
$D_p = \left(\frac{kT}{q}\right)\mu_p$	diffusion coefficient for holes
$t_a = \tau\langle M\rangle$	avalanche build-up time
$\tau = N(\beta/\alpha)(x_a/v_s) = Nk\frac{x_a}{v_s}$	mean free time between the ionizing collisions
$k = \beta/\alpha$	ionization coefficient ratio
$t_d = \frac{w}{v_d}$	transit time in the depletion region

$t_D = \frac{4l_D^2}{\pi^2 D}$ diffusion time in the undepleted region

where

k	Boltzmann constant
T	absolute Temperature
q	magnitude of electronic charge
N_A	acceptor-impurity concentration
N_D	donor-impurity concentration
n_i	intrinsic carrier concentration
ε_s	semiconductor permittivity
V_R	reverse bias (voltage)
μ_n	electron mobility
μ_p	hole mobility
M	multiplication factor
$\langle M \rangle$	mean value of multiplication factor
N	constant varying from 1/3 to 2

β	hole ionization coefficient
α	electron ionization coefficient
x_a	width of the avalanche region
v_s	saturation velocity
w	width of depletion region
v_d	drift velocity
l	length of undepleted region
D	diffusion coefficient of Si

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국문요약

CMOS-Compatible Avalanche 광검출기를 위한 등가회로 모델

본 논문에서는 0.18 μm 표준 CMOS 공정에서 제작된 Si avalanche 광검출기의 등가회로 모델을 개발하였다. 이 모델을 사용하여 CMOS-compatible 광검출기 (CMOS-APD)에서 대역폭을 증가시키는 rf-peaking 효과의 물리적 원인을 avalanche 영역의 인덕티브 성분을 통해 명확하게 설명하였다.

우선, 제작된 CMOS-APD의 물리적인 구조에 따른 등가회로 모델을 제안하였다. 제안된 모델은 avalanche 영역에 avalanche 지연에 의한 인덕티브 성분을 포함한다. 더 나아가서, CMOS-APD의 광검출 주파수 응답은 RC time과 transit time 뿐만 아니라 diffusion time에도 제한을 받기 때문에, 정확한 광검출 특성을 설명하기 위해서 dual current source 모델이 추가되었다.

CMOS-APD의 광검출 특성을 밝히기 위해 DC 상태에서 빛의 유무에 따른 전압-전류 관계를 실험적으로 살펴보았고, 그에 따른 광검출 전류와 avalanche 이득을 파악하였다. 제안된 등가회로 모델을 사용하여 바이어스 조건에 따른 임피던스 특

성을 조사하여 파라미터 값들을 추출하였고, rf-peaking 효과의 원인이 되는 인덕턴스가 바이어스 전류에 반비례한다는 것을 실험적, 이론적으로 입증하였다. 또한, 바이어스 조건에 따라 광변조 주파수 응답을 측정하였고, 제안된 등가회로 모델의 결과와 잘 맞는 것을 확인하였다. 바이어스 조건에 따라 결정되는 rf-peaking 주파수의 물리적 원인을 추출된 인덕턴스 값들로써 명확히 규명하였다. Rf-peaking 효과로 3-dB 대역폭이 3.83 GHz까지 증가하는 것을 보였다.

위와 같은 연구 결과를 통해, CMOS-APD가 발달된 CMOS 테크놀로지와 rf-peaking 효과의 도움으로 낮은 제조 가격과 큰 대역폭을 갖는 집적화된 광수신기로 활용될 수 있을 것이라 기대된다.