The Effect of Shallow Trench Isolation on the Performance of Single-Photon Avalanche Diodes in CMOS Technology

Won-Yong Ha

The Graduate School

Yonsei University

Department of Electrical and Electronic Engineering

The Effect of Shallow Trench Isolation on the Performance of Single-Photon Avalanche Diodes in CMOS Technology

A Master's Thesis

Submitted to the Department of Electrical and Electronic Engineering

and the Graduate School of Yonsei University

Won-Yong Ha

December 2021

This certifies that the master's thesis of Won-Yong Ha is approved.

Thesis Supervisor: Prof. Woo-young Choi

Thesis Co-Supervisor: Ph.D. Myung-Jae Lee

Prof. Youngcheol Chae

The Graduate School

Yonsei University

December 2021

Table of Contents

Table of Contents ······ i

List of Figures ······ iv

List of Equations ······ vi

List of Tables ······ vi

Abstract ······ vii

1. Introduction ······ 1

1.1. SPAD ······ 1

1.2. SPADs in CMOS Technology ······ 2

1.3. Motivation ······ 3

1.4. Organization ······ 4

2. Principle ······ 5

2.1. Operating Principle of SPAD 5

2.2. Guard ring 8

2.3. Parameter 12

2.3.1. I-V Characteristics 13

2.3.2. DCR 15

2.3.3. APP 17

2.3.4. PDP 19

3. Simulation and Experiment 21

3.1. TCAD Simulation 22

3.2. Measurements 23

3.2.1. I-V Characteristics 24

3.2.2. LET 26

3.2.3. DCR 28

3.2.4. APP 30

3.2.5. PDP ······ 32

4. The Effect of the STI on the SPAD ······ 35

4.1. Device Structure ······ 36

4.2. TCAD Simulation ······ 38

4.3. Experimental Results and Analysis ······ 42

5. Conclusion ······ 53

Reference ······ 57

Abstract in Korean ······ 61

List of Figures

Fig. 2-1. Basic operation of SPAD. 7
Fig. 2-2. Cross-section of a SPAD with diffused guard ring. 11
Fig. 2-3. Cross-section of a SPAD with STI guard ring. 11
Fig. 2-4. Cross-section of a SPAD with virtual guard ring. 11
Fig. 2-5. I-V characteristic of a SPAD. 14
Fig. 2-6. DCR characteristic of a SPAD. 16
Fig. 2-7. Inter-arrival time histogram of the SPADs. 18
Fig. 2-8. PDP characteristic of a SPAD. 20
Fig. 3-1. Measurement setup for I-V characteristic. 25
Fig. 3-2. Measurement setup of LET. 27
Fig. 3-3. Measurement setup of DCR characteristic. 29
Fig. 3-4. Inter-arrival time histogram of the SPADs. 31
Fig. 3-5. Measurement setup of PDP characteristic. 34
Fig. 4-1. Cross sections of the SPADs: (a) with full STI, (b) without STI, and (c) with partial STI. 37
Fig. 4-2. Current density – voltage characteristics of the SPADs obtained with TCAD simulation: (a) with full STI and (b) without STI, and (c) with partial STI. 39
Fig. 4-3. Electric field profiles of the SPADs obtained with TCADD simulation: (a) with full STI and (b) without STI, and (c) with 40

Fig. 4-4. Electric field vs width for the SPADs obtained with TCAD simulation. 41
Fig. 4-5. . I-V characteristics for SPADs under dark and illumination conditions: (a) with full STI, (b) without STI, and (c) with partial STI 44
Fig. 4-6. Results of light emission tests of SPADs: (a) SPAD before the breakdown voltage (b) SPAD with full STI at V_{EX}= 3V, (c) SPAD without STI at V_{EX}= 3V, and (d) SPAD with partial STI at V_{EX}= 3V. 45
Fig. 4-7. DCR of the SPADs. 48
Fig. 4-8. Energy band diagram of virtual guard ring of SPAD with partial STI. 48
Fig. 4-9. Inter-arrival time histogram of the SPADs: (a) with full STI, (b) without STI, and (c) with partial STI 49
Fig. 4-10. PDP of the SPADs without STI: (a) without STI and (b) with partial STI. ..51
Fig. 4-11. PDP of the CMOS-SPADs in the range of 900nm to 950nm, when V_{EX} is 3V. 52

List of Equations

Equation. 3-1. 30
Equation. 3-2. 32
Equation. 3-3. 32
Equation. 3-4. 33

List of Table

Table. 1. Performance summary and comparison with deep junction CMOS-SPAD. 56

Abstract

The Effect of Shallow Trench Isolation on the Performance of Single-Photon Avalanche Diodes in CMOS Technology

Won-Yong Ha

Dept. of Electrical and Electronic Engineering

The Graduate School, Yonsei University, Seoul, Korea

Single-photon avalanche diode (SPAD) fabricated in complementary metal-oxide-semiconductor (CMOS) technology plays a significant role in various fields such as ranging technologies and the biomedical fields. Although CMOS-SPADs have a great advantage on cost, mass production, and integration with other electronic devices, current CMOS-

SPADs have limitations due to their sensitivity and high noise characteristics. Moreover, many reported SPADs have a shallow junction for multiplication regions that are not suitable for detecting long-wavelength, especially 940 nm where many ranging technologies are of interest.

In this thesis, by comparing the different structures of SPADs, an optimized SPAD's structure is proposed in terms of noise characteristics, such as dark count rate (DCR) and afterpulsing probability (APP), and photon detection probability (PDP) characteristics. Proposed SPAD structures in this thesis are designed to have P-well/Deep N-well multiplication region to increase the PDP in the long-wavelength and fabricated with 110nm CMOS image sensor technology. First, two SPADs are compared in terms of noise characteristics: with and without shallow trench isolation (STI). Through comparison, SPAD without STI showed significantly lower noise characteristics and proved more suitable for SPAD's applications than SPAD with full STI. Secondly, comparing SPAD without STI and SPAD with partial STI in terms of PDP, higher PDP was observed in SPAD with partial STI. When it comes to PDP at 940nm, the PDP of SPAD with partial STI increased by 12% from PDP of SPAD without STI. In addition, SPAD with partial STI showed a little higher but still reasonable noise characteristics which are DCR and APP.

Keywords: Afterpulsing probability (APP), avalanche gain, avalanche photodiode, dark count rate (DCR), guard ring, multiplication, optoelectronics, photon detection probability (PDP), photodetector, photodiode, photogeneration, premature breakdown, shallow trench isolation (STI), single photon avalanche diode (SPAD), standard CMOS technology.

1. Introduction

1.1. SPAD

A single-photon avalanche photodiode (SPAD) is a photodiode design to detect a single photon using avalanche breakdown. It is different from conventional silicon photodiode (PD) in that it operates above the breakdown referred to as the Geiger mode [1]. Therefore, SPAD has a very high gain that allows to detection of a single photon, unlike conventional PD.

Recently, SPAD received many attentions for promising semiconductor devices that can be utilized in a lot of applications from light detection and ranging (LiDAR) to three-dimensional (3D) gesture recognition and face recognition [2], [3]. Moreover, SPADs can be also applied in biomedical imaging such as time-of-flight (ToF) positron emission tomography (PET) and fluorescence correlation spectroscopy (FCS) [4], [5].

1.2. SPADs in CMOS Technology

There two types of SPAD in terms of fabrication: SPADs fabricated in custom process [6], [7] and silicon-based SPADs (CMOS-SPADs) fabricated in standard complementary metal-oxide-semiconductor (CMOS) process [8], [9]. Although custom-made SPAD showed a better photon detection probability (PDP) compared to CMOS-SPADs, there are many advantages of CMOS-SPADs in terms of low manufacture cost and ability to integrate with other electronics on the same chip [10]. Recently, many groups have conducted research to increase PDP and maximum responding wavelength to overcome the limitation of CMOS-SPADs [11]. Moreover, many SPADs have been reported utilizing CMOS image sensor (CIS) technology that provides deeper junctions based on more lightly-doped layers and suitable layers for photodetectors [12], [13].

1.3. Motivation

Although CMOS-SPAD has a high potential for ranging technologies, it needs to acknowledge that CMOS SPAD still has many obstacles to overcome. First, one of the limitations that need to be overcome is high dark noise. The dark noise of CMOS-SPAD consists of tunneling noise, thermal noise, and trap noises [14]. Because CMOS-SPAD operates in a very high electric field, small noise can highly impact the overall performance. Therefore, it is essential to lower the dark noises as much as possible. Secondly, in ranging technologies, high PDP, especially in the near-infrared region, is required. In conventional CMOS-SPAD, the active junction is designed to be near the silicon surface called a shallow junction [15], [16]. For this reason, the PDP of conventional devices was not suitable for ranging technologies. Recently, many of the SPADs with deeper multiplication junctions were reported and the PDP of the region of interest increased. However, still, PDP for the near-infrared region is not sufficient to actualize the ranging technologies.

1.4. Organization

The thesis is organized as follows.

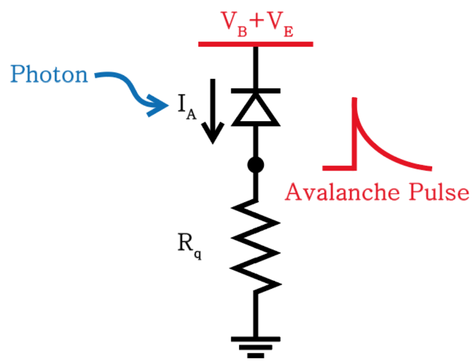
- Chapter 2 presents the various guard rings and SPAD's characteristics.
- Chapter 3 presents SPAD's design and SPAD characterization techniques.
- Chapter 4 presents an optimized SPAD structure in terms of noise and PDP characteristics.
- Chapter 5 summarizes the thesis and concludes the result based on the experiment's results.
- Reference presents the literature I looked up for the thesis.

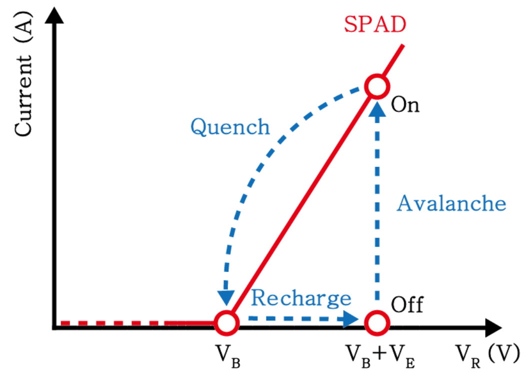
2. Principle

2.1. Operating Principle of SPAD

As shown in Fig. 2-1, the quenching circuit is consisted of SPAD placed in series with a resistor (R_q) greater than 100kΩ [17]. Originally, SPAD is in the open state even though voltage over the breakdown voltage is applied to SPAD. When a photon that has energy over the bandgap of the SPAD's material comes to the device, electron-hole pairs (EHP) are generated. Due to the high electric field of the depletion region, carriers collide with the lattice at a high-speed leading to impact ionization [18]. This process continues sequentially and results in avalanche breakdown which changes the SPAD into short. Because the SPAD and the resistor are connected in series, the voltage applied to the SPAD is divided proportionally into two electrical components. Since the resistor has a high resistance than SPAD, the most of voltage applied to the circuit is distributed to the resistor. As a result, the voltage applied to the SPAD becomes lower than the breakdown voltage and leads the circuit into the original state. Therefore, the current in the circuit stops flowing,

and SPAD is ready to detect another photon. By repeating those stages, SPAD can detect whenever the photon comes to the devices.


V_B+V_E
Photon
I_A
Avalanche Pulse
R_q


Current (A)
SPAD
On
Quench
Avalanche
Recharge
Off
V_B
V_B+V_E
V_R (V)

2.2. Guard ring

It is highly important for CMOS-SPAD to have a uniform electric field in the multiplication region for high performance. However, the electric field across the edges of the multiplication region can lead to premature breakdown [13]. To solve this problem, it is crucial to carefully design a guard ring to prevent premature breakdown. There are three types of guard rings: diffused guard ring, shallow trench isolation (STI) guard ring, merged implant guard ring, and virtual guard ring [11].

First, the diffusion guard ring was introduced by Haitz [19]. It is a guard ring formed by inserting a layer with a low doping concentration around the multiplication region [20]. As shown in Fig. 2-2, P-well is used as the diffused guard ring to prevent premature breakdown from P+/Deep N-well.

However, diffused guard ring has many limitations. First, when diffused guard ring fabricated in the modern CMOS process, high doping concentration and shallow implants cause high tunneling noise, resulting in high DCR [19]. Secondly, the increase of the quasi-neutral region at the edge of the multiplication region leads to late diffusion of minority

carriers coming to the central high-field region. It causes a long diffusing tail which worsens the timing resolution of the SPAD [21]. Lastly, diffused guard ring limits the total diameter of the SPADs because the depletion region of the guard ring merged when the active region is narrowed [22].

Second, the shallow trench isolation (STI) guard ring structure was first proposed by Finkelstein [23]. STI layer is fabricated by inserting SiO_2 into the etched silicon surface to block the surface leakage current. As shown in Fig. 2-3, the STI layer inserted the edge of the P+/N-well multiplication region. Because of its dielectric characteristics, it prevents premature breakdown efficiently. Furthermore, it can fabricate smaller than diffused guard ring when it is inserted around the multiplication region. However, due to the fabrication of STI accompanied etching process, a lot of defects were created resulting in high DCR [24].

Lastly, the virtual guard ring was first introduced by Petrillo [25]. This type of guard ring is formed by implanting a layer that has retrograded deep doping characteristics, resulting in a low doping surface. This characteristic allows preventing premature breakdown when it is inserted around the multiplication region as can be seen in Fig. 2-4.

The virtual guard ring has many advantages compared to the other type of guard rings. First, by removing the quasi-neutral regions around the guard ring, the long tail of minority carrier diffusion caused is reduced, leading to improving timing resolution. Secondly, unlike a diffused guard ring. the SPAD with virtual guard ring is free from depletion region merging when active region diameter is scale downed. Lastly, it tends to have fewer defects than the STI guard ring due to the absence of the etching process in silicon.

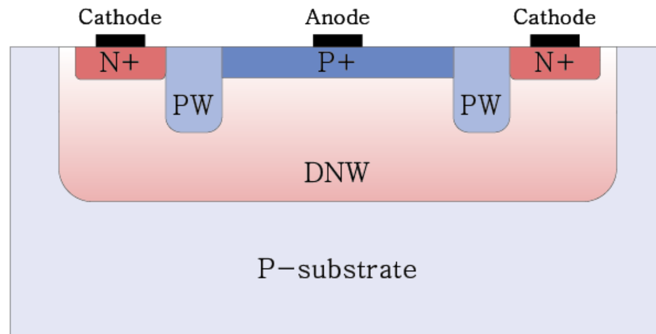


Fig. 2-2. Cross-section of a SPAD with diffused guard ring.

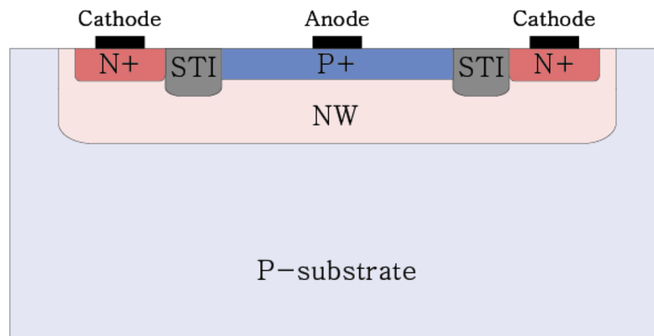


Fig. 2-3. Cross-section of a SPAD with STI guard ring.

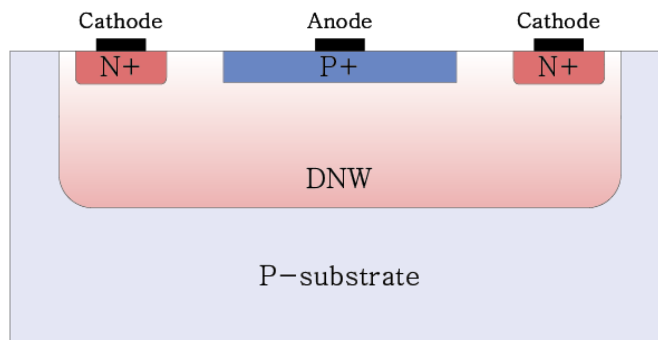


Fig. 2-4. Cross-section of a SPAD with virtual guard ring.

2.3. Parameter

Several factors need to be considered when the characteristics of SPAD are evaluated.

First, the electrical characteristics of the SPAD can be evaluated by current-voltage (I-V) characteristics.

Second, it is important to evaluate SPAD's characteristics in terms of efficiency. For the evaluation, factors such as PDP, dark count rate (DCR), and afterpulse probability (APP) need to be considered.

In this section, various parameters for the evaluation will be discussed.

2.3.1. I-V Characteristics

The SPAD operates in reverse bias and shows different current characteristics below and over the breakdown voltage as shown in Fig. 2-5. In a dark condition, SPAD shows a very low dark current below few pA when a reverse bias is below the breakdown voltage. However, when the device is applied voltage over the breakdown voltage, the current increases dramatically due to impact ionization and multiplication. The current soon saturates due to the space-charge effect and series resistance [26]. A similar phenomenon was observed in an illuminated condition. Below the breakdown voltage, current flows a very low photogenerated current below few nA. As soon as, the reverse bias is over the voltage, the current increases sharply and soon saturates due to the same reason in the dark condition.

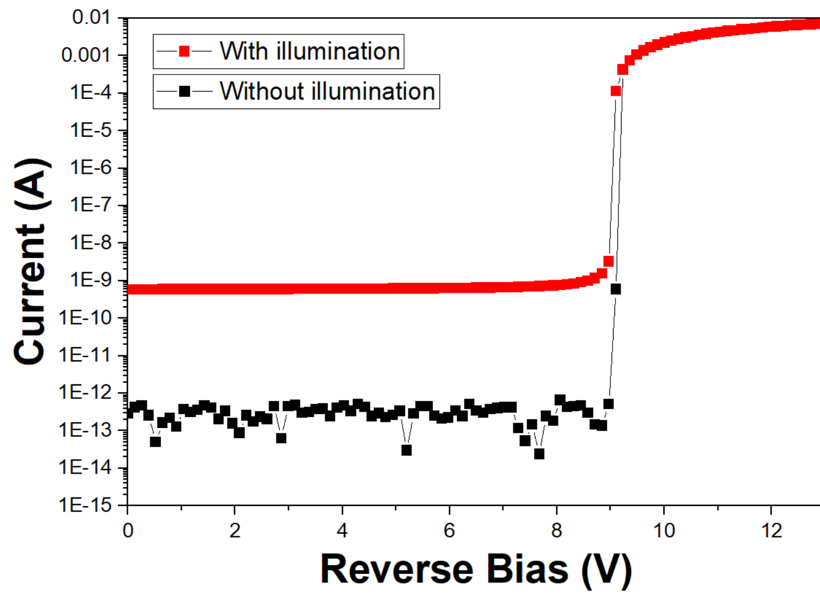


Fig. 2-5. I-V characteristics of a SPAD.

2.3.2. DCR

SPAD needs to produce avalanche current by incident photon. However, some carriers generate avalanche current by other factors and these carriers are called dark count. The number of dark counts per unit time is referred to as DCR.

There are various causes of DCR. First, thermally generated carriers trigger the dark count. Therefore, DCR is proportional to temperature [27]. Second, trapped carriers in the trap state between the bandgap of the material could trigger avalanche breakdown by the acceleration of a high electric field [28]. Lastly, an increase in excess bias increases tunneling noise caused by band-to-band tunneling as can be seen in Fig. 2-6 [29].

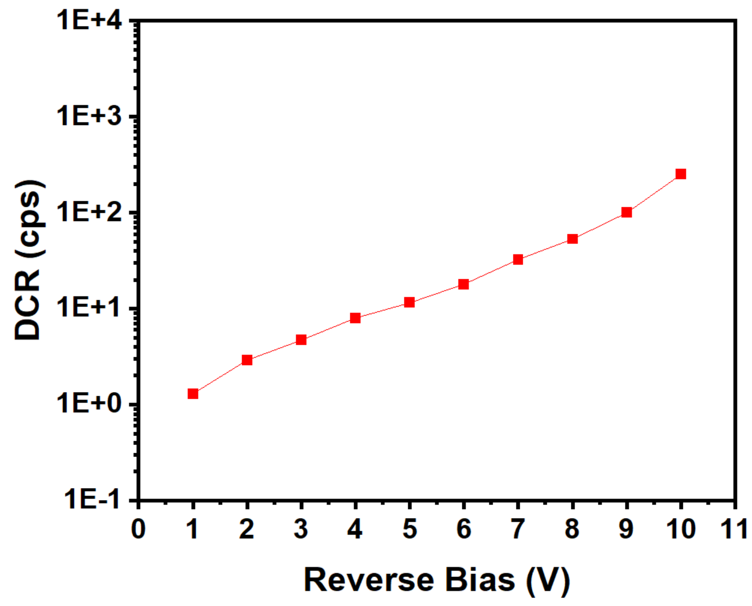


Fig. 2-6. DCR characteristic of a SPAD.

2.3.3. APP

When the carriers trapped in the trap state are released after the avalanche breakdown, the high electric field formed inside of the device accelerates the carriers to retrigger avalanche breakdown which is called afterpulses. Due to the release of the carriers is statistical, afterpulse probability can be evaluated through the time-correlated carrier counting technique [30]. Fig. 2-7 shows the probability density as a function of time for the event of a second pulse after an initial avalanche pulse for a CMOS-SPAD.

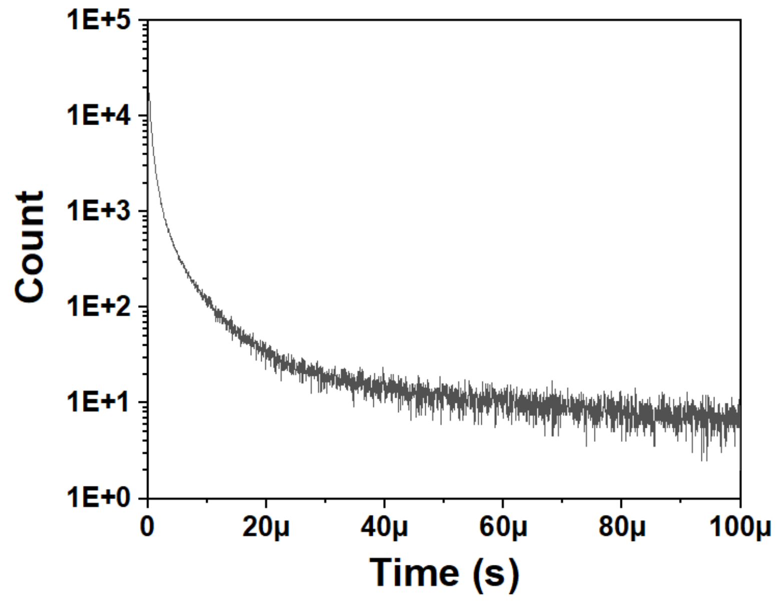


Fig. 2-7. Inter-arrival time histogram of the SPADs.

2.3.4. PDP

For SPAD, it is significant to consider the photons that come in the active region as well as the photons that trigger the avalanche breakdown. PDP refers to the number of photons that trigger an avalanche among the photons that enter the active region.

PDP is depending on two variables: excess bias and wavelength as shown in Fig. 2-8 [30]. When the excess bias increases, the multiplication region of SPAD increases and accelerates carriers faster. This results in increasing avalanche-triggering probability leading to increases in the PDP. Also, it is crucial that photons in a specific wavelength successfully penetrate the device and reach the multiplication region. Therefore, the multiplication region of the SPAD needs to be designed carefully considering the target wavelength due to the depth of the multiplication region highly the wavelength of peak PDP.

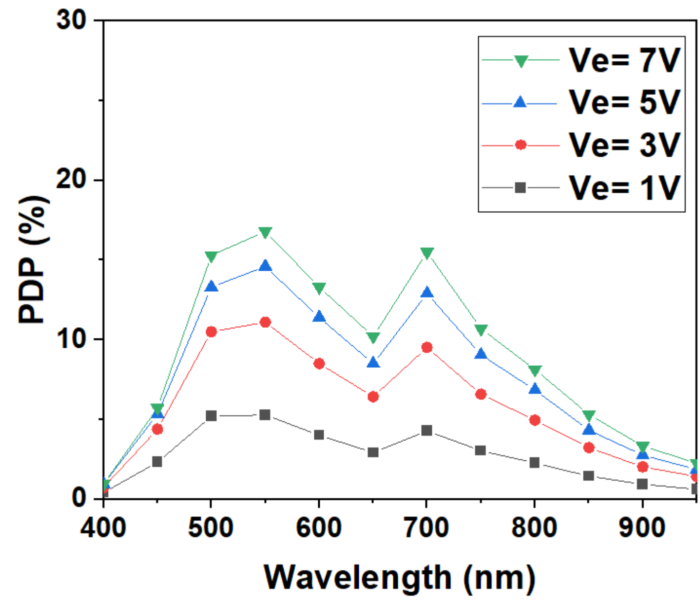


Fig. 2-8. PDP characteristic of a SPAD.

3. Simulation and Experiment

This chapter handles the method of measuring SPAD's characteristics that are used throughout this thesis. The measurement techniques introduced in this chapter are based on the literature and experience cultivated during this thesis work.

First, SPAD's design and foundry process used for the fabrication will be introduced. Second, the actual measurement process will be proposed and investigated. Lastly, detailed information of TCAD simulation used for analyzing SPAD's electrical characteristics will be discussed.

3.1. TCAD Simulation

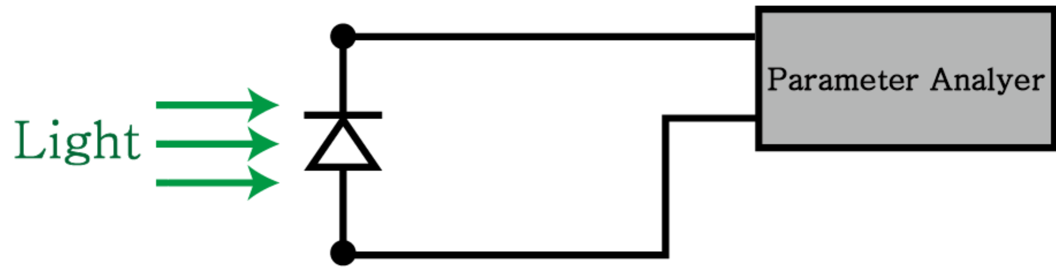
Technology computer-aided design (TCAD) simulation of Synopsys Sentaurus was used for investigating doping profile and electric field profile. The simulations used the doping profile of SPAD provided by Dongbu Hitek. In this simulation, generation and recombination are important phenomena in avalanche breakdown simulation, Shockley-Read-Hall, Okuto avalanche, Auger recombination, band-to-band tunneling, breakdown probability, and optical generation models were utilized in the SPAD simulation.

3.2. Measurements

SPAD's electrical characteristics can be evaluated in three parts: the current response of SPAD due to the reverse bias voltage by I-V characteristics and light emission test (LET), the noise characteristics via DCR and APP, and the performance of SPAD through PDP.

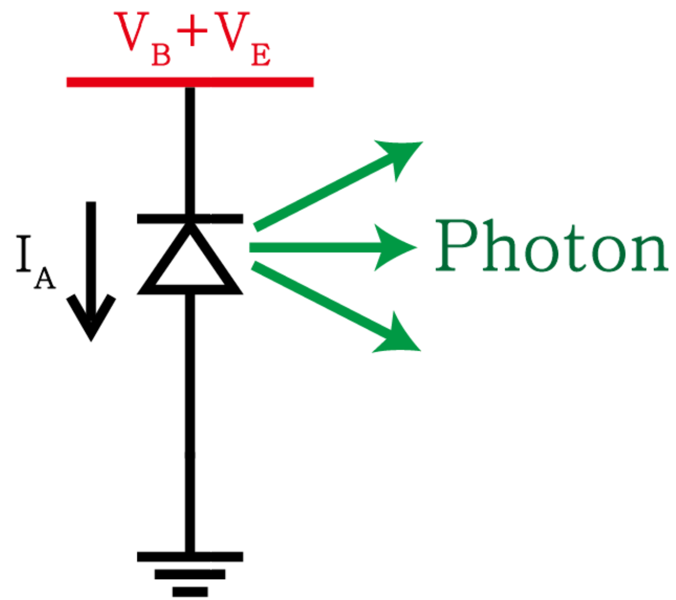
3.2.1. I–V Characteristics

I-V measurement is conducted in two conditions: without illumination and with illumination. In both conditions, the same measurement method is used. As shown in Fig. 3-2, the I-V characteristic is evaluated by applying a reverse bias to the SPAD and measuring the following current through the diode. The Keysight B1500A parameter analyzer was used for the measurement of I-V characteristics.


Light
Parameter Analyer

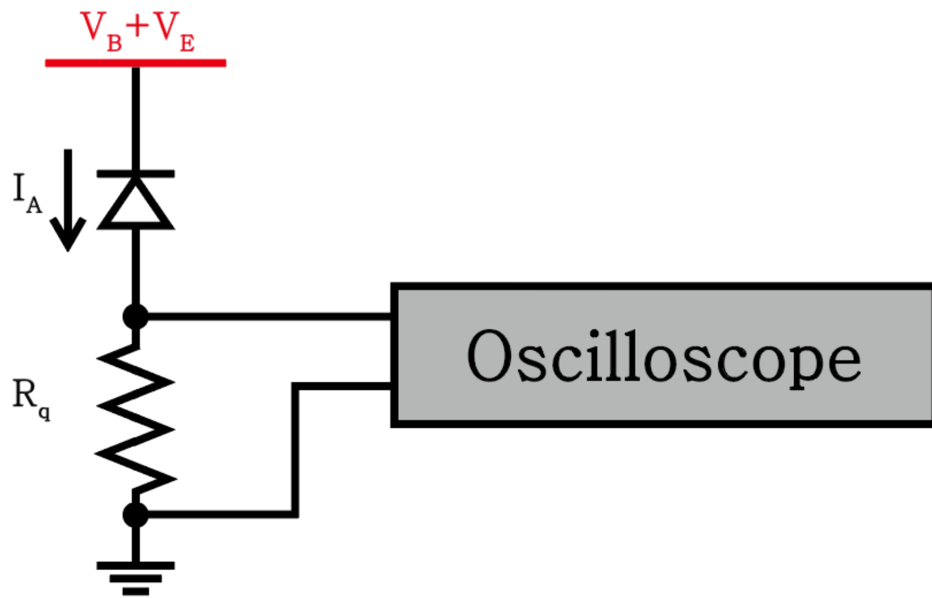
3.2.2. LET

In LET measurement, the SPAD is applied reverse bias without quenching resistor to persist avalanche breakdown as shown in Fig. 3-3. The silicon emits a small portion of photons during recombination, although silicon has an indirect bandgap [31]. Using this characteristic, the diode starts to emit light from the breakdown voltage. The area that emits light indicates the place where undergoes the avalanche breakdown. From this experiment, we can decide whether the avalanche breakdown occurs in the active region or not.


$V_B + V_E$
I_A
Photon

3.2.3. DCR

As shown in Fig. 3-4, oscilloscope and passive quenching circuit that consists of 100 kΩ as quenching resistor (R_q) and SPAD is used for a DCR measurement. In a completely dark environment, SPAD is applied bias that is higher than the breakdown voltage. Due to the various noise component of the device, avalanche current is generated and flow through the circuit. It triggers to raise the voltage across the R_q and quenched to make the circuit into the original state [17]. Through this process, DCR is measured as the number of these pulses per 1 second by using an oscilloscope



V_B+V_E
I_A
R_q
Oscilloscope

3.2.4. APP

APP is calculated by using an inter-avalanche time histogram and passive quenching circuit in the complete dark condition. The histogram is built using the time interval measured between two consecutive avalanche pulses. If DCR consists of only primary pulses, the primary pulses will show in an exponential distribution due to the Poissonian nature. However, if secondary pulses exist, the histogram will show a multi-exponential characteristic. As the trapped carrier lifetime ranges from a few nanoseconds to microseconds, it can be safely assumed that exponential distribution after 20 μs indicates the primary pulse. When an exponential curve fits the data points of the histogram where it is measured above 20 μs, the primary pulse can be represented by the area under the fitted exponential curve. The area subtracted from the area of total measured avalanche pulses to the area of a primary pulse represents the secondary pulse. APP can be calculated using Equation 3-1 [17].

$$APP = \frac{Area\ of\ secondary\ pulse}{Area\ of\ total\ measured\ avlanche\ pulses} \tag{3-1}$$

Since there are no avalanche pulses during the dead time, the area until the dead time is neglected at the calculation.

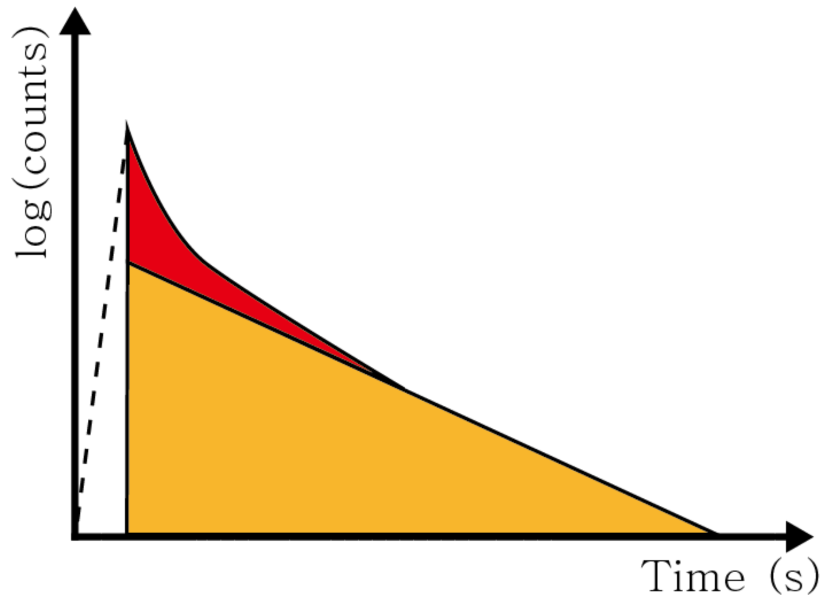


Fig. 3-4. Inter-arrival time histogram of the SPADs.

3.2.5. PDP

PDP is calculated by comparing the reference photodiode's sensitivity and that of a SPAD. The measurement of PDP is conducted as depicted in Fig. 3-6. In the measurement, a monochromator is utilized to select and illuminate a specific wavelength to an optical sphere from a lamp emitting a wide range of wavelengths. Through the optical sphere, the reference photodiode and SPAD are illuminated at the same light intensity. Using optical current flowed through reference photodiode and known its responsivity at different wavelengths, the optical power of light illuminated to the reference photodiode and SPAD can be calculated. Using optical power, the number of incident photons on the reference photodiode ($M_{REF}(\lambda)$) was calculated by following equation 3-2.

$$M_{REF}(\lambda) = Optical\ power \cdot \frac{\lambda}{h \cdot c} \tag{3-2}$$

Since the active area of SPAD and reference photodiode is different, normalization is required as shown in equation 3-3.

$$M_{SPAD}(\lambda) = M_{REF}(\lambda) \cdot \frac{AA_{SPAD}}{AA_{Ref}} \tag{3-3}$$

where $M_{SPAD}(\lambda)$ is the number of an incident of photons on the SPAD, AA_{SPAD} is the active area of SPAD, and AA_{Ref} is the active area of reference photodiode.

For each wavelength, $M_{SPAD}(\lambda)$ is measured and photon detected by SPAD is calculated by subtracting SPAD output pulse rate from its DCR. PDP was calculated as photon detected by SPAD over $M_{SPAD}(\lambda)$ as shown in equation 3-4 [17].

$$PDP(\lambda) = \frac{SPAD\ output\ pulse\ rate - DCR}{M_{SPAD}(\lambda)} \qquad (3\text{-}4)$$

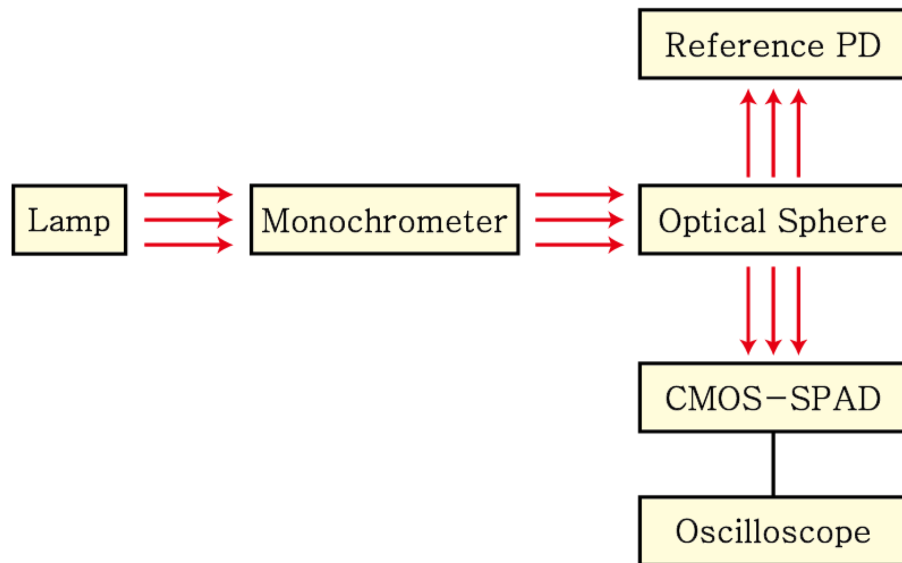


Fig. 3-5. Measurement setup of PDP characteristics.

4. The effect of the STI on the SPAD

In SPADs, the noise plays an important role in determining the device PDP and timing performance. Also, PDP is the important parameter that indicates the sensitivity of the SPAD. Therefore, SPAD should be carefully designed to lower the noise and higher the PDP. This chapter focuses on the effect of the STI in terms of noise and PDP. I designed three CMOS-SPADs fabricated in 110nm CIS technology: with full STI, without STI, and with partial STI to find the optimized SPAD structure in terms of noise characteristics and PDP. Through the comparison, the effect of STI in deep junction SPAD will be investigated in terms of TCAD simulation, I-V, LET, DCR, APP, and PDP characteristics. From these investigations, the optimized structure for SPAD will be clarified.

4.1. Device Structure

As shown in Fig. 4-1, all SPADs have the same deep multiplication region with P-well/Deep N-well to achieve a high PDP at a long wavelength region. Also, SPADs have the same virtual guard ring to prevent premature breakdown. All devices are reverse biased by applying a positive bias to the N+ and putting ground on P+ and substrate. The difference is one SPAD exists fully covered STI on the virtual guard ring as shown in Fig. 4-1(a), another SPAD without STI as shown in Fig. 4-1(b), and the other SPAD with partial STI as shown in Fig. 4-1(c). For all SPADs, the active area diameter is 10 μm and the guard ring width is 2 μm.

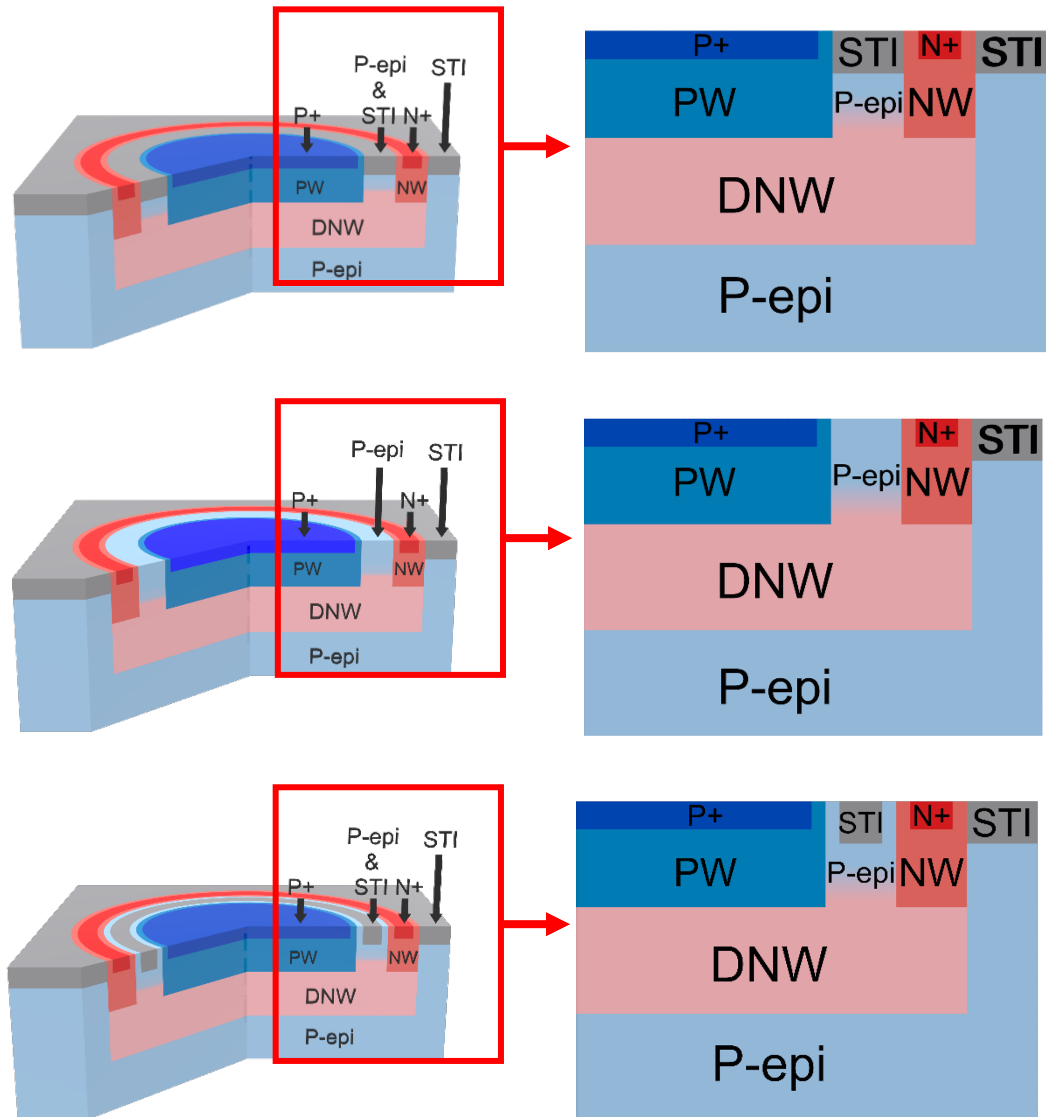


Fig. 4-1. Cross-sections of the SPADs: (a) with full STI, (b) without STI, and (c) with partial STI.

4.2. TCAD Simulation

TCAD simulation was performed to investigate the electric field profile of CMOS-SPADs in reverse bias. Through the comparison of the simulation results, there was not any difference in leakage current as can be seen in Fig. 4-2. As shown in Fig. 4-3, electric field uniformly formed in multiplication region in all CMOS-SPADs without premature breakdown. The results implied that the premature breakdown is effectively prevented through the guard ring in both devices. When the electric field at multiplication junction was observed according to the width of the SPADs, the SPAD with partial STI and with full STI showed a larger active area than SPAD without STI as can be seen in Fig. 4-4. This is due to the low doped virtual guard ring created by STI. When the Deep N-well is doped, STI blocks some of the doping. Due to this fact, a lower doped virtual guard ring is formed compared to its SPAD without STI. Due to the low doped guard ring, the P-well can diffuse more than the SPAD without STI. Therefore, SPAD with partial STI and full STI has a larger multiplication region than SPAD without STI. In addition, the more STI covered the virtual guard ring, the P-well tends to extend more as depicted in Fig. 4-4.

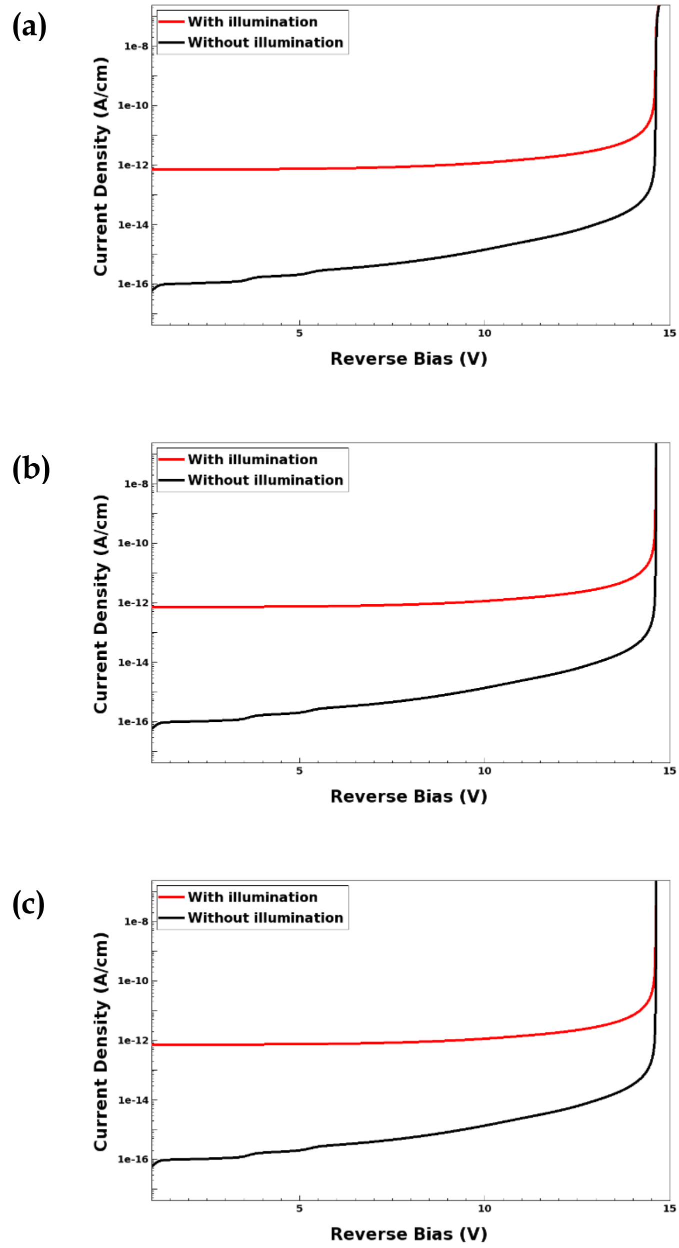


Fig. 4-2. Current density vs voltage characteristics of SPADs obtained with TCAD simulations: (a) with full STI, (b) without STI, and (c) with partial STI

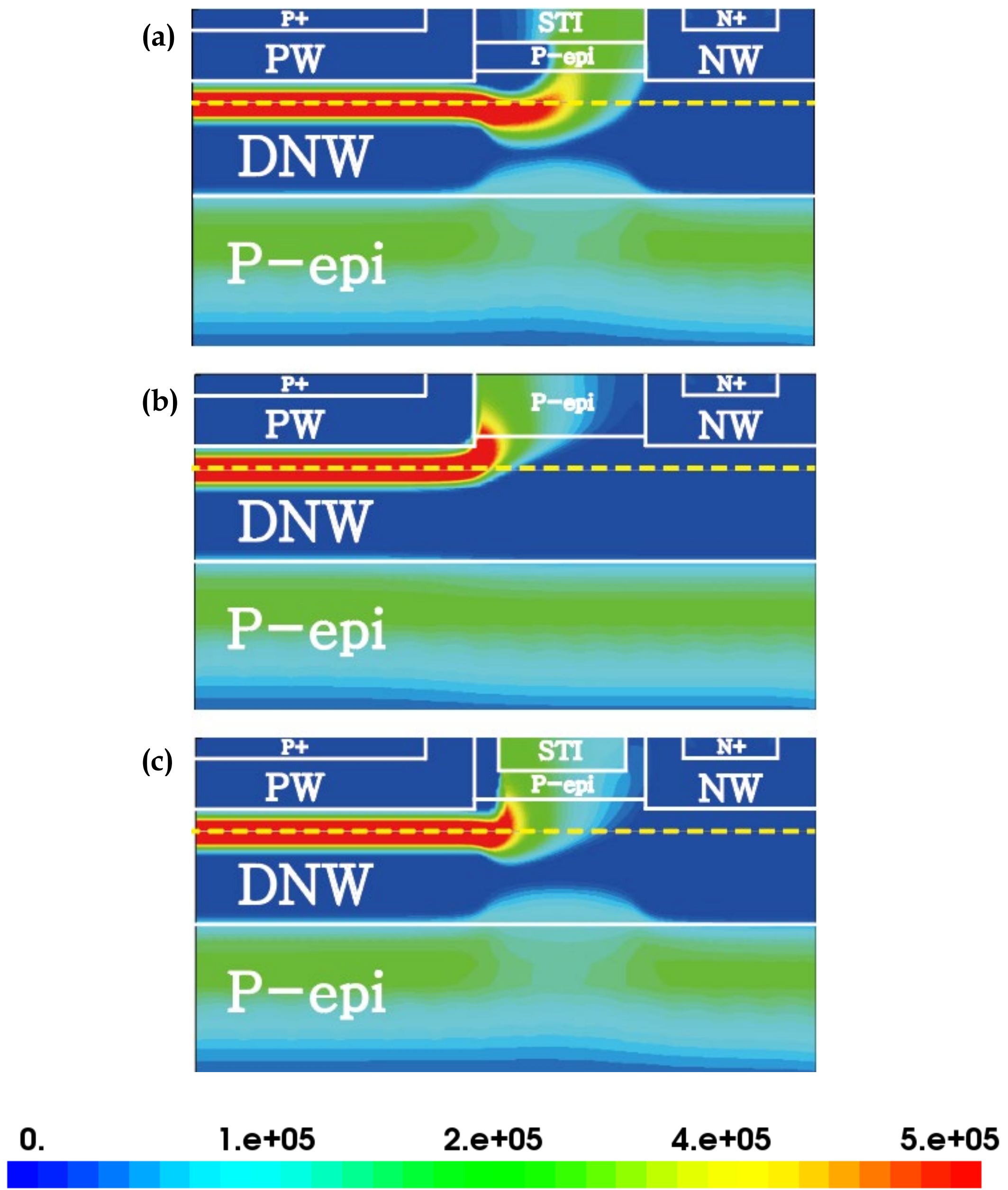


Fig. 4-3. Electric-field profiles of the SPADs obtained with TCAD simulations: (a) with full STI, (b) without STI, and (c) with partial STI

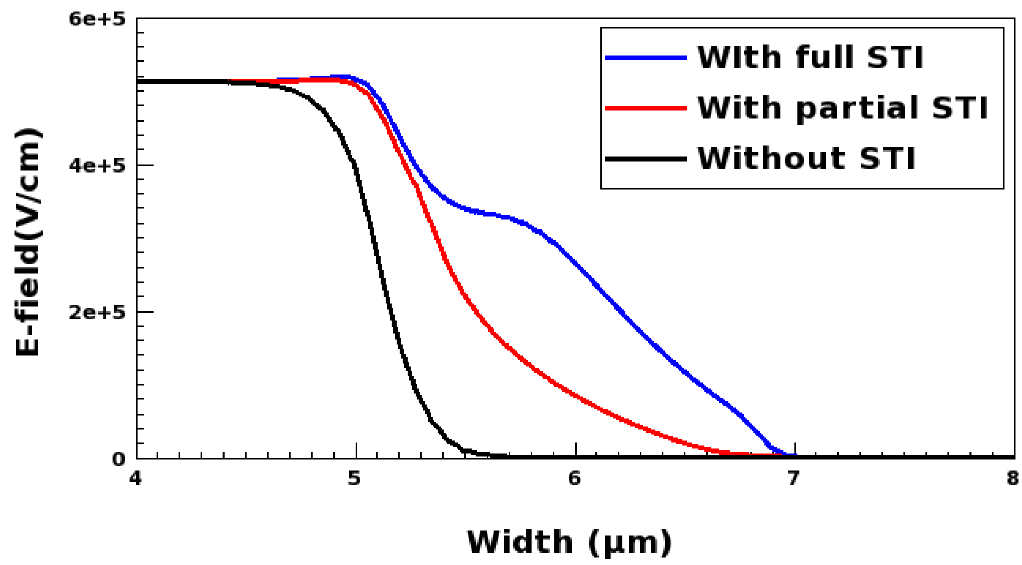


Fig. 4-4. Electric field vs width for the SPADs obtained with TCAD simulation.

4.3. Experimental Results

I-V characteristics of the SPADs were measured in two conditions: without illumination and with illumination. Devices were reverse biased, and currents were measured from an anode which is a P+ port. When the reverse bias is under the breakdown voltage, all SPADs exhibit a low dark current of about 2 pA and a low photogenerated current of about 3 nA as shown in Fig. 4-5. With the reverse bias near and over breakdown voltage, dark and photocurrent increased dramatically due to multiplication and eventually saturated because of the series resistance and the space-charge effect [26]. As expected through the TCAD simulation, I-V characteristics showed no difference in terms of leakage current. In addition, the avalanche breakdown of CMOS-SPADs is identical to 14V due to the same multiplication junction.

Fig. 4-6(a) shows the SPAD when the voltage is not applied over the breakdown voltage. As shown in Fig. 4-6(b), Fig. 4-6(c), and Fig. 4-6(d), regardless of the STI, the active area of SPADs shows a circle emitting light. This indicates the region where avalanche breakdown was occurred and eventually implies that the SPAD was not having any premature breakdown. The difference was that SPAD with partial STI and with full STI

showed a circle that has 0.6 μm larger diameter and 0.8 μm larger diameter respectively than SPAD without STI. This implies that SPAD with STI has a larger active region than SPAD without STI as supported by the electric profile simulated through TCAD simulation.

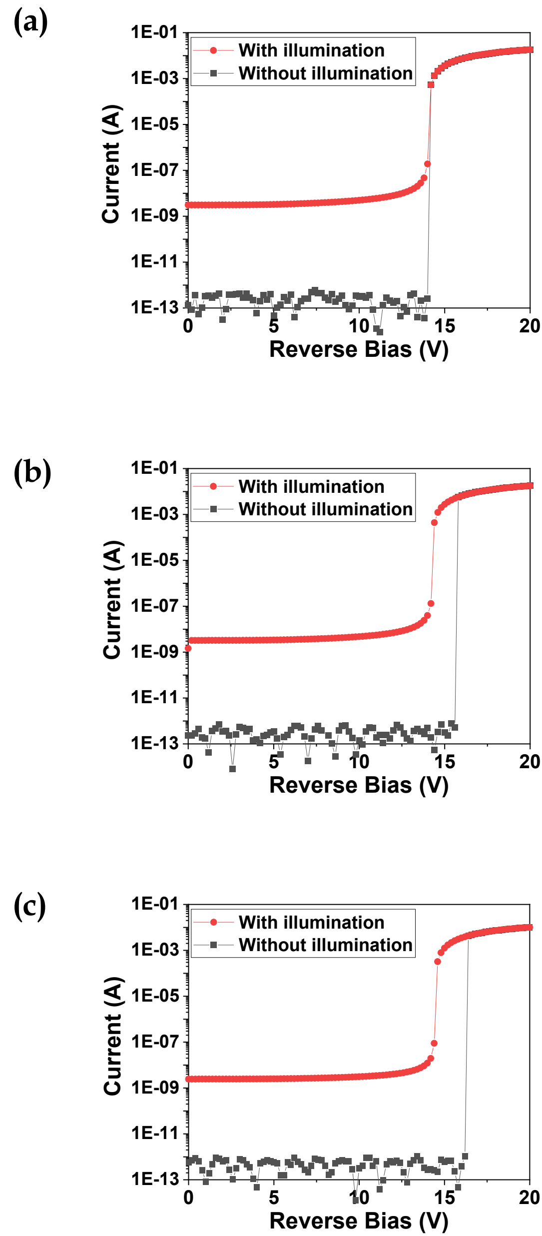


Fig. 4-5. I-V characteristics for SPADs under dark and illumination conditions: (a) with full STI and (b) without STI.

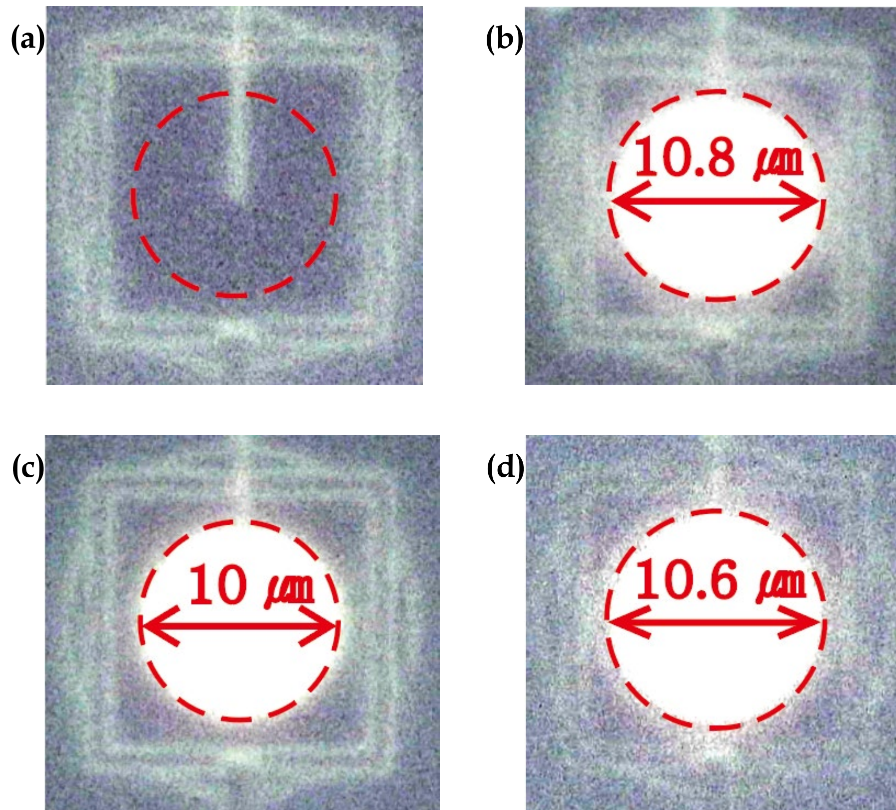


Fig. 4-6. Results of light emission tests of SPADs: (a) SPAD before the breakdown voltage, (b) SPAD with full STI at V_{EX}= 3V, (c) SPAD without STI at V_{EX}= 3V, and (d) SPAD with partial STI at V_{EX}= 3V.

DCR was measured at 0.5V intervals from 0.5V to 3V where the quenching resistor was 100 kΩ. CMOS-SPAD with full STI showed a very high DCR. However, DCR of CMOS-SPAD without STI showed a lower DCR that is less than three orders of magnitude as shown in Fig. 4-7. This result indicated that STI is the main cause of the high DCR due to defects created during its fabrication. When it comes to the DCR of SPAD with partial STI, it has a higher DCR than that of the SPAD without STI. However, it shows not much big difference with the comparison. This is because the P-epi surrounding STI operates as the passivation. As the PW has higher conduction energy than P-epi's, the electrons need to overcome the energy barrier as shown in Fig. 4-8. The energy barrier obstructs trapped carriers caused by defects created during STI fabrication coming to the multiplication region. Therefore, P-epi surrounding STI allowed SPAD with partial STI to have low DCR despite STI existing in the virtual guard ring. In addition, DCR increased accordingly to the excess bias. This showed that excess bias increased tunneling noise and resulted in high DCR.

As the DCR of SPAD with full STI was so high when excess bias was 3V, APP at 3V could not be measured. Therefore, APP was calculated and compared when excess bias voltage was 1 V by using the interval-time histogram and the ideal line as shown in Fig. 4-

9. In addition, it was calculated when the dead time was 100ns and the quenching resistor was 15 kΩ. SPAD with full STI has a very high APP of 92%, and SPAD without STI and SPAD with partial STI showed a very negligible APP value. This indicates that defects caused by the etching process to create full STI trap the carrier and high impact on APP. Moreover, p-epi that surround the partial STI operates as the passivation to block the trapped carriers. Therefore, these results explain why the APP of SPAD with full STI is very high and the others have a negligible APP which also coincides with results of DCR. As a result, eliminating full STI in the SPAD can optimize noise characteristics. Also, there was no influential performance degradation on SPAD in terms of noise characteristics even partial STI is inserted in the virtual guard ring.

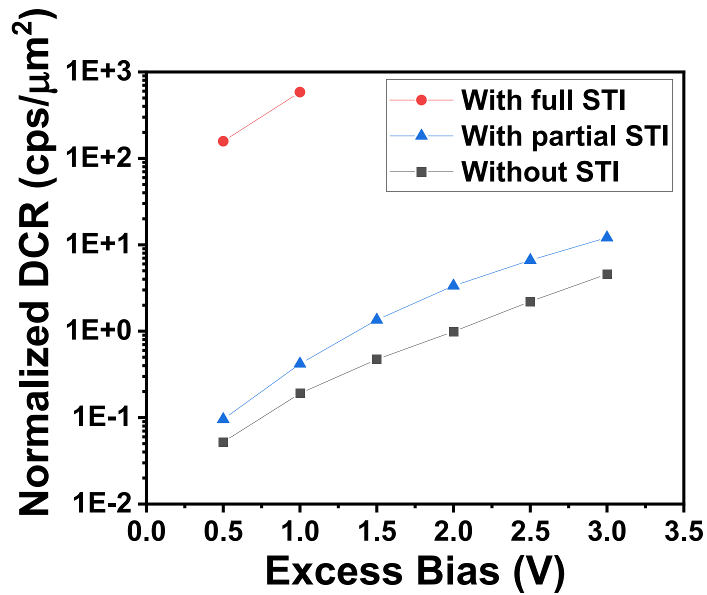


Fig. 4-7. DCR of the SPADs.

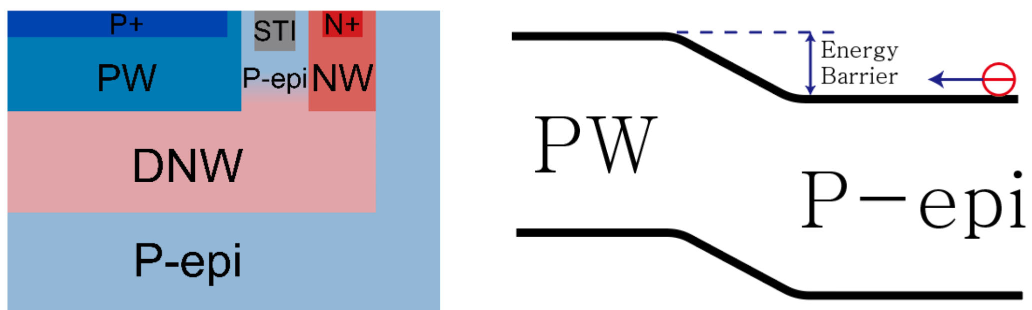
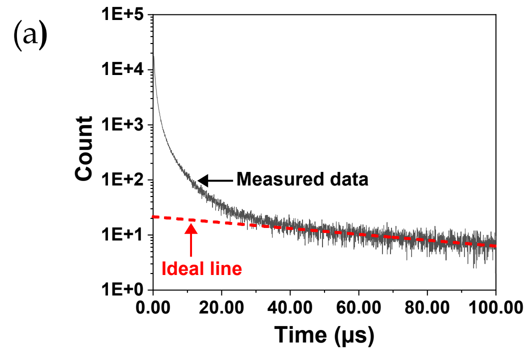
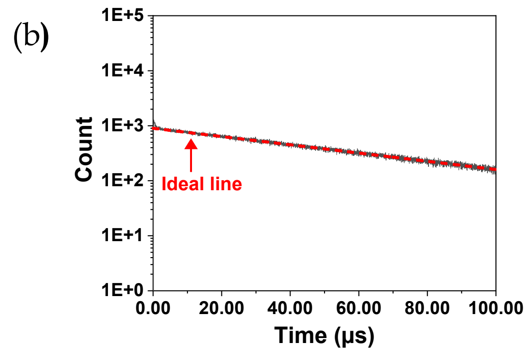


Fig. 4-8. Energy band diagram of virtual guard ring of SPAD with partial STI.





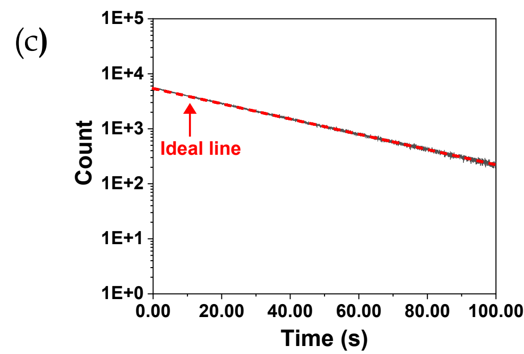
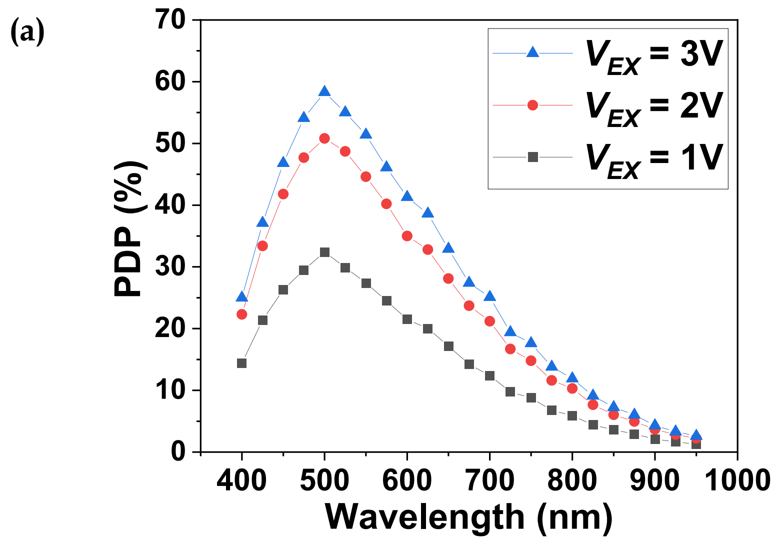


Fig. 4-9 Inter-arrival time histogram of the SPADs: (a) with full STI, (b) without STI, and (c) with partial STI.

Due to the high noise of SPAD with full STI, the PDP of the device could not be measured. However, as the SPAD without STI has a low noise characteristic, PDP could be calculated. As shown in Fig. 4-10(a), the peak PDP of the device is 58.3% at 500nm and PDP at 940nm where the ranging technologies are interested in is 3% when excess bias is 3V. PDP of SPAD with partial STI was also calculated due to the low noise characteristics. As depicted in Fig. 4-10(b), the device has a peak PDP of 63.3% at 500nm and PDP at 940nm of 3.38%. Therefore, there was a 5% increase at peak PDP which is a meaningful difference. Furthermore, PDP of SPAD with partial STI increased 12% of PDP of SPAD without STI at 940nm as can be seen in Fig. 5-9. The reason that SPAD with partial STI has a higher PDP than SPAD without STI is partial STI allows SPAD to have a larger multiplication region due to the low doped virtual guard ring, SPAD with partial STI has a higher PDP.

(a)



(b)

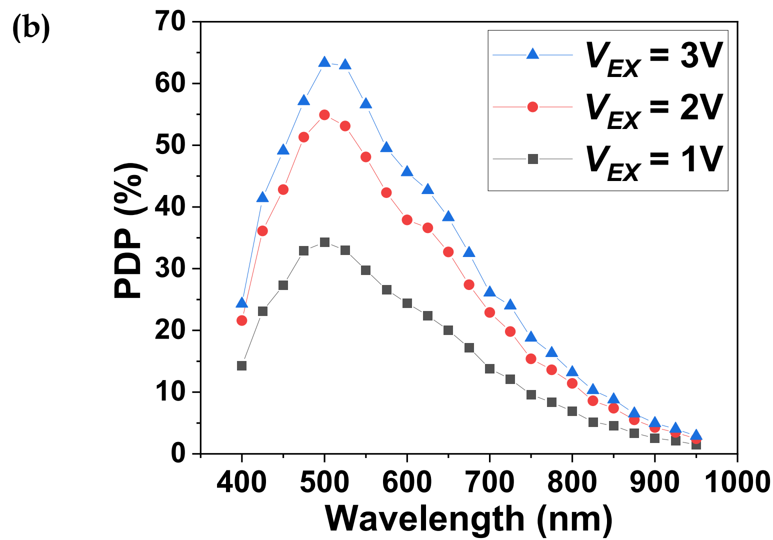


Fig. 4-10. PDP of the SPADs: (a) without STI and (b) with partial STI.

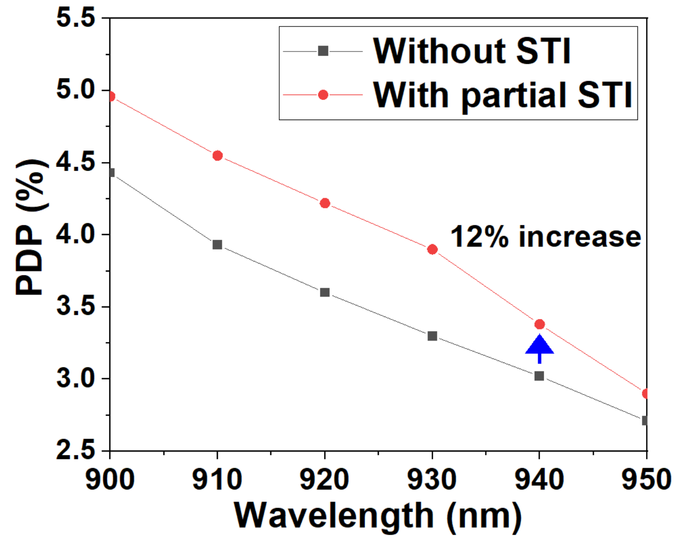


Fig. 4-11. PDP of the CMOS-SPADs in the range of 900nm to 950nm, when V_{EX} is 3 V.

5. Conclusion

The SPAD fabricated in the standard CMOS technology has been researched actively because of cost and integration with other electronic devices in the same chip. However, CMOS-SPADs showed poor PDP and high noise compared to SPADs that are fabricated in a custom process.

In this thesis, I designed and compared three SPADs that have the same P-well/Deep-N-well multiplication junction but have a difference on the top of the virtual guard ring: with full STI, without STI, and with partial STI.

I compared SPADs with full STI, without STI, and with partial STI in various characteristics. Through comparison, there were notable differences in DCR and APP. DCR of SPAD with full STI showed higher than three orders of magnitude compared to its of SPAD without STI and with partial STI. Moreover, SPAD with full STI showed a very high APP of 92% but SPAD without STI showed negligible APP when the excess bias is 1V. This is because of defects created at a silicon surface during the fabrication of STI. When the SPADs without STI and with partial STI are compared in terms of DCR and APP, SPAD with partial STI showed a little higher value than SPAD without STI due to the

defect caused by STI. However, the difference was small and still can be applied to the ranging technologies. This is because the P-epi surrounding the STI created an energy barrier that blocks trapped carriers come into the multiplication region. The active area of SPAD with full STI and with partial STI showed a larger area than that of SPAD without STI through LET and TCAD simulation. The reason is that the partial STI blocked DNW doping and created a lower doped virtual guard ring compared to the SPAD without STI. This low doped virtual guard ring allows the P-well to diffuse more than the P-well of SPAD without STI. Therefore, SPAD with full STI and with partial STI has the larger active area. When it comes to PDP, SPAD with partial STI has 5% more peak PDP than that of SPAD without STI. Moreover, PDP of SPAD with partial STI increased 12% of PDP of SPAD without STI at 940nm. The PDP results are due to the larger active area.

In conclusion, I investigated 3 different SPADs: with full STI, without STI, and with partial STI. Through the comparison of various parameters, SPAD with partial STI showed the highest PDP with an acceptable DCR. It might seem that the enhancement of PDP is not advantageous due to the increase of DCR. However, the SPAD for ranging technologies is utilized where ambient light exists. Due to the ambient light, the DCR of the SPAD tends to increase by about tens of thousands. Therefore, the increase of DCR in a dark condition

of about 100 cps is negligible and enhancement of PDP is a much more crucial matter. When it was compared to the recently reported SPADs as shown in Table 1, the proposed SPAD has a higher PDP than [32] and [33]. When it comes to the comparison with [12], the proposed SPAD has almost the same PDP but a higher DCR. However, as mentioned earlier, when it applied to the applications for ranging technologies, the DCR increased tens of thousands due to the ambient light. Therefore, the difference of DCR between the proposed SPAD and [12] is negligible. Moreover, the operation voltage of the proposed SPAD is lower than that of [12]. This gives a huge advantage to the mobile application where low power consumption is required. In conclusion, the proposed SPAD shows a sufficiently high PDP, low noise characteristics, and low operation voltage which is favorable for mobile applications.

	Proposed SPAD	[32]	[33]	[12]
Technology	**110nm CIS**	**110nm CIS**	**110nm CIS**	**110nm CIS**
Junction	**PW/DNW**	**PW/DNW**	**PW/DNW**	**HVPW/DNW**
Guard Ring	**Virtual GR**	**Virtual GR**	**Virtual GR**	**Poly GR**
STI Location	**Partial STI at the top of the GR**	**Full STI at the top of the GR**	**Between GR and cathode**	**Between GR and cathode**
Active Area	**78.5 μm^2**	**19.6 μm^2**	**50 μm^2**	**78 μm^2**
V_{BD}	**14 V**	**15 V**	**14.4 V**	**18 V**
V_{EX}	**3V**	**2 V**	**1.4 V**	**3 V**
Normalized DCR @ V_{EX}	**6.11 cps/μm^2 @ 3V**	**41.1 cps/μm^2 @ 2V**	**2 cps/μm^2 @ 1.4V**	**0.4 cps/μm^2 @ 3V**
PDP Peak	**63.3% @ 500 nm**	**50.7% @ 540 nm**	**28% @ 500 nm**	**64% @ 500 nm**
PDP @ 940nm	**3.38%**	**1.2%**	**1.64%**	**-**
APP @ V_{EX}, Dead Time	**5.8% @ 3V, 100-ns**	**-**	**0.02% @ 1V, 100-ns**	**0.5% @ 3V, 5-us**

Table 1. Performance Summary and Comparison with Deep Junction CMOS-SPAD

References

[1] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Applied Optics*, vol. 35, no. 12, pp. 1956-1976, 1996.

[2] F. Zappa and A. Tosi, "MiSPIA: microelectronic single-photon 3D imaging arrays for low-light high-speed safety and security applications," in *Advanced Photon Counting Techniques VII*, 2013, pp. 87270L-1-87270L-11.

[3] M. J. Lee and E. Charbon, "Progress in single-photon avalanche diode image sensors in standard CMOS: From two-dimensional monolithic to three-dimensional-stacked technology," *Japanese Journal of Applied Physics*, vol. 57, no. 10, pp. 1–6, 2018.

[4] S. Mandai, M. W. Fishburn, Y. Maruyama, and E. Charbon, "A wide spectral range single-photon avalanche diode fabricated in an advanced 180 nm CMOS technology," *Optics Express*, vol. 20, no. 6, pp. 5849–5857, 2012.

[5] C. Veerappan and E. Charbon, "A substrate isolated CMOS SPAD enabling wide spectral response and low electrical crosstalk," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 6, pp. 299–305, 2014.

[6] J. M. Lee, S. H. Cho, and W. Y. Choi, "An equivalent circuit model for a Ge waveguide photodetector on Si," *IEEE Photonics Technology Letters*, vol. 28, no. 21, pp. 2435–2438, 2016.

[7] Y. Kang *et al.*, "Monolithic germanium/silicon avalanche photodiodes with 340GHz gain-bandwidth product," *Nature Photonics*, vol. 3, no. 1, pp. 59–63, 2009.

[8] S. Cova, A. Longoni, and A. Andreoni, "Towards picosecond resolution with single-photon avalanche diodes," *Review of Scientific Instruments*, vol. 52, no. 3, pp. 408–412, 1981.

[9] A. Rochas, A. R. Pauchard, P. A. Besse, D. Pantic, Z. Prijic, and R. S. Popovic, "Low-noise silicon avalanche photodiodes fabricated in

conventional CMOS technologies," *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 387–394, 2002.

[10] M. J. Lee and W. Y. Choi, "Area-dependent photodetection frequency response characterization of silicon avalanche photodetectors fabricated with standard CMOS technology," *IEEE Transactions on Electron Devices*, vol. 60, no. 3, pp. 998–1004, 2013.

[11] G.-F. Dalla, L. Pancheri, D. Stoppa, R. Henderson, and J. Richardson, "Avalanche photodiodes in submicron CMOS technologies for high-sensitivity imaging," *Intech*, 2011.

[12] I. Vornicu, F. Bandi, R. Carmona-Galan, and A. Rodriguez-Vazquez, "Low-noise and high-efficiency near-IR SPADs in 110nm CIS technology," in *European Solid-State Device Research Conference*, 2019, pp. 250–253.

[13] M. Gersbach, C. Niclass, E. Charbon, J. Richardson, R. Henderson, and L. Grant, "A single photon detector implemented in a 130nm CMOS imaging process," in *Proceedings of the 38th European Solid-State Device Research Conference*, 2008, pp. 270–273.

[14] Dongseok Shin, "Design optimization of the guard ring structures for silicon based single photon avalanche diodes," Ph.D. dissertation, Yonsei University, 2020.

[15] B. Nouri, M. Dandin, and P. Abshire, "Characterization of single-photon avalanche diodes in standard 140-nm SOI CMOS technology," in *Proceedings of IEEE Sensors*, 2009, pp. 1889–1892.

[16] H. S. Kang, M. J. Lee, and W. Y. Choi, "Si avalanche photo detectors fabricated in standard complementary metal-oxide-semiconductor process," *Applied Physics Letters*, vol. 90, no. 15, pp. 3–5, 2007.

[17] Chockalingam Veerappan, "Single-photon avalanche diodes for cancer diagnosis," Ph.D. dissertation, TU Delft, Delft University of Technology, 2016.

[18] S. Dutta, R. J. E. Hueting, A. J. Annema, L. Qi, L. K. Nanver, and J. Schmitz, "Opto-electronic modeling of light emission from avalanche-mode silicon p+n junctions," *Journal of Applied Physics*, vol. 118, no. 11, pp. 1–10, 2015.

[19] J. Ii and S. Perfect, "Avalanche effects in silicon p - n junctions. II. structurally perfect junctions," vol. 32, no. 6, pp. 1591–1599, 1963.

[20] N. A. W. Dutton, "A CMOS SPAD-based image sensor for single photon counting and time of flight imaging," Ph.D. dissertation, University of Edinburgh, 2015.

[21] M. Ghioni, A. Gulinatti, I. Rech, F. Zappa, and S. Cova, "Progress in silicon single-photon avalanche diodes," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 13, no. 4, pp. 852–862, 2007.

[22] M. Gersbach *et al.*, "A low-noise single-photon detector implemented in a 130 nm CMOS imaging process," *Solid-State Electronics*, vol. 53, no. 7, pp. 803–808, 2009.

[23] H. Finkelstein, M. J. Hsu, and S. Esener, "An ultrafast Geiger-mode single-photon avalanche diode in 0.18-µm CMOS technology," in *Advanced Photon Counting Techniques*, 2006, pp. 63720W-1-63720W-10.

[24] H. Finkelstein, M. J. Hsu, and S. C. Esener, "STI-bounded single-photon avalanche diode in a deep-submicrometer CMOS technology," *IEEE Electron Device Letters*, vol. 27, no. 11, pp. 887–889, 2006.

[25] G.A.Petrillo, "Scintillation detection with large-area reach-through avalanche photodiode," *IEEE Transactions on Nuclear Science*, vol. NS-31, no. 1, pp. 417-423, 1984.

[26] M. Lee, "Silicon avalanche photodetectors fabricated with standard CMOS/BiCMOS technology" Ph.D. dissertation, Yonsei University, 2013.

[27] A. J. P. T. Peter Seitz, "Single-photon imaging," *Springer*, 1995.

[28] M. M. Vignetti, F. Calmon, R. Cellier, P. Pittet, L. Quiquerez, and A. Savoy-Navarro, "Design guidelines for the integration of Geiger-mode avalanche diodes in standard CMOS technologies," *Microelectronics Journal*, vol. 46, no. 10, pp. 900–910, 2015.

[29] M. A. Itzler *et al.*, "Single photon avalanche diodes (SPADs) for 1.5 µm photon counting applications," *Journal of Modern Optics*, vol. 54, no. 3–4, pp. 283–304, 2007.

[30] S. Cova, M. Ghioni, M. A. Itzler, J. C. Bienfang, and A. Restelli, "Semiconductor-based detectors", *Elsevier*, 2013.

[31] J. Xue *et al.*, "Low voltage, high brightness CMOS LEDs," in *International Electron Devices Meeting*, 2020, pp. 33.5.1-33.5.4.

[32] D. Shin, B. Park, Y. Chae, and I. Yun, "The effect of a deep virtual guard ring on the device characteristics of silicon single photon avalanche diodes," *IEEE Transactions on Electron Devices*, vol. 66, no. 7, pp. 2986–2991, 2019.

[33] J. A. Richardson, L. A. Grant, and R. K. Henderson, "Low dark count single-photon avalanche diode structure compatible with standard nanometer scale CMOS technology," *IEEE Photonics Technology Letters*, vol. 21, no. 14, pp. 1020–1022, 2009.

Abstract in Korean

CMOS 기술로 제작된 Single-Photon Avalanche Diodes의 성능에 대한 Shallow Trench Isolation 영향

연세대학교 대학원

전기전자공학과

하 원 용

Complementary metal-oxide-semiconductor (CMOS) 공정에서 제작된 single-photon avalanche diode (SPAD)은 거리 측정 기술 분야, 생물 의학 분야 등 여러 분야에서 중요한 역할을 담당하고 있다. 비록, CMOS-SPAD가 가격, 대량 생산, 다른 전자기기와의 통합과 같은 장점을 가지고 있지만, 낮은 sensitivity와 높은 noise라는 한계를 가지고 있다. 더욱이, 보고된 많은 SPAD들을 얇은 multiplication region을 가지고 있어, 장파장

측정에 유리하지 않다.

본 논문에서는 다른 구조의 SPAD들을 비교하여, dark count rate (DCR), afterpusling probability (APP) 와 같은 noise 측면과 photon detection probability (PDP) 측면에서 최적화된 SPAD 구조를 제시한다. 본 논문에서 제시된 SPAD 구조는 P-well/Deep-N-well 구조로 장파장 측정에 유리하게 설계되었고, Dongbu Hitek의 110nm CMOS image sensor 공정으로 SPAD을 설계했다. 첫번째로는 두 SPAD (STI 있는 모델과 없는 모델)을 noise 측면에서 비교했다. 비교를 통해 STI가 없는 SPAD가 더 낮은 noise 특성을 보임을 확인했다. 다음으로, STI가 없는 SPAD와 STI가 일부 있는 SPAD을 비교를 통해, STI가 일부 있는 SPAD의 PDP가 더 높음을 알 수 있었다. 940nm에서 PDP에 관해서는 STI 일부 있는 SPAD의 PDP가 STI 없는 SPAD PDP의 12% 향상이 있음을 확인했다. 추가로, SPAD 일부 있는 SPAD의 noise가 SPAD 없는 SPAD보다 크지만, 합리적인 수준의 noise 크기를 가짐을 보여줬다.

Keywords: 전자 사태 항복, 광검출기, 광소자, 광전자공학, 포토다이오드, 표준 CMOS 공정