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상세보기 중국 마이폴더 다운로드

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(54) Anti noise and burst mode receiving equipment and method for recovering clock signal and its data
恢复时钟信号及其数据的抗噪、猝发模式接收设备和方法

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(57) 요약 Abstract (영문:휴먼번역)

A noise-resistive, burst-mode receiving apparatus and a method for recovering a clock signal and data therefrom are provided. The noise-resistive, burst-mode receiving apparatus includes a voltage control signal generator for multiplying frequency of a system clock signal and for generating a voltage control signal whose level corresponds to the multiplied frequency of the system clock signal; a reset signal generator for delaying an input signal which is irregularly input in the unit of packet, in response to the voltage control signal, carrying out an exclusive OR operation on the delayed signal and the input signal, and outputting the result of the exclusive OR operation as a reset signal; a clock signal generator for generating a signal whose level is changed at the middle point of each bit included in the packet, as a recovered clock signal in response to the reset signal and the voltage control signal and for outputting the recovered clock signal; and an output buffer for buffering the input signal and outputting the buffered signal as recovered data in response to the recovered clock signal. According to this apparatus and method, the clock signal and data can be stably recovered even though errors occur in the input signal has errors due to jitter or other factors. Also, an input signal can be locked within 1 bit according to the present invention, and thus, it is possible to speedily recover a clock signal and data. <IMAGE>

(57) 요약 Abstract

提供一种用于恢复时钟信号及其数据的抗噪、猝发模式接收设备和方法。该设备包括：电压控制信号发生器，倍增系统时钟信号的频率并产生电压控制信号，该信号的电平对应于系统时钟信号的该倍增频率；复位信号发生器，用于响应于该电压控制信号，将以分组单位不规

则输入的输入信号延迟，对该延迟信号和输入信号执行“异或”运算，并把“异或”运算结果输出为复位信号；时钟信号发生器，用于响应于复位信号和电压控制信号，产生在包括在分组中的每个比特T的中点处其电平改变的信号，并且输出该恢复时钟信号；和输出缓存器，缓存输入信号并响应于该恢复时钟信号来输出该缓存信号作为恢复数据。因此，即使输入信号中发生差错，时钟信号和数据也可以可靠恢复。

대표도면

대표도면이 없습니다.

(57) 대표청구항 Exemplary Claim (영문:기계번역)

1.A kind of noiseproof, burst mode receiving apparatus, comprising: A voltage control signal generator, and the frequency used for clock signal of the dynode system is used for producing the control signal of the voltage, the level of the control signal of this voltage is correspondent to the frequency of this multiplication of the systematic clock signal; One reduce signal generator, use for, respond to this voltage control signal, with grouping input signal delay that unit abnormality input into, carry out the operation of XOR exclusive OR to this delayed signal and input signal, and regard result of operation of XOR exclusive OR as the reset signal to export; A clock signal generator, are used for responding to the reset signal and control signal of the voltage, produce the signal that its level changes at middle point including each bits of T in grouping, and output this and resume clock signal; And An output state, are used for buffering the input signal, and respond to this and resume image output of clock and buffer the signal as resuming machine format this, Among them, the stated clock signal generator includes: The second delayer, stated recovery clock signal of delay comes and output this delayed clock signal to use for responding to the stated voltage control signal; The first selector, are used for responding to the stated reset signal, output by

signal; The first selector, are used for responding to the stated reset signal, output by the second delayer delayed signal and stated and resume one of the clock signals selectively; The third delayer, are used for responding to the stated voltage control signal, delay the signal chosen by the first selector, and output the stated delayed signal; First inverter, used in, recover the oppisite phase of the clock signal but also output the stated oppisite phase signal while being stated; The second selector, are used for responding to the stated reset signal, output by the in opposition signal of the first inverter selectively and by one of the third delayer delayed signals; And The second inverter, and the signal oppisite phase that used in being chosen by the second selector resumes the stated oppisite phase signal as being stated the clock signal exporting.

(57) 대표청구항 Exemplary Claim

1.一种抗噪、猝发模式接收设备，包括： 一个电压控制信号发生器，用于倍增系统时钟信号的频率并且用于产生
电压控制信号，该电压控制信号的电平对应于系统时钟信号的该倍增频率； 一个复位信号发生器，用于响应该电压控制信号，将以分组单位不规则
输入的输入信号延迟，对该延迟信号和输入信号执行"异或"运算，并且把"
异或"运算的结果作为复位信号进行输出； 一个时钟信号发生器，用于响应于复位信号和电压控制信号，产生在包
括在分组中的每个比特T的中点处其电平改变的信号，并且输出该恢复时钟信
号；和 一个输出缓存器，用于缓存输入信号，并响应于该恢复时钟信号输出作
为恢复数据的该缓存信号， 其中，所述时钟信号发生器包括： 第二延迟器，用于响应于所述电压控制信号来延迟所述恢复时钟信号并
且输出该延迟的时钟信号； 第一选择器，用于响应于所述复位信号，选择性地输出由第二延迟器延
迟的信号和所述恢复时钟信号其中之一； 第三延迟器，用于响应于所述电压控制信号，延迟由第一选择器选择的
信号，并且输出所述延迟的信号； 第一反相器，用于将所述恢复时钟信号反相并且输出所述反相信号； 第二选择器，用于响应于所述复位信号，选择性地输出由第一反相器反
相的信号和由第三延迟器延迟的信号其中之一；和 第二反相器，用于将由第二选择器选择的信号反相并且把所述反相信号
作为所述恢复时钟信号输出。

전체청구항 전체청구항 보기 (8)

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