Analysis of a Novel Elevated Source Drain MOSFET with High Performance and Low Leakage Current

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김 경 환

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이 논문을 박사 학위논문으로 제출함

2000 년 12 월 일

연세대학교 대학원

전기·전자공학과

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김경환의 박사 학위논문을 인준함

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Analysis of a Novel Elevated Source Drain MOSFET with High Performance and Low Leakage Current

by

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ABSTRACT

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A novel elevated source drain (E-S/D) MOSFET which has reduced leakage current and higher driving capability is proposed and analyzed. The proposed structure has recessed channel structure make use of dry etching process. The device characteristics are determined by the recessed channel depth and sidewall length, which are directly related with the dry etching process. Its main structural advantages are summarized as the elevated source drain extension (SDE) region and the selectively doped channel region. The elevated SDE region helps to avoid low-activation effect caused by very low energy ion implantations. The SDE implantation is performed with large-angle-tilted implantation technique. The selectively doped channel helps reducing the lateral electric field and the junction capacitances. In addition, the self-aligned poly-Si gate is formed by the inverted sidewall spacers so that self-alignment is realized for both source/drain and gate regions on the recessed channel.

In the proposed structure, elevated SDE region helps to alleviate the increase of parasitic resistance at the SDE region by adopting relatively higher implantation energy for the SDE implantation step. In addition, the problem of

gate-induced drain leakage (GIDL) current, which is degraded as the SDE dose is increased, significantly alleviated in case of newly proposed structure. Unlike conventional LDD and SEG MOSFETs, the GIDL current of proposed E-S/D device is decreased without sacrificing the driving current. The E-S/D MOSFET shows approximately one orders of magnitude lower GIDL current than that of LDD MOSFET (HL) having the same SDE implantation dose condition ($5\times10^{14}cm^{-2}$) while maintaining the higher saturation current levels. The main reason for the reduction of GIDL current is the decreased electric field at the point of the maximum band-to-band tunneling as the peak electric field is shifted toward the drain side. From the hot-carrier simulation results, the lateral electric field of the E-S/D device is significantly reduced compared with those of conventional LDD devices under worst bias condition. The selectively doped channel combined with the gradually varying doping distribution of SDE region helps to reduce the electric field near the drain edge. From the short-channel effect simulations, the DIBL and breakdown characteristics are enhanced compared with those of LDD devices. The V_T roll-off characteristics were slightly degraded due to the lack of impurities near the channel edges but the difference between the E-S/D and the LDD devices was comparable.

As the proposed E-S/D MOSFET has simple fabrication steps and simultaneously guarantees the improved device performance and the reduced leakage components, this structure is expected to be a potential candidate for the deep submicron device structures.

Keywords: elevated source drain, dry etching, self-align, SDE, GIDL, lateral electric field, selectively doped channel

Chapter 1 Introduction

Since the development of MOSFET structure in the early 1970's, MOSFET large-scale integration circuits (LSI's) have made great progress. The progress of LSI's is directly related to the scaling of MOSFET structures. By the down-scaling of MOSFET structures, the integration rate of transistors and the functionality of LSI's have been greatly increased. The device performance and the circuit operation speed also have been greatly improved. These facts are the main cause for the downsizing of MOSFET devices.

In the scaling method, the most important matter is to suppress the short channel effects [1-8] to ensure the transistor actions. To suppress the short channel effects, shallow junction and highly doped channel structure are essentially needed. Shallow junction is required for better controllability over conduction carriers and highly doped channel is required for preventing the penetration of depletion region at drain side. However, the shallow junction and highly doped channel have negative effects on the device performances. They make the series resistance of source/drain to be increased and the carrier mobility to be degraded. The junction capacitance is also increased. Fortunately, in the scaling method, unlike any other scaling factors, supply voltage seldom has been changed [9-10]. It is mainly to keep the compatibility with conventional systems. This has imposed additional merit for the improvement of the device performances. However, as the gate length of MOSFET's has been scaled down below 0.5μm, the increased electric field across the gate oxide and the hot-carrier induced degradation have become serious problems, and the supply voltage also started to decrease with the

downsizing of MOSFET structures. As a result, the improvement of device performance has been slowed down. Such problems worsen as the gate length is scaled down to 0.1μm or below.

As the MOSFET's have been scaled down to sub-0.1μm regime, some of scaling factors revealed its limitations for further scaling [11]. For example, the gate oxide thickness and the threshold voltage are restricted due to the direct tunneling of electrons and the leakage current, respectively. Such facts make the scaling of MOSFET structures more difficult because the device performance can be hardly improved. Furthermore, due to the extremely large number of transistors integrated on a chip, suppressing the cutoff leakage and decreasing the junction capacitance are also becoming very important for the low power and high-speed MOSFET technologies.

Since there are trade-off relationships between the device performance and the short channel behaviors, and the situation is even worse as MOSFET structures are scaled down to 0.1μm regime, there have been many efforts to overcome such problems for maximizing the device performances. Modifying the device structure from the conventional structure is one of the effective methods for solving such problems. Elevated source drain (E-S/D) structure is one example of such modifications. This structure is expected to enhance the device performance even in the sub-0.1μm technologies. The main idea of the E-S/D structure is that the shallow junction can be more easily formed make use of the extra silicon region existing above the source/drain region.

Many E-S/D MOSFETs have been proposed to enhance the device performance and to suppress the short channel effects [12-25]. It was first proposed to effectively suppress the short channel effects by reducing the

junction depth [12]. Thereafter, more attention has been given to hot-carrier problems and the improvement of the device performances [13-14]. E-S/D MOSFET with Selective Epitaxial Growth (SEG) process [21-24], Grooved Gate MOSFET [15-16] and Recessed Channel MOSFET [17-20] are well known type of E-S/D MOSFETs.

E-S/D MOSFET with SEG process is one example of E-S/D MOSFET, which utilizes the silicon growth by epitaxy. Crystalline silicon layer is selectively grown on the source/drain side resulting in the E-S/D structure. This technology is favorable in that the fabrication step is very similar to that of conventional devices except for the epitaxy process. However, facet generation and additional thermal budget problem exists in the process. Recently, many works concerning SEG process are being developed and widely studied in the device manufacturing fields.

Grooved gate MOSFET and recessed channel MOSFET are another kinds of E-S/D MOSFET. Unlike the E-S/D MOSFET with SEG process, these MOSFETs don't realize the E-S/D structure by means of epitaxial growth of silicon. These methods use etching or field oxidation process to make the recessed channel structure. The main difference from the E-S/D MOSFET with SEG process is that the silicon is removed rather than additionally grown from the original silicon surface. Grooved gate MOSFET is reported to have advantages in suppressing the short-channel effects with the help of corner effect. On the contrary, it is also reported that the corner effect deteriorates the enhancement of device performances due to the large potential barrier. The recessed channel MOSFET structures are reported to have better trade-off relationships between the driving capability and the short channel effects.

However, in respect of self-alignment problem and fabrication complexities, there are still rooms to be improved.

Recently, E-S/D MOSFETs are expected to be potential candidates for the sub-0.1μm devices [9],[18]. As stated previously, in the conventional MOSFET structures, the improvement of the device performance can be hardly expected for the sub-0.1μm devices due to the limitation factors such as the source/drain junction depth, the gate oxide thickness and the threshold voltage. The source/drain junction depth is becoming extremely shallow (<50nm) increasing the series resistance of source/drain region. The channel impurity concentration is becoming very high (~$1\times10^{18}cm^{-3}$) degrading carrier mobility and isolation properties of the substrate. And the gate oxide thickness cannot be further decreased below 15nm due to the direct tunneling of electrons [10]. The threshold voltage also cannot be continuously decreased, to ensure low off-state leakage current.

In order to make ultrashallow junctions with the conventional ion implantation technology, very low-energy ion implantation and rapid thermal annealing is indispensable. However, the low implantation energy causes higher sheet resistance due to the low-activation effect [26]. In various recent works [26-28], the Source Drain Extension (SDE) region is usually formed with relatively higher implantation dose to ensure enhanced driving capabilities. But in conventional Lightly Doped Drain (LDD) MOSFETs, the increase of the SDE implantation dose results in the increase of the Gate-Induced Drain Leakage (GIDL) current [28]. GIDL is one of the major leakage components that determine the off-state leakage characteristics and it can also act as a scaling limiting factor in deep submicron devices [29-30].

Consequently, for the conventional LDD structures, there exists a significant trade-off relationship between the driving capability and the GIDL current. Since the aim of improving the device performance is very important as the device is scaled down, increasing the SDE dose seems to be inevitable. However, the problem of increased leakage current due to the increased SDE dose should also be carefully investigated and solved. As for the highly doped channel structure, the impurity scattering and highly doped p-n junction problem deteriorates the device performances. In addition, the junction capacitance is also increased resulting in the degradation of device speed.

In this thesis work, a novel self-aligned E-S/D MOSFET structure [31] is proposed to solve the ultrashallow junction and the heavily doped channel problems. The recessed channel of this structure is realized by the dry etching process, and its electrical characteristics are mainly determined by the shape of recessed channel. It has solved the self-alignment problem which is often the serious problem in the recessed channel MOSFETs. The proposed structure is self-aligned for both the source/drain and gate regions on the recessed channel. And it is designed to have elevated SDE region to improve the driving capability. The relatively higher energy ion implantation step combined with the large-angle-tilted implantation method is used for avoiding the low activation effect. The selectively doped channel and its impact on the hot-carrier characteristics are investigated. Conventional LDD MOSFETs with different SDE dose are designed to compare their electrical characteristics with that of the proposed structure. Several conventional E-S/D MOSFETs with SEG process are also designed for comparison with the proposed structure.

Since there have been difficulties in fabricating various kinds of device

structures having exact the desired design parameters, two-dimensional process and device simulators are used to study alternative MOSFET structures extensively [32].

This thesis work is organized as follows. In chapter 1, the introduction of this thesis work is presented. In chapter 2, the characteristics of E-S/D MOSFETs and the factors to be considered in deep submicron MOSFETs are explained. Particularly, previously reported E-S/D structures and the theories of GIDL and hot-carrier effects are described more in detail. In Chapter 3, the details on the design of proposed E-S/D MOSFET are discussed. Various simulation results confirming the benefits of the proposed structure are given in Chapter 4. The GIDL characteristics of the E-S/D and conventional LDD MOSFETs are compared and the differences between these structures are explained. Short channel characteristics and current driving capability of the proposed E-S/D MOSFET are compared with the conventional ones. Several kinds of E-S/D MOSFETs with SEG process are presented and compared each other. Finally, the conclusion will be presented in Chapter 5.

Chapter 2 Backgrounds

In this chapter, the characteristics of elevated source drain (E-S/D) MOSFET and some of the factors to be considered in designing of deep submicron devices are described. The general features of the E-S/D MOSFETs are explained and the previously reported E-S/D MOSFETs are introduced to help for understanding the thesis work. The threshold voltage lowering effect and the drain induced barrier lowering effect among the short channel effects are explained for the analysis of the device characteristics. In addition, the Gate-Induced Drain Leakage (GIDL) and the hot-carrier effects are explained more in detail.

2.1 The Characteristics of Elevated Source Drain MOSFET

Elevated Source Drain (E-S/D) MOSFET is a modified MOSFET structure which has elevated source drain (or recessed channel) region unlike the conventional MOSFETs. It is also called Raised Source Drain MOSFET. Grooved Gate MOSFET [15-16], Gate Recessed MOSFET [17], Recessed Channel MOSFET [19] and the E-S/D MOSFETs with Selective Epitaxial Growth (SEG) process [21-24] are some examples of such E-S/D MOSFETs. Figure 2-1 shows simplified schematic cross section of E-S/D MOSFET. The main difference between E-S/D and conventional MOSFET is that the surface of S/D is located above the channel interface. To obtain such structure, one of the following should be proceeded: 1) the channel region is etched away 2) the S/D regions are additionally grown by epitaxy process. As can be seen

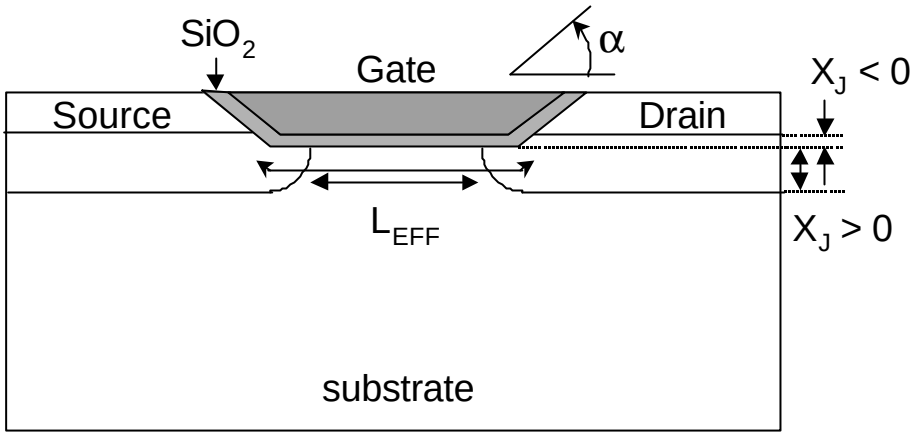


Fig. 2-1. Simplified schematic cross section of E-S/D MOSFET structure.

from the figure, the junction depth (X_J) can be more easily restricted to have very shallow junction in E-S/D MOSFET. It is shown that even the negative value of junction depth (*i.e.* $X_J<0$) is also possible for E-S/D MOSFETs.

E-S/D structure was first proposed to effectively suppress the short channel effects by reducing the junction depth while preventing the series resistance of the source/drain to be increased. As the hot-carrier induced degradation have become serious concern in the MOSFET technology, several modified structures, hot-carrier suppressed (HCS) MOSFET [13] and profile doped E-S/D MOSFET [14] were proposed to solve the problem. Recently, the E-S/D MOSFETs are gaining more attention as potential candidates for the sub-0.1μm MOSFET structures. It is mainly because the improvement of device performance can be hardly achieved in the conventional MOSFET structures below 0.1μm dimension. On the other hand, the improvement of device performance can be expected in the E-S/D structure below 0.1μm dimension

because the junction depth can be scaled more freely without increasing the series resistance of source/drain regions.

2.1.1 Gate Grooved or Gate Recessed MOSFET

Figure 2-2 shows the schematic view of the Grooved Gate MOSFET and the Gate Recessed MOSFET. The process steps for fabricating the Grooved Gate MOSFET is as follows [15]: (1) elevated S/D delineation and the diffusion layer implantation for S/D; (2) sidewall oxide formation and self-aligned groove formation and B-ion punchthrough implantation; (3) gate oxidation and W gate electrode delineation and metallization. This process is reported to enable spacing of less than 0.1μm for the gate. According to Tanaka *et al*. [16], in the Gate Grooved case, large and steep potential barriers are formed at the corner of gate edges when $X_J<0$ (see Fig. 2-1) and the device characteristics are dominantly affected by the existence of such potential barriers. Such "corner effect" is determined by corner angle α ($0<\alpha<90°$) and the channel doping concentrations (see Fig. 2-1). As the corner angle α and the channel doping concentration are increased, the corner effect is becoming more definite. The potential barrier caused by the corner effect is maintained even if the channel length is scaled down. It means that the influence of the drain side is less severe by help of the potential barrier resulting in the better short channel characteristics. Figure 2-3 shows the surface potential distribution of the E-S/D MOSFET with corner effect and that of the conventional MOSFETs.

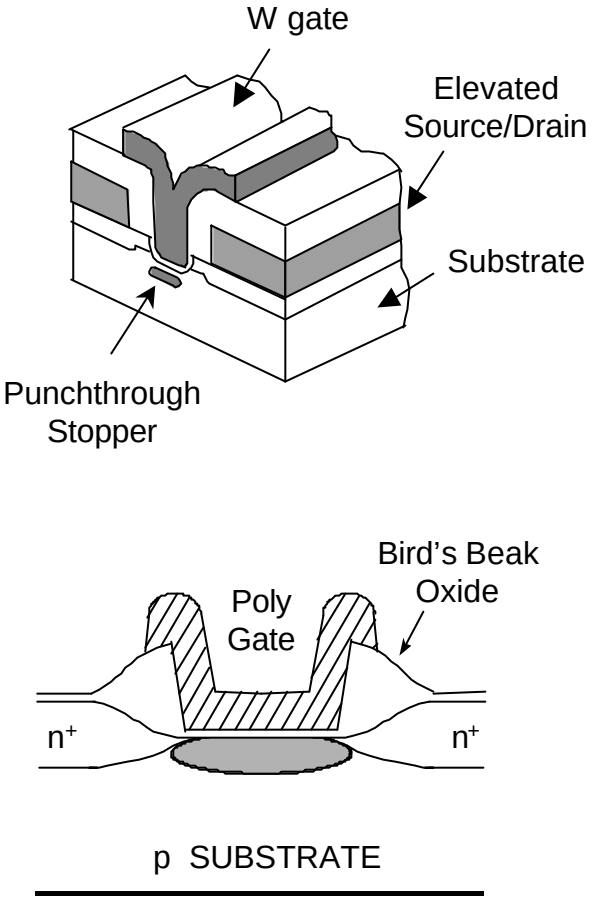


Fig. 2-2. The schematic cross section of Gate Grooved MOSFET and Gate Recessed MOSFET [15],[17].

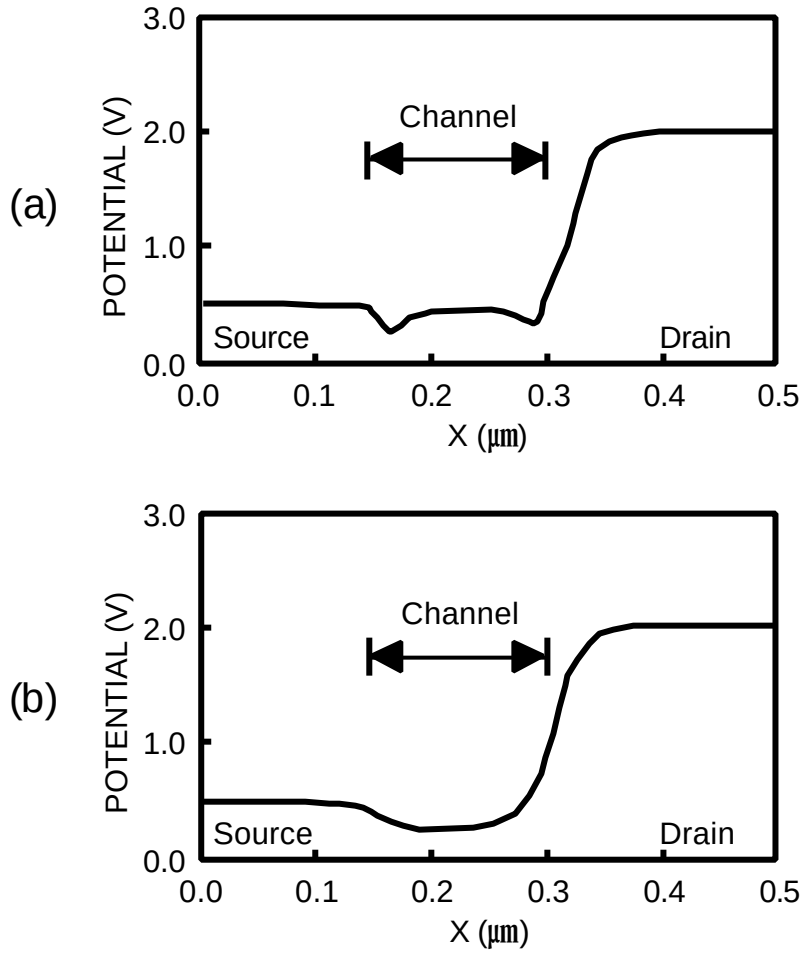


Fig. 2-3. Surface potential distribution of (a) E-S/D MOSFET with corner effect and (b) conventional MOSFET [16].

However, the corner effect is known to deteriorate the driving capability due to the existence of large potential barrier. In the Grooved Gate MOSFET, the complex fabrication steps, unfitness for the dual (poly) gate MOSFET technology and the reduced driving capability problems should be solved for high performance applications.

Another method for fabricating E-S/D MOSFET is the Gate Recessed (or Recessed Channel) MOSFET [17],[19]. In such structures, the recessed channel is constructed as follows: (1) The field oxide is grown on the active region and the silicon is consumed during the oxidation step; (2) By etching all of the field oxide, recessed channel is formed on the active area; (3) After the channel implantations, poly-Si gate is formed on the recessed channel. The channel implantation is performed through the field-oxide-etched region resulting in the selectively doped channel structure. The channel doping and S/D doping are both decreasing near the channel edges. The lateral doping profiles of such structure is compared with that of conventional LDD MOSFETs in Fig. 2-4. This doping profile is obtained by the bird's beak of the locally oxidized channel and provides some advantages compared with LDD structures. The reported advantages are reduced junction capacitance by using the selective channel doping method, increased current driving capability by forming the deeper S/D junction, reduced hot-carrier generation by reducing the lateral electric field at the drain edge, reduced impurity scattering at channel edges and reduced penetration of the drain field through the source by graded drain doping profile.

However, the formation of the self-aligned poly-Si gate on the recessed channel is a difficult task for such structures. Emphasis on the self-alignment

in both source/drain and gate structure in recessed channel region was made by J.H. Lee *et al*. [20]. Figure 2-5 shows the schematic cross section of self-aligned recessed channel SOI structure. This structure was reported to have achieved for the first time that the self-alignment was achieved in both source/drain and gate structure in recessed channel Silicon-On-Insulator (SOI) device fabrication. The device needs no margin in layer-to-layer registration due to the self-alignment.

However, it requires consideration from various structural aspects. This structure is reported to have "LOCOS-like" shape poly-Si gate, and it is expected that the fabrication difficulty and reproducibility still remain to be solved. Since the E-S/D MOSFETs are not yet the major device structure in the present-day LSI technologies, many efforts still have been made for the development of high performance E-S/D MOSFETs.

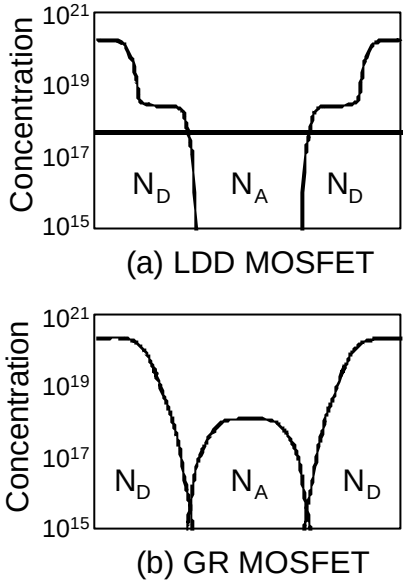


Fig. 2-4. The lateral doping profiles of (a) LDD MOSFET and (b) GR MOSFET structure [17].

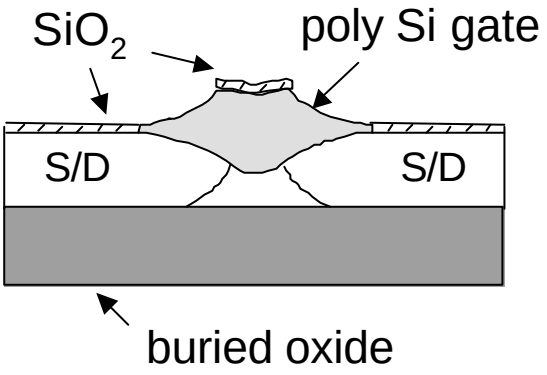


Fig. 2-5. Schematic cross sectional view of self-aligned recessed channel SOI structure [20].

2.1.2 E-S/D MOSFET with Selective Epitaxial Growth Process

Elevated source drain (E-S/D) structure can be achieved with the Selective Epitaxial Growth (SEG) process. These types of E-S/D MOSFETs have very similar fabrication steps to those of conventional LDD MOSFETs. The SEG step is added to the conventional LDD MOSFET process to form the elevated source/drain region. Usually, after the source drain extension (SDE) implantation step, additional silicon layers are grown selectively at source/drain regions by epitaxy. Compared with other E-S/D MOSFETs, these kinds of structures (here after SEG MOSFETs for convenience) have benefit in the process compatibility.

The SEG MOSFETs have several advantages over the conventional MOSFETs. Epitaxially grown extra Si-layer above the source/drain region helps to solve the contact spiking problem and the silicon consumption problem caused by the silicide process. Furthermore, if the thermal budget is strictly limited, the extra Si-layer helps to reduce the junction depth. Figure 2-6 shows the difference between SEG MOSFET and conventional MOSFET.

On the contrary, the SEG type MOSFETs have some problems to be solved. The growth rate of the silicon during the epitaxy is different at the sidewall spacer edge or at the field oxide edge compared to that at the plain Si surfaces. Because of the difference in the growth rate, the facet is generated [33] as shown in Fig. 2-6. During the heavy source drain implantation, junction depth is not kept uniform due to the facet near sidewall spacer. More dopants are penetrated near the channel region deteriorating the short channel behaviors.

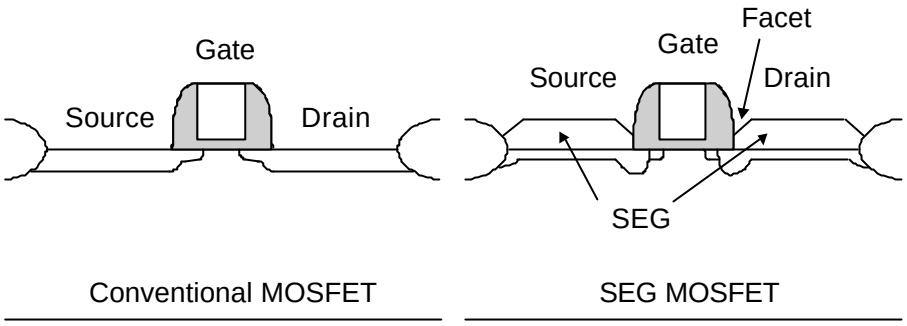


Fig. 2-6. Conventional LDD MOSFET and SEG MOSFET

As for the well-known methods to prevent such degradation of the short channel effects, one is the use of sidewall spacer twice [23] and the other is the use of removable nitride spacers [22]. Figure 2-7 shows the two methods to prevent the degradation of the short channel effects caused by the facets. In the first method, sidewall spacers are formed both before and after the selective epitaxial silicon deposition in S/D regions. In the second method, disposable nitride spacers are used before the selective epitaxial silicon deposition and then nitride spacers are completely removed. LDD implantation is performed and the permanent nitride sidewall spacers are formed to cover the facet regions. This method is advantageous in that the LDD junctions are not exposed to the high temperature prebake and deposition conditions. Shallow LDD junctions provide improved short channel behavior while maintaining good hot-carrier protection. Both the methods have in common that the facet region is covered with insulator material to avoid the facet effects. As a result, the short channel degradation caused by the facet is effectively suppressed.

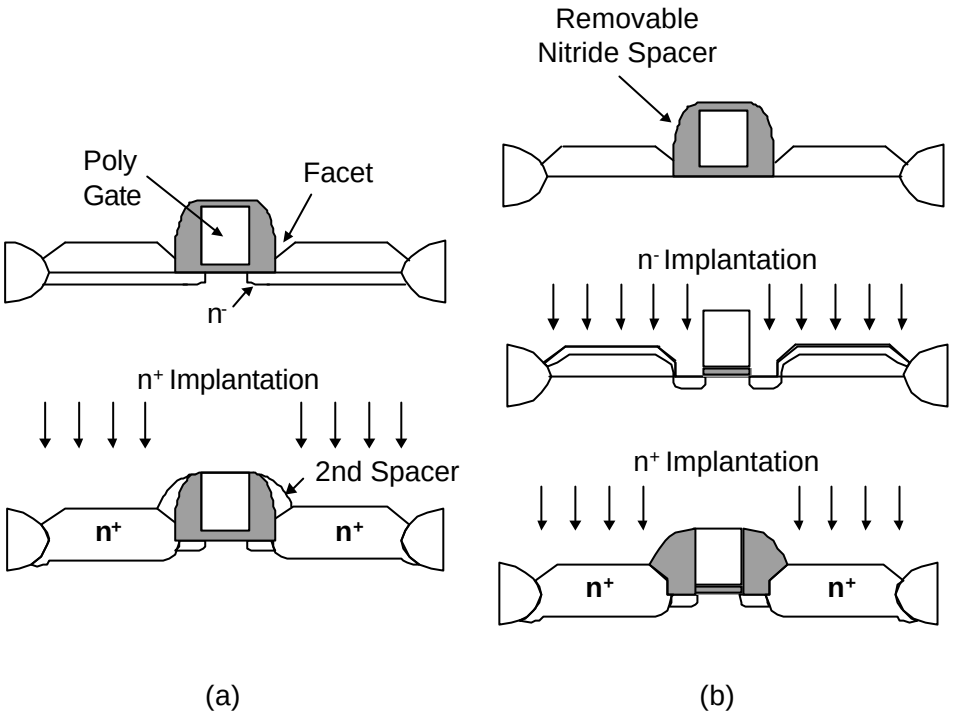


Fig. 2-7. Methods of preventing the degradation of short channel effects caused by the facets [22-23]: (a) Second sidewall is used to cover the facet region. (b) Removable nitride sidewall is used prior to SDE implantation.

However, if the heavy source/drain implantation is performed after the facet region is covered, the device should be designed considering the device performances. It is because the insulator material which covers the facet region, has the effect of increasing the sidewall spacer thickness.

2.2 Factors to be Considered in Deep Submicron Devices

As the MOSFETs have been scaled down to submicron region, various kinds of phenomena are observed that were not observed in the long channel devices. These phenomena are so-called the “short-channel effects”. The short-channel effects can be divided into three categories, one is the effects that affect the threshold voltage characteristics, the second is related to the subthreshold current characteristics and the third is the ones that affect the saturation current characteristics. Among the various short-channel effects, the threshold voltage lowering effect and the drain induced barrier lowering effect are explained because these effects are often used as major indicators for the short channel characteristics. In addition, the gate-induced drain leakage and the hot-carrier-induced current generation are explained more in detail, which are the main interest throughout the thesis work.

2.2.1 Threshold Voltage Lowering Effect and Drain Induced Barrier Lowering Effect

Threshold voltage (V_T) lowering effect is the most well known phenomenon among the short-channel effects [34]. The channel depletion charge consists of depletion charge which is influenced by gate and space charge which is caused by the junction depletion regions. As the channel length is scaled down, the space charge caused by the junction depletion region occupies a greater part of the channel depletion region. Consequently,

gate needs a smaller control voltage, V_T, to turn on the device. As there is appropriate threshold voltage to effectively suppress the leakage current, threshold voltage lowering effect is the cause of increased leakage current deteriorating the device electrical behaviors. Usually, the threshold voltage adjust implantation is used to increase the threshold voltage. However, the degradation of mobility and the increase of junction capacitance should also be carefully considered.

The threshold voltage lowering effect is also regarded as an indicator for the scaling limitations. It is reported that in order to turn the device off properly at room temperature allowing process and temperature tolerances, a minimum threshold voltage of 0.4V is required [35]. In Fig. 2-8, the sample device A reaches more faster to its scaling limitation compared with the sample device B.

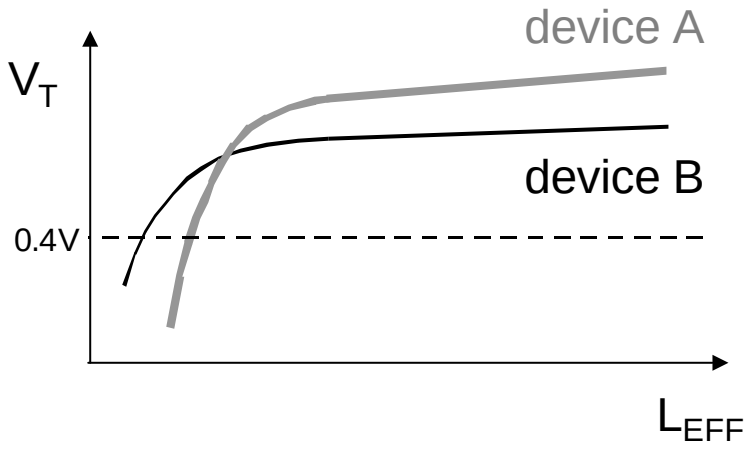


Fig. 2-8. Threshold voltage (V_T) roll-off characteristics as a function of effective channel length (L_{EFF}).

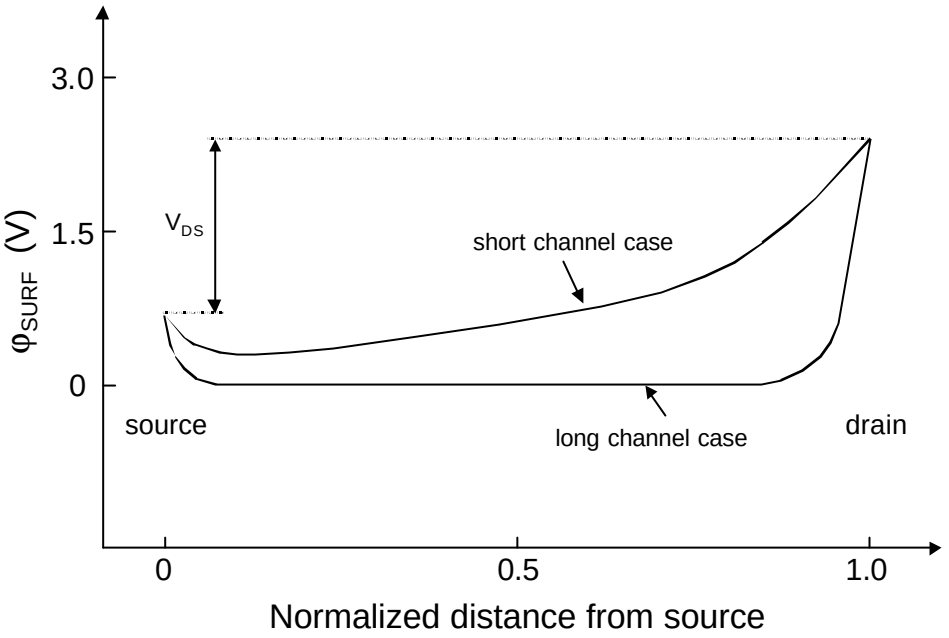


Fig. 2-9. Surface potential distribution for constant gate voltage. The potential barrier of the source is lowered in case of short channel device.

Drain-induced barrier lowering (DIBL) is another kind of short-channel effect that is widely used for estimating the amount of short channel degradation [1]. DIBL is a phenomenon that the potential barrier of source is lowered by the penetration of the electric field caused by the potential of drain side. Figure 2-9 shows the surface potential distribution along the channel that illustrates the concept of DIBL. As the distance between the source and drain is becoming closer (i.e. short channel case), the potential barrier of source side is lowered, which is greatly affected by the potential of drain side.

DIBL is more likely to occur 1) the deeper the source/drain diffusions, 2) the higher the substrate resistivity, and 3) the closer the diffusion-to-diffusion

spacing [1]. The main result due to DIBL effect can be summarized as follows: the decrease of threshold voltage and the increase of subthreshold current.

The DIBL is extracted using the I_{DS}-V_{GS} plot. Figure 2-10 shows the I_{DS}-V_{GS} plot with V_{GS}=0V. Usually, the DIBL is defined as $\triangle V_{TH}$= $V_{TH}(V_{DS}=0.1V)$-$V_{TH}(V_{DS}=V_{DD})$.

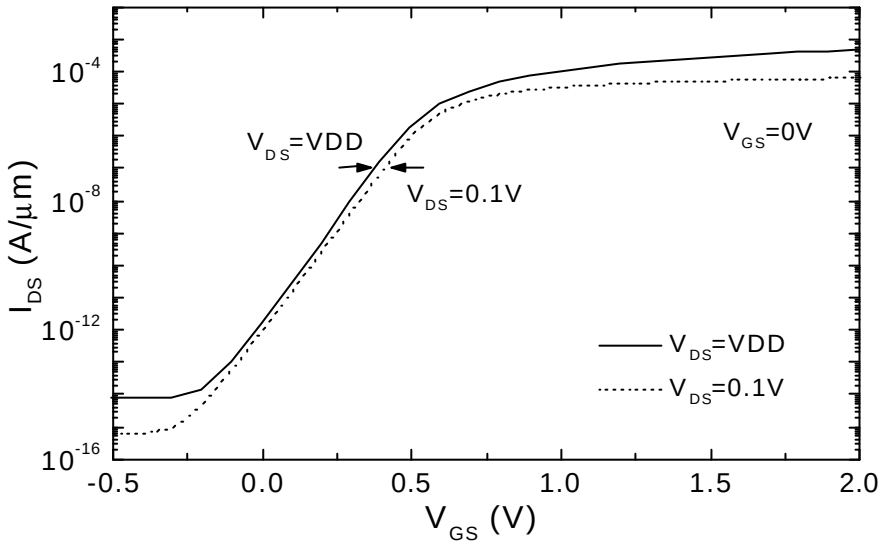


Fig. 2-10. I_{DS}-V_{GS} plot for extracting the value of Drain-Induced Barrier Lowering (DIBL).

2.2.2 Gate-Induced Drain Leakage (GIDL)

Gate-induced drain leakage (GIDL) is one of leakage current observed in off-state MOSFETs [29-30],[36-37]. Because there are growing demand for battery-operated portable electronics, minimizing the off-state leakage current is becoming more important. Furthermore, the GIDL is reported to play a key role in determining the scaling limitation in deep submicron devices [29-30].

GIDL occurs when there exists a large electric field across the gate oxide. From bias point of view, the gate is grounded and the drain is at V_{DD}. The simple schematic view of the gate-induced drain leakage mechanism for n-channel device is shown in Fig. 2-11 [34]. The electric field is supported by charge in the drain depletion region. As the electric field becomes sufficiently large, an inversion layer is likely to be formed at the silicon surface of the drain side. However, as the minority carriers (i.e. holes) arrive at the surface to form the inversion layer, they are immediately swept laterally to the substrate. It is because the potential of the substrate is lower for holes than the surface potential of the drain. Consequently, an inversion layer cannot be formed at the surface of the drain. As a result, the holes are immediately swept to the lower potential substrate. The current component from this phenomenon constitutes the GIDL current.

Band-to-band or band-to-trap tunneling is reported to be the responsible mechanism for GIDL. Figure 2-12 shows the energy band diagram of the gate oxide-n^+ drain region. The possible components for the GIDL generation are presented. The mechanisms for the GIDL generation have been widely investigated. It was reported that the traps caused by hot-carrier injection

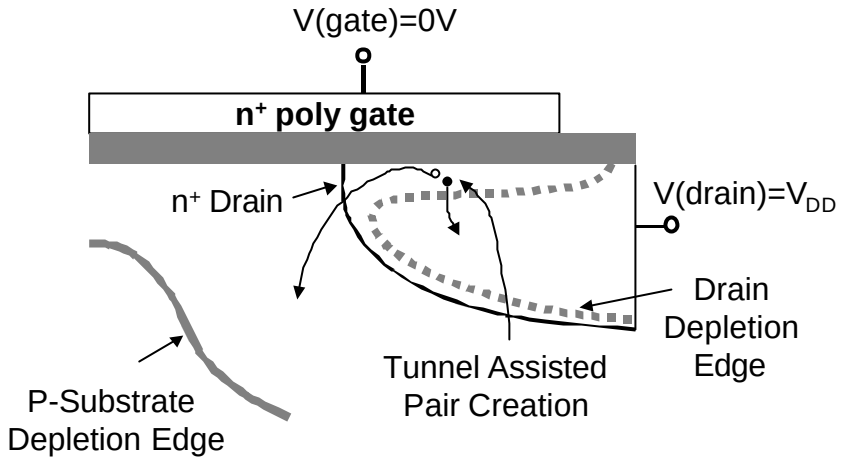


Fig. 2-11. Simplified schematic view of gate-induced drain leakage generation for n-channel MOSFET [34].

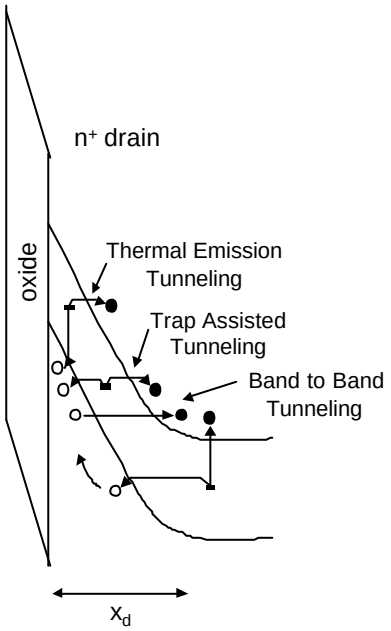


Fig. 2-12. Energy band diagram of n^+ drain - gate oxide region [38]. The possible components of the GIDL current generation are described.

might cause the GIDL to be increased. Ge preamorphization [39] and Fowler-Nordheim tunneling [40] were also reported to increase the GIDL current.

To suppress the GIDL current, several methods can be effectively adopted. Since the electric field between the drain and the gate is reduced as the gate oxide thickness (T_{OX}) is increased, T_{OX} can be increased to reduce GIDL. However, this method is unfavorable because it results in the degradation of short channel characteristics and the reduction of current driving capability. Poly re-oxidation process was also reported to be effective in reducing the GIDL [30] due to the locally increased T_{OX}. Another method for reducing the GIDL current is minimizing the trap density near the Si-SiO_2 interface. This method is mainly related to the ultraclean fabrication technologies. The LDD structure was also reported to be effective in suppressing the GIDL current because the lateral electric field can be suppressed.

According to Chan *et al.* [36], to limit the undesirable GIDL current to 0.1pA per μm channel width, the oxide field in the gate-to-drain overlap region must be limited to 1.9MV/cm. This relation sets another limit to the minimum oxide thickness or the maximum power supply voltage in MOSFET scaling, and can be described as [36],

$$V_{CC} = 1.2 + T_{OX} \times 1.9 MV/cm \qquad (2\text{-}1)$$

where T_{OX} is the gate oxide thickness.

In the n-channel MOSFET, the band-to-band tunneling results in the generation of electron-hole pairs and the holes are swept to the substrate region making the off-state leakage current. It occurs in regions of high electric field where the local band bending causes the tunneling probability to become significant.

The tunneling probability in the band-to-band tunneling can be extracted from the parabolic barrier properties [41]. For the parabolic barrier, E_0 is defined as the energy measured from the electron energy to the center of the band, and the form of (PE-E) is [42]

$$PE - E = \frac{(E_G/2)^2 - E_0^2}{E_G} = \frac{(E_G/2)^2 - (eE \cdot x)^2}{E_G} \qquad (2\text{-}2)$$

where PE is the potential energy and E the incoming electron energy, E_G the bandgap of the semiconductor, and E the electric field. This form is also the simplest algebraic function that has the correct behavior at the band edges [41]. Then the probability can be given by the WKB approximation (Wentzel-Kramers-Brillouin method) [43]:

$$\begin{aligned} P_t &\cong \exp\left[-2\int_{-x_1}^{x_2} |k(x)|dx\right] \\ &= \exp\left[-2\int_{-x_1}^{x_2} \sqrt{\frac{2m^*}{\eta^2}\left(\frac{(E_G/2)^2 - (eE \cdot x)^2}{E_G}\right)}dx\right] \\ &= \exp\left(-\frac{pm^{*1.2}E_G^{3/2}}{2\sqrt{2}q\eta E}\right) \end{aligned} \qquad (2\text{-}3)$$

where k(x) is the absolute value of the wave vector of the carrier in the barrier, and $-x_1$ and x_2 are the classical turning points. From the probability relationship, band-to-band tunneling is modeled with the following equation [36-37]:

$$J_t = \frac{A}{B}E_S \exp\left(-\frac{B}{E_S}\right) \qquad (2\text{-}4)$$

where

$$A = \frac{2qm^* pE_G^2}{h^3} \tag{2-5}$$

and

$$B = \frac{p^2\sqrt{m^*}E_G^{3/2}}{qh\sqrt{2}} = 21.3\frac{MV}{cm} \tag{2-6}$$

where E_S is the electric field at the point of maximum band-to-band tunneling. This field has been modeled as [37]:

$$E_S = \frac{V_{DG} - V_{FB} - 1.12}{3T_{ox}} \tag{2-7}$$

This model is suitable for the devices with no LDD or with fully-overlapped LDD's. Figure 2-13 shows the schematic cross section of devices with no LDD and with fully-overlapped cases.

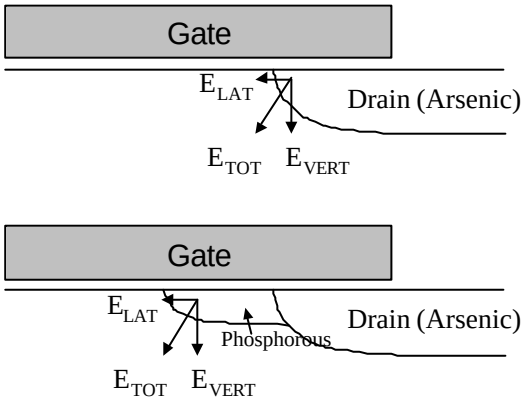


Fig. 2-13. The schematic cross sections of non LDD (upper) and fully-overlapped LDD device (bottom). The total electric field is the vector sum of E_{LAT} and E_{VERT}. By increasing the phosphorous doping, E_{LAT} is suppressed similar to non LDD case.

In these cases, the lateral field is suppressed while the drain concentration is high enough so that the dominant tunneling point has a band bending of 1.12eV. The average electric field for the tunneling current equation is obtained by dividing the surface field by 2 [37].

On the other hand, for the devices with nonfully overlapped LDD's, the model in (2-7) is not adequate since the total band bending in the silicon is more than the required E_G due to drain depletion. The average electric field that the tunneling electron experiences should be used in (2-4) instead of surface electric field. In the nonfully-overlapped LDD, average electric field is [29],

$$E_{TOT} \approx (E_{VERT})_{avg} = \frac{E_S}{h} \qquad 1 \le h \le 2 \qquad (2\text{-}8)$$

For the derivation of η, the exact 2-dimensional doping profile, which varies according to processes, should be calculated with the help of device simulators.

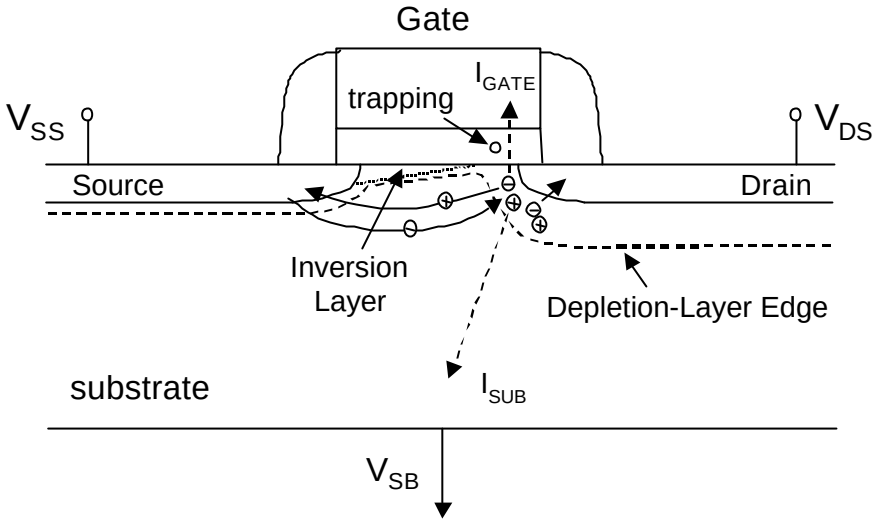


Fig. 2-14. A schematic illustration of the hot-carrier-induced current generation for n-MOSFET.

2.2.3 Hot-Carrier-Induced Current Generation: Substrate Current and Gate Current

Hot-carrier effect is one of serious problems that occur as a result of downsizing process. Since the supply voltage has been changed much slowly unlike other scaling factors, hot-carrier induced degradation greatly menaced the device reliability problems. The hot-carrier current generation can be explained by impact ionization and channel hot-carrier injection. Impact ionization occurs when there exists a large electric field in the channel. The conduction carriers are accelerated to have sufficient kinetic energy to cause an ionizing collision with the lattice. The electron-hole pairs are created during the collision process. Furthermore, if the carriers acquire sufficient energy

from the lateral electric field, they can surmount the Si-SiO_2 barrier resulting in the channel hot-carrier injection. Thus, the measurement of substrate current and gate current are widely used as an indicator for estimating the impact ionization and channel hot-carrier injections.

The two current components are schematically illustrated in Fig. 2-14. The substrate current (I_{SUB}) is formed by the electrons or holes created by impact ionization process and drift into substrate contact. This substrate current is correlated with device degradation reducing the device lifetime [44-45]. The gate current (I_{GATE}) is usually formed by the conduction electrons with high kinetic energy, which can surmount the Si-SiO_2 barrier at the channel interface. The injected carriers constitute the gate current.

The substrate current model for n-channel MOSFET is simply expressed as [46],

$$I_{sub} = I_{ds} \int_0^{l_{sat}} a_n dy \qquad (2\text{-}9)$$

where I_{ds} is the drain current, l_{sat} is the velocity saturated length of the channel, and α_n is the electron impact ionization rate. Note that α_n is directly correlated with the lateral electric field distribution and can be expressed as

$$a_n = A_i \exp\left(-\frac{B_i}{E}\right) \qquad (2\text{-}10)$$

where A_i and B_i are the ionization constants. E is the channel electric field. The channel electric field and potential can be expressed based on a quasi-two-dimensional model as [46]

$$E(y) = E_{sat} \cosh\left(\frac{y}{l_d}\right) \qquad (2\text{-}11)$$

$$V(y) = V_{dsat} + I_d E_{sat} \sinh\left(\frac{y}{l_d}\right) \tag{2-12}$$

where y is the distance along the channel. (y=0 at the starting point of velocity saturation) E_{sat} is the electric field at which the carriers reach the velocity saturation. In the saturation region, the electron velocity saturates because the lateral electric field exceeds the saturation field, $E_{sat}=4\times10^4$V/cm. l_d is an effective ionization length and can be expressed as [47]

$$l_d^2 = \frac{e_{si}}{e_{ox}} t_{ox} X_j \tag{2-13}$$

where t_{ox} is the gate oxide thickness and X_j is the junction depth. If (2-11) and (2-12) are solved for expressing E(y), and (2-10) is replaced for α_n in (2-9), The substrate current can be described as [48]

$$\begin{aligned} I_{sub} &= I_{ds} A_i \int_0^{l_{sat}} \exp\left(-\frac{B_i}{E}\right) dy \\ &= I_{ds} A_i l_d \int_{E_{sat}}^{E_m} \frac{1}{\sqrt{(E_m^2 - E_{sat}^2)}} \exp\left(-\frac{B_i}{E_m}\right) \\ &\cong I_{ds} A_i l_d \frac{1}{\sqrt{(E_m^2 - E_{sat}^2)}} \frac{E_m^2}{B_i} \exp\left(-\frac{B_i}{E_m}\right) \end{aligned} \tag{2-14}$$

From the above equations, it is shown that I_{sub} depends exponentially on the E_m. Consequently, the exact modeling of E_m is very important in the modeling of the substrate current. If E_m is approximated to $(V_{ds}-V_{dsat})/l_d$, widely used form of I_{sub} is obtained as [49]

$$I_{sub} = I_{ds} \frac{A_i}{B_i} (V_{ds} - V_{dsat}) \exp\left(-\frac{l_d B_i}{V_{ds} - V_{dsat}}\right) \tag{2-15}$$

According to Arora and Sharma [48], E_m is approximated to $(V_{ds}-\eta V_{dsat})/l_d$,

which has considered the empirical factors ($0<\eta\leq 1$). l_d is also modified to take the bias dependency into account and is given as

$$l_d = l_0 + l_1(V_{ds} - V_{geff}) + l_2(V_{ds} - V_{geff})^2 \qquad (2\text{-}16)$$

where $V_{geff}=V_{gs}-V_{th0}$. V_{th0} is the threshold voltage at $V_{bs}=0$, l_0, l_1, l_2 are fitting parameters. The substrate current equation can be then expressed as [48]

$$I_{sub} = I_{ds}\frac{A_i}{B_i}(V_{ds} - hV_{dsat}) \cdot \exp\left[-\frac{B_i}{(V_{ds} - hV_{dsat})}\{l_0 + l_1(V_{ds} - V_{geff}) + l_2(V_{ds} - V_{geff})^2\}\right] \qquad (2\text{-}17)$$

The gate current generation is modeled by "lucky-electron model" [50]. The principle ideas of the model are based on the lucky electron concept. This model calculates the probabilities for certain scattering events to occur that result in current being injected into the gate. The total gate current can be obtained by integrating the flux of carriers injected into the gate from each location in the device structure. Channel hot-electron injection into the gate can result in the degradation of device performance due to the trapping of electrons in the gate oxide and the generation of interface traps [51].

To generate the gate current by hot electrons, the hot electrons must gain high enough kinetic energy from the channel electric field and has its momentum redirected towards the Si-SiO_2 interface in order to surmount the SiO_2 potential barrier. The probability of an electron acquiring the required kinetic energy and retaining the appropriate momentum after redirection can be expressed as [51]

$$P_{\Phi_b} = \int_{\Delta\Phi=0}^{\Delta\Phi=\infty} \frac{\Delta\Phi}{4\Phi} e^{-[(\Phi_b+\Delta\Phi)/E_x l]} \frac{d(\Delta\Phi)}{E_x l}$$
$$= 0.25 \frac{E_x l}{\Phi_b} e^{-(\Phi_b/E_x l)} \qquad (2\text{-}18)$$

where Φ_b is the Si-SiO_2 potential barrier, λ is the scattering mean-free-path of the hot electron.

The hot electrons, after having their momenta re-directed, have to travel vertically to the Si-SiO_2 interface, without suffering any other collisions, in order to be injected into the gate oxide. The probability of collision-free travel to the barrier peak, $P(E_{OX})$ is defined as the product of P_1 and P_2, where P_1 is the probability factor weighted by the electron concentration in the inversion layer and P_2 is the probability factor of the scattering in the oxide image-potential well. $P(E_{OX})$ is approximated by [52]

$$P(E_{OX}) \approx \left[\frac{5.66\times10^{-6} E_{OX}}{\left(1+\frac{E_{OX}}{1.45\times10^{5}}\right)} \times \frac{1}{\left(1+\frac{2\times10^{-3}}{L_{eff}} e^{(-E_{OX}X_{OX}/1.5)}\right)} + 2.5\times10^{-2} \right] e^{(-300/\sqrt{E_{OX}})} \qquad (2\text{-}19)$$

for $E_{OX} \geq 0$ and

$$P(E_{OX}) \approx 2.5\times10^{-2} e^{(-X_{OX}/l_{OX})} \qquad (2\text{-}20)$$

for $E_{OX} < 0$.

where X_{OX} is the gate oxide thickness.

The gate current I_{gate} can be expressed in terms of the probability for each individual event to occur, and is described as [50],

$$I_{gate} = 0.25\frac{l^2 E_m^3 I_{ds} P(E_{OX}\mid_L)}{l_r \Phi_b^2 (dE_x/dx)\mid_L} e^{-(\Phi_b / E_m l)} \approx 0.5\times\frac{I_{ds} X_{OX}}{l_r}\left(\frac{l E_m}{\Phi_b}\right)^2 P(E_{OX}\mid_L) e^{-(\Phi_b / E_m l)} \quad (2\text{-}21)$$

where E_m is the channel electric field at the drain end, L is the length of the channel and λ_r is the re-direction scattering mean free path.

Chapter 3 Design of the Proposed E-S/D MOSFET

As the MOSFET size shrinks to deep submicron regime, E-S/D MOSFETs have been received more attention because it has many advantages over the conventional MOSFETs. It is widely studied for overcoming the limitation of the conventional MOSFETs. Although the E-S/D MOSFET seems to be attractive for the deep submicron devices, there still exist a lot of problems to be solved. The main issue of the E-S/D MOSFET can be summarized as follows:

In the fabrication point of view, there have been a lot of fabrication methods proposed [12-25] but there are still confusion and the prevailing methods are still in the development stage. The complexity and the cost of the process are also critical issues for the development of the E-S/D MOSFET process. And the self-alignment problem exists because it is difficult to align the poly-Si gate on the recessed channel precisely [19]. Furthermore, it would be favorable if the process compatibility should be offered for the dual poly MOSFET technologies. In the performance point of view, the tradeoff relationship between the device performance and the short channel effect should be enhanced compared to that of the conventional LDD MOSFETs. In other words, the device performance should be improved without aggravating the short channel behaviors. Minimizing the parasitic resistance and the junction capacitance should be also carefully considered.

The proposed E-S/D MOSFET is designed to take into account the issues stated above. In the fabrication method, emphasis on the self-alignment and simplified fabrication process are made. In respect of performance,

minimizing the parasitic series resistance and the junction capacitance are considered without aggravating the short channel behaviors.

3.1 Fabrication Steps for the Proposed E-S/D MOSFET

The main fabrication steps for the proposed E-S/D MOSFET are summarized in Fig. 3-1 and schematically shown in Fig. 3-2. Two-dimensional process simulator TSUPREM-4 is used for the simulations [53]. After the mask oxidation on p-type (100) silicon wafer, the channel region is opened by dry-etching [15]. Silicon surface is etched to the depth of X_R. B^+ ($4\times10^{12}cm^{-2}$, 45keV) and BF_2^+ ($6\times10^{12}cm^{-2}$, 90keV) implantations are performed for punchthrough prevention and threshold voltage adjustment, respectively. The implanted ions are blocked by the mask oxide, resulting in the selectively doped channel [17-20]. Nitride is deposited and etched to form inverted sidewall spacers which have the width of W_S. These structural parameters (X_R and W_S) have powerful influence on the device characteristics such as short-channel effects and driving capabilities because they determine the shape of the SDE regions. In this work, W_S and X_R are selected 15nm and 30nm respectively to effectively suppress the short-channel effects. 50Å gate oxide is grown. Poly-Si is deposited and etched until the mask oxide reveals. After etching all of the mask oxide, As^+ ($5\times10^{14}cm^{-2}$, 25keV, 30° tilt) implantation is performed for the SDE regions. Large-angle-tilted implantation [54] is performed to guarantee the sufficient gate-to-drain overlap area. After the formation of 65nm thick 2nd nitride sidewall, which results in the final nitride sidewall spacer thickness of 80nm, As^+ ($5\times10^{15}cm^{-2}$, 20keV) implantation is

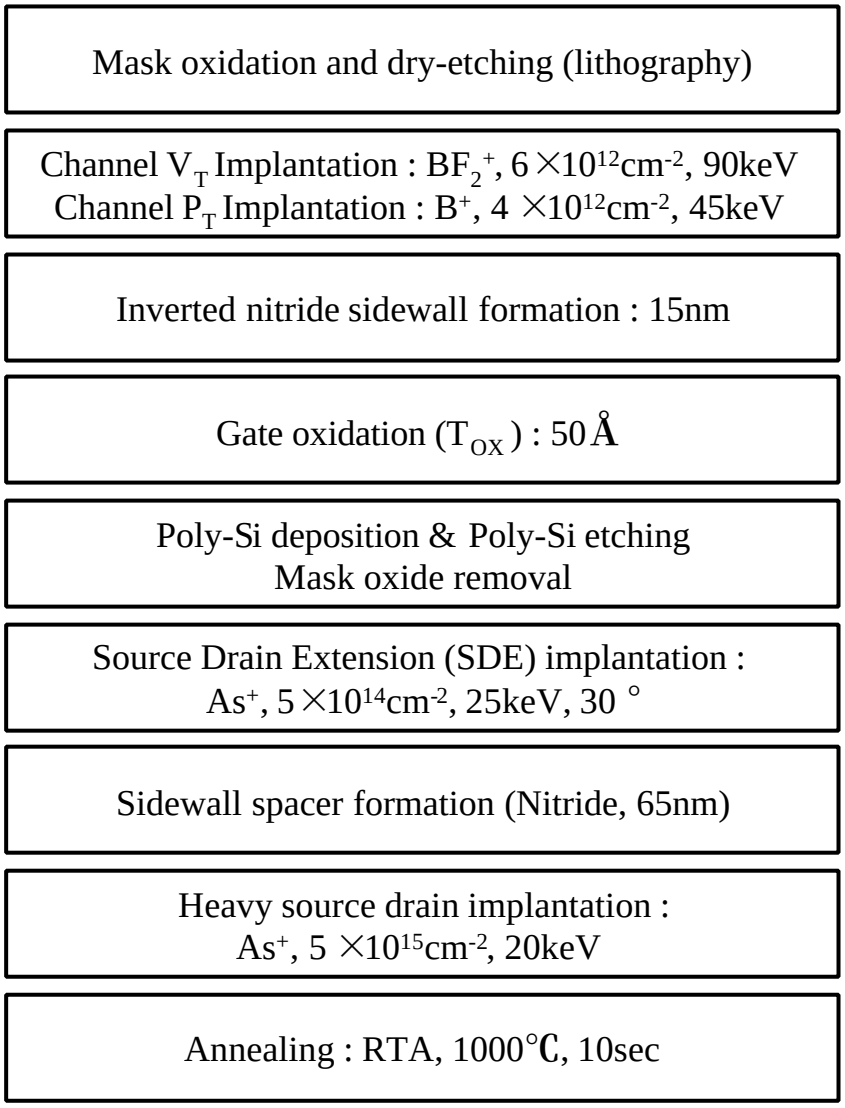


Fig. 3-1. Main fabrication steps for the proposed E-S/D MOSFET.

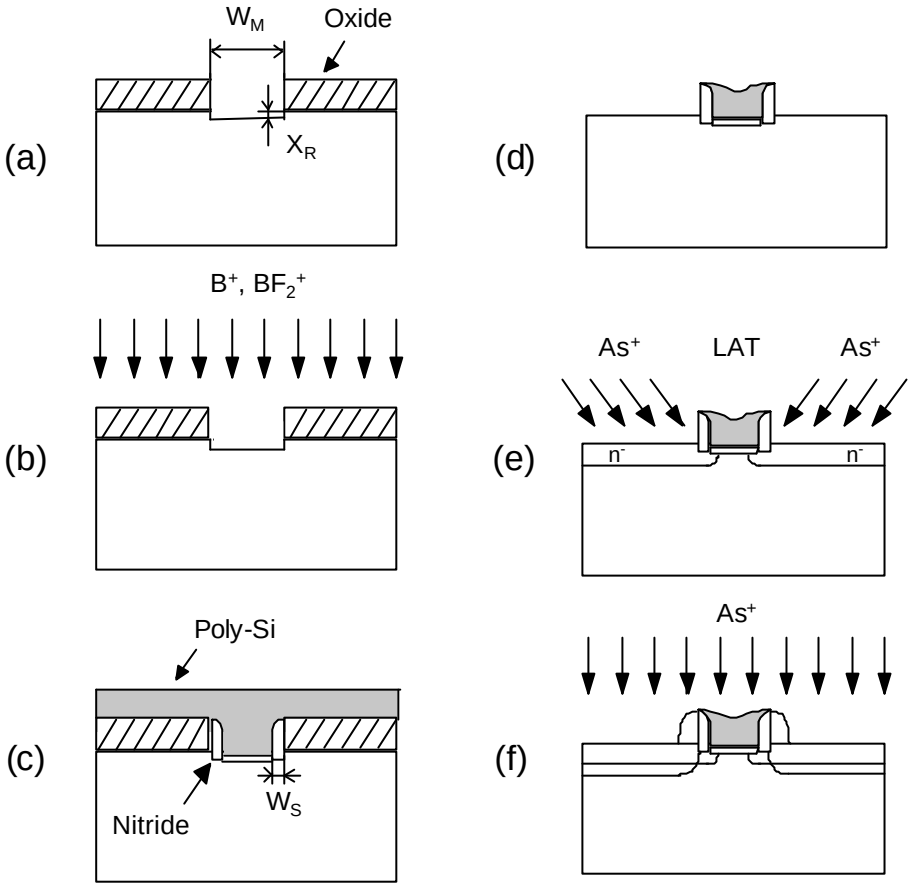


Fig. 3-2. Fabrication steps for the proposed E-S/D MOSFET. (a) mask oxidation and dry etching (b) selective channel implantations (c) nitride sidewall formation and poly-Si deposition (d) poly-Si etching and mask oxide removal (e) large-angle-tilted (LAT) SDE implantation (f) n^+ source/drain implantation.

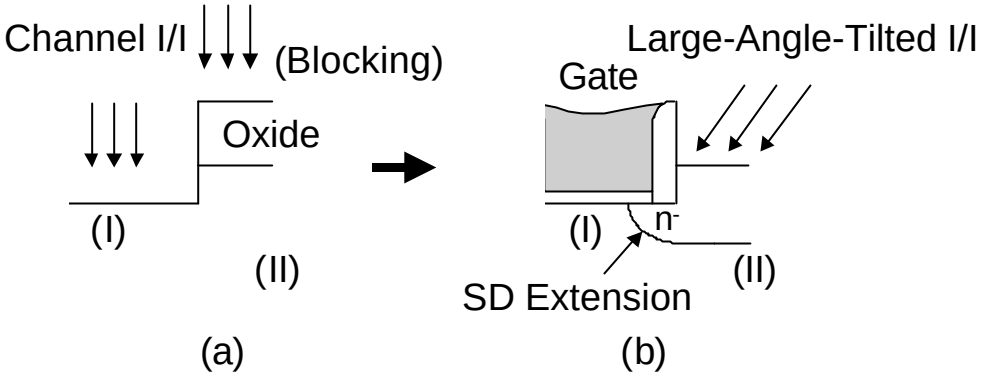


Fig. 3-3. Channel implantation and SDE implantation steps for the proposed structure. (a) Selective channel implantation: Region (I): reduced lateral electric field at drain edge. Region (II): reduced junction capacitance. (b) Elevated SDE region: relatively high energy large-angle-tilted implantation for n^- region.

performed for the heavy source/drain regions. RTA is done at 1000℃ for 10s.

The proposed structure has several advantages. First, the self-aligned poly-Si gate is formed by the inverted sidewall spacers so that self-alignment is realized for both source/drain and gate regions on the recessed channel [20]. Since the definition of the poly gate needs only one lithography step, fabrication steps are simplified and can be easily adopted for the dual gate MOSFET technologies. Secondly, the proposed structure has the selectively doped channel profile as a result of channel implantation as shown in Fig. 3-3(a). With this profile, the junction capacitance is reduced as the doping concentration at the bottom of the drain region (II) is minimized. Thirdly, the proposed structure has elevated SDE regions so that low-energy ion implantation can be avoided. It should be pointed out that although there have

been many E-S/D MOSFETs reported, most of the E-S/D structures have failed to notice the importance about the elevation of the source drain extension region. A lot of E-S/D MOSFETs have nearly the same source drain extension structures as those of conventional LDD MOSFETs. As shown in Fig. 3-3(b), relatively high energy (25keV) implantation is used by help of large-angle-tilted implantation.

The final device cross section is schematically shown in Fig. 3-4. The recessed channel depth is 30nm and the inverted sidewall width is 15nm, respectively. The self-aligned gate is formed by use of the inverted sidewall spacers. Second nitride spacers (65nm) are deposited to form the final sidewall thickness of 80nm. Source drain extension region is formed by help of large-angle-tilted implantations. Since the proposed E-S/D MOSFET requires only one lithography step for the definition of the gate and the recessed channel area, the fabrication process is simple and self-aligned. The selectively doped channel region is formed in region (I) and the region (II) is not affected by the channel implantations. The simulated subthreshold characteristics of the E-S/D MOSFET are shown in Fig. 3-5. Two-dimensional device simulator, MEDICI [55] is used for the simulation. The effective channel length is 0.154 μm. As shown in the figure, the drain induced barrier lowering (DIBL) is defined as $\triangle V_{TH}=V_{TH}(V_{DS}=0.1V)-V_{TH}(V_{DS}=V_{DD})$. The subthreshold swing of the device is approximately 80mV/dec. There seems no sign of device punchthrough phenomenon.

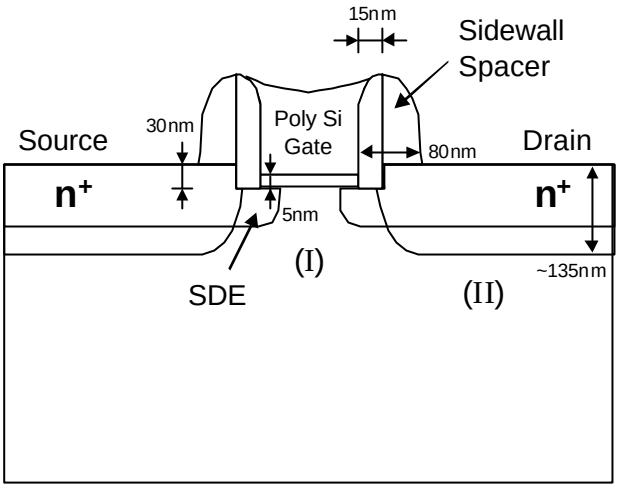


Fig. 3-4. Cross sectional schematic of the proposed E-S/D structure. Nitride sidewall spacers are formed twice resulting in the final thickness of 80nm.

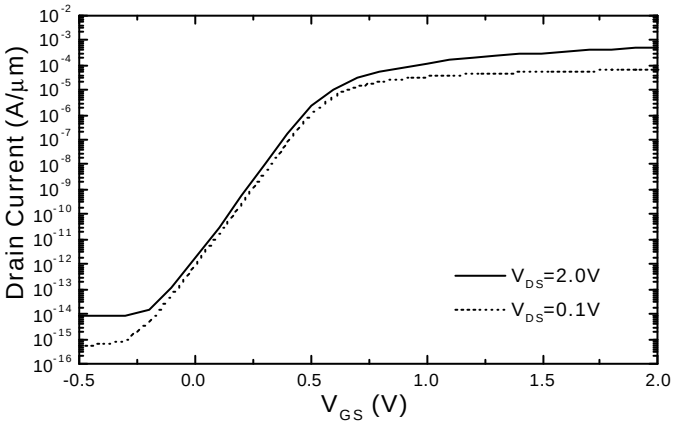


Fig. 3-5. Subthreshold characteristics of the proposed E-S/D MOSFET.

L_{EFF}=0.154 ㎛, SS≅80mV/dec.

3.2 Design of the Recessed Channel Structure

The short channel effects in the proposed E-S/D MOSFET are mainly determined by the feature of recessed channel structure. The shape of the recessed channel structure can be described by the recessed channel depth (X_R) and the sidewall spacer width (W_S). Figure 3-6 shows the relationship between X_R and W_S for a given source drain implantation condition. To explain the relationship between X_R and W_S in Fig. 3-6, some assumptions are made as follows: The poly gate lengths (L_{POLY}) are fixed regardless of X_R and W_S. The effective channel lengths (L_{EFF}) should have the same value regardless of X_R and W_S. The junction depths (X_{J2}) are the same because the source drain implantation conditions are the same.

To satisfy such assumptions, X_R and W_S should be inversely proportional to each other. This relationship is illustrated in Fig. 3-6. The width of the recessed region (W_R), which is determined in the lithography step, is a varying value according to X_R and W_S conditions. It can be simply expressed as $W_R = L_{POLY} + 2 \times W_S$. From this result, it can be seen that the proposed structure has benefit in the lithography step. To explain it more in detail, in case of the conventional LDD MOSFET, the minimum poly gate length is determined by the resolution of lithography. However, the proposed structure adds additional margins of ($2 \times W_S$) for the lithography step.

To determine the X_R and W_S, short channel characteristics should be considered. Figure 3-7 and 3-8 show the threshold voltage roll-off and the drain induced barrier lowering (DIBL) characteristics of proposed E-S/D MOSFET for some combinations of the X_R and W_S. DIBL is defined as $\triangle$

$V_{TH}=V_{TH}(V_{DS}=0.1V)-V_{TH}(V_{DS}=2.0V)$. The simulations are done for 1) W_S=10nm, X_R=45nm, 2) W_S=15nm, X_R=35nm, 3) W_S=20nm, X_R=25nm, 4) W_S=25nm, X_R=15nm, respectively. To maintain approximately the same effective channel length, X_R is decreased as W_S is increased. The As^+ ($5\times10^{14}cm^{-2}$, 25keV, 30°) implantation condition for SDE is fixed for all cases. This means that the junction depths (X_{J2} in Fig. 3-6) of SDE are the same for all cases. The threshold voltage roll-off characteristics and the DIBL characteristics worsen as W_S is increased (X_R is decreased). As W_S increases, the junction depth (X_{J1} in Fig. 3-6) of SDE is also increased resulting in the poor short channel behaviors. Figure 3-9 shows the I_{DSAT} characteristics of proposed E-S/D MOSFET for some combinations of X_R and W_S. I_{DSAT} is selected for $V_{DS}=V_{GS}-V_T=2.0V$. The I_{DSAT} is increased as W_S is increased (X_R is decreased). Furthermore, if $W_S \gg X_R$, the SDE region nearly has the form of single drain MOSFET.

From these results, it can be seen that there exist tradeoff relationships between the short channel effects and the driving capability according to W_S and X_R. Thus W_S and X_R should be selected within the range of their respective design window. In the thesis work, W_S and X_R are selected 15nm and 30nm respectively.

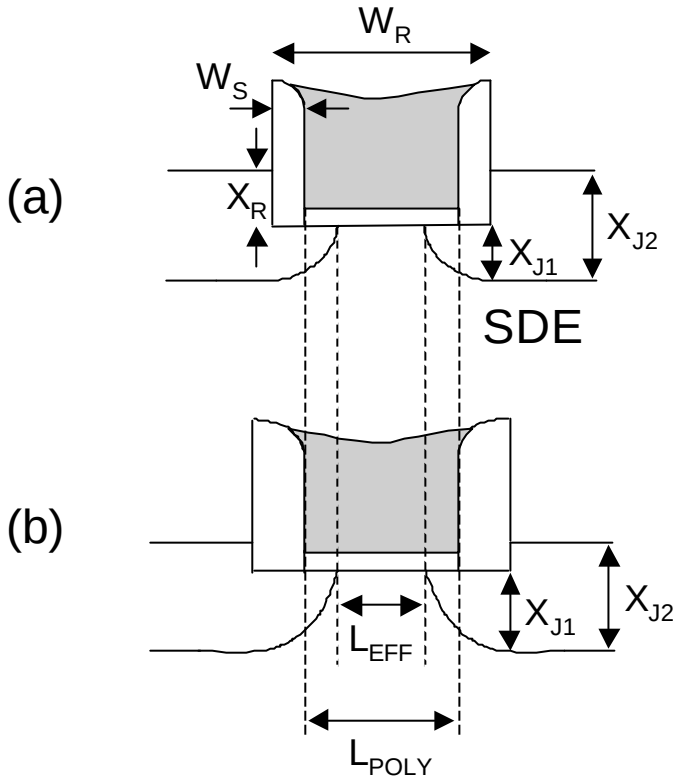


Fig. 3-6. The relationship between X_R and W_S for a given source drain implantation condition.

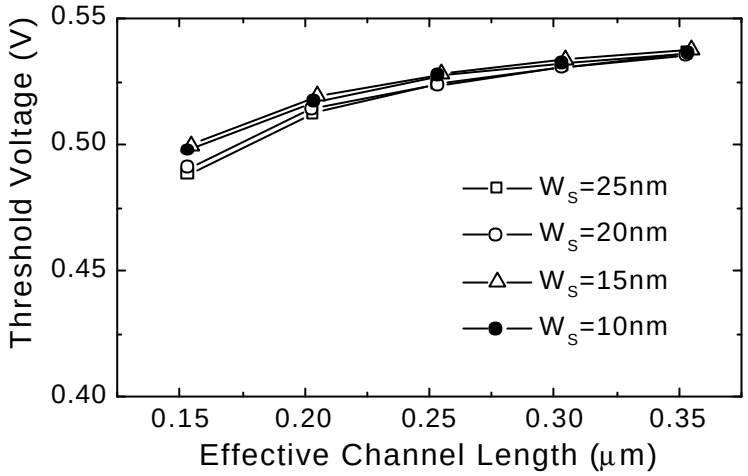


Fig. 3-7. Threshold voltage roll-off characteristics of proposed E-S/D MOSFETs according to W_S.

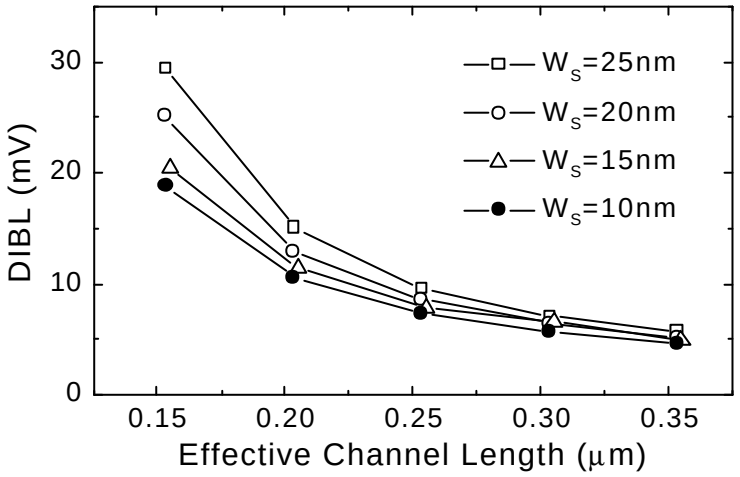


Fig. 3-8. DIBL characteristics of proposed E-S/D MOSFETs according to W_S.

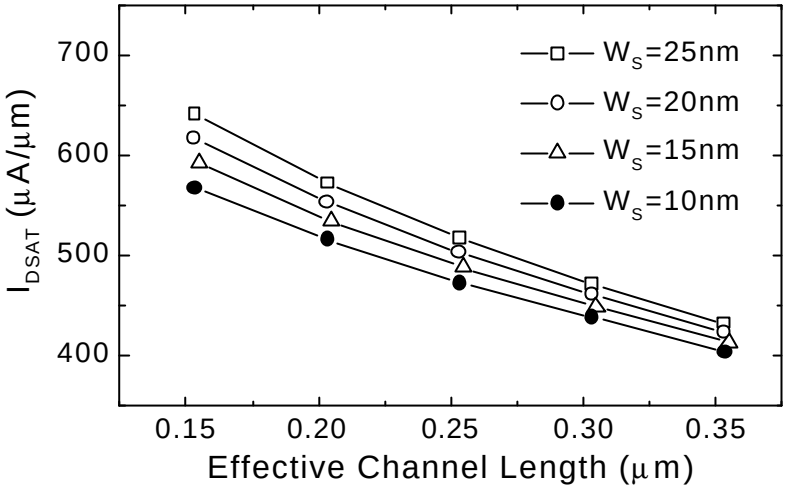


Fig. 3-9. I_{DSAT} characteristics of proposed E-S/D MOSFETs according to W_S.

3.3 Large-Angle-Tilted Implantation for Source Drain Extension

For the source drain extension (SDE) implantation, the proposed E-S/D MOSFET make use of the large-angle-tilted implantation technique. Since the proposed structure has inverted sidewall spacers inside the recessed channel, implanted dopants should laterally diffuse to the area beneath the poly gate. If the inverted sidewall width increases, the lateral diffusion of dopants should be increased more further. However, to guarantee the sufficient gate to drain overlap area for the SDE region, the junction depth is also increased at the same time resulting in the degradation of the short channel effect. Such relationship can be relieved by use of large-angle-tilted implantation technique.

Figure 3-10 shows the schematic cross sectional view of the SDE region according to the large-angle-tilted implantations. By increasing the angle θ, sufficient gate to drain overlap area can be more easily achieved and the junction depth is also decreased. Figure 3-11 shows the DIBL characteristics according to the tilt angle, *q*. The target of effective channel length is fixed to 0.154μm and 0.133μm, respectively. To meet the effective channel length conditions, if the tilt angle (*q*) is determined, then the implantation energy is also determined. It is shown that the DIBL is degraded as the tilt angle is increased from 0 to 20°. As there exists nitride spacer at the corner of the recessed channel, the shape of SDE region can be affected by the large-angle-tilted implantations deteriorating the short channel characteristics. However, the DIBL is decreased when the tilt angle is increased from 20° to 45°. It is mainly due to the reduced junction depth that is also indicated in Fig. 3-10. Since the driving current is also decreased as tilt angle is increased, the tilt angle should be selected considering the short channel effects and the driving capability. In this work, tilt angle of 30° and implantation energy of 25keV are selected.

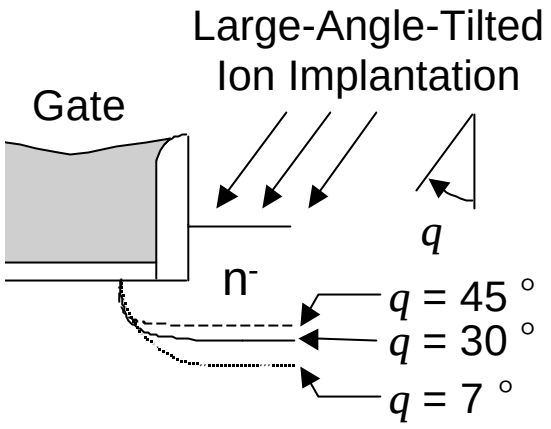


Fig. 3-10. Determination of SDE junction according to the various angle conditions of large-angle-tilted ion implantations.

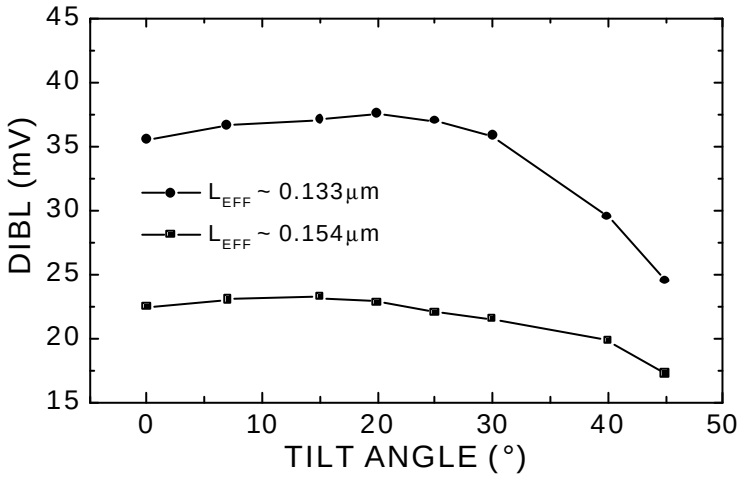


Fig. 3-11. DIBL characteristics as a function of tilt angle, *q*. The target of L_{EFF} is fixed to 0.133 and 0.154μm, respectively.

3.4 Selectively Doped Channel Structure

The proposed E-S/D MOSFET has selectively doped channel region compared with that of conventional MOSFETs [17-20]. In the proposed MOSFET, only the channel area is exposed to air and the rest of the silicon wafer is covered with the thick blocking oxide layer during the channel implantations. As a result, the channel implantation is implemented only through the exposed silicon area. Figure 3-12 shows the doping profile difference between the uniformly doped channel structure and the selectively doped channel structure.

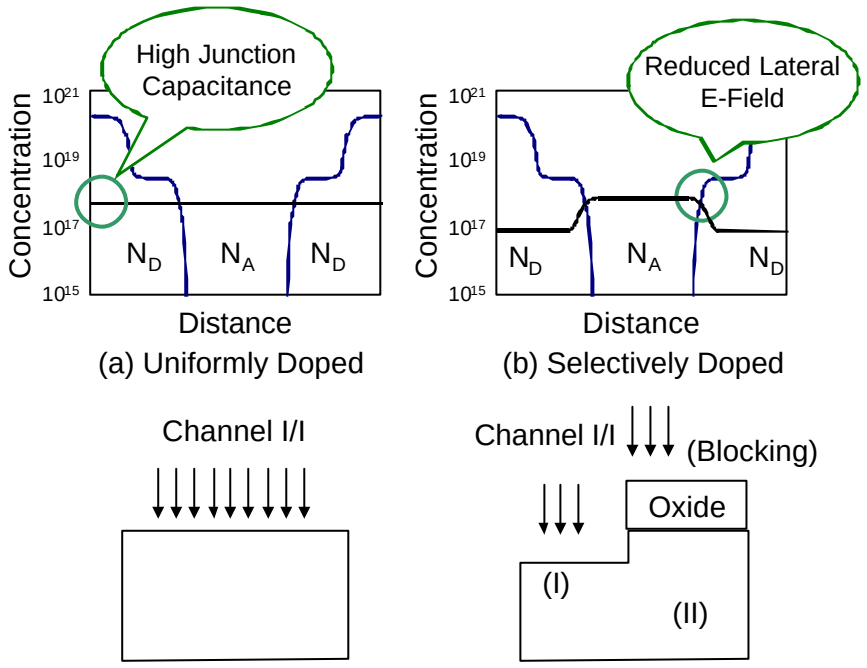


Fig. 3-12. Doping profile difference between uniformly doped and selectively doped channel structure. In the selectively doped channel, the thick oxide layer acts as a blocking material during the implantations.

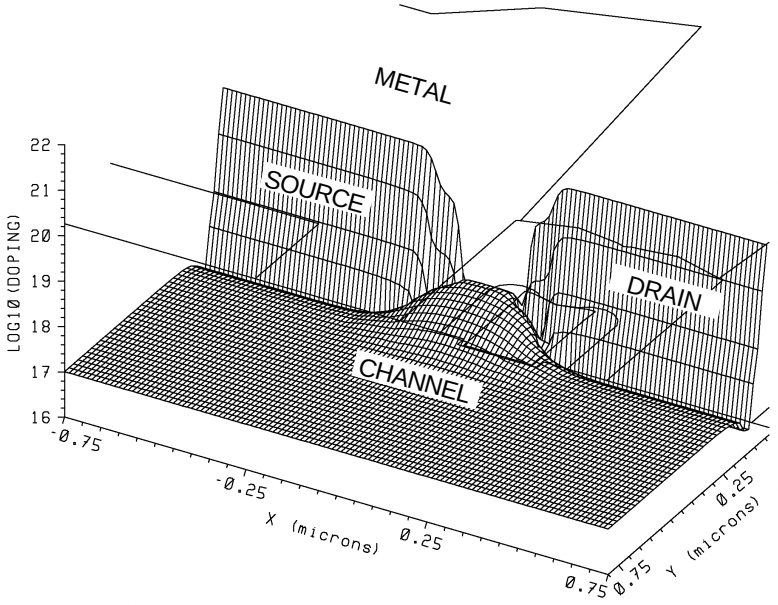


Fig. 3-13. Three-dimensional projection plot of the doping concentration for the proposed E-S/D MOSFET.

Figure 3-13 shows the three-dimensional projection plot of the doping concentration for the proposed E-S/D MOSFET. The effective channel length is approximately 0.15 μm. Unlike the conventional MOSFETs, the channel implantations are performed selectively in the channel region. Thus the doping concentration beneath the heavy source/drain region is not affected by the channel implantations.

The junction capacitance (C_J) between source/drain and substrate can be treated as asymmetrically doped p-n junction. That is, the depletion region extends primarily into the less heavily doped side (substrate side). Thus the C_J

is determined by only one of the doping concentrations [56]. For a p^+-n junction, $N_a \gg N_d$ and C_J is proportional to $N_d^{1/2}$. For a n^+-p junction, $N_a \ll N_d$ and C_J is proportional to $N_a^{1/2}$, where N_d is the doping concentration of the donor ions and N_a is the doping concentration of the acceptor ions.

From Fig. 3-12, it can be seen that the junction capacitance of uniformly doped structure is directly related to the channel doping concentrations. As the MOSFETs have been scaled down to deep submicron regime, the doping concentration of channel region should be increased in order to suppress the short channel effects. Consequently, the uniformly doped channel structure suffers from increased junction capacitance problem deteriorating the device performance. On the contrary, the selectively doped channel structure has reduced junction capacitance because the doping concentration beneath the source/drain is not affected by the channel implantations.

To investigate the effect of selectively doped channel on the electric field, the proposed E-S/D structures with different channel doping profiles are analyzed. As previously described in the fabrication process (Figs. 3-1 and 3-2), the proposed structure make use of nitride sidewall spacers for the inverted sidewall spacers. The nitride sidewall can be selectively removed by particular solution such as H_3PO_4. Note that the thick blocking oxide layer is not removed during the process. By utilizing such properties, different selectively doped channel profiles can be achieved. Figure 3-14 shows the process for achieving the different channel profiles. Note that the fabrication process is modified compared with that of Fig. 3-2. In Fig. 3-14, the inverted sidewall spacers are formed prior to the channel implantations. W_{RN} is the width of removable nitride spacer and W_S is the width of final nitride spacer. If W_{RN} is

kept larger than W_S, more selectively doped channel can be achieved. On the contrary, if W_{RN} is smaller than W_S, channel doping profile tends to be more like that of the uniformly doped case. In the simulations, W_{RN} values are selected 35nm, 25nm and 15nm, respectively. Figure 3-15 shows the two dimensional electric field contours of the proposed E-S/D MOSFETs according to W_{RN}. The contours of electric field are plotted from 0.22MV/cm in steps of 0.05MV/cm for a drain bias of 2.5V. V_{GS}=1.3V for the worst case conditions and L_{EFF}=0.154μm. As W_{RN} is increased, it can be seen that the magnitude of the electric field is decreased. However, the selection of W_{RN} should be carefully determined considering the width of recessed channel region (W_R). Since the channel implantation is performed through the open area (W_R-2W_{RN}), the decreased ratio of (W_R-2W_{RN})/W_R can aggravate the punchthrough phenomenon due to the insufficient channel implantations. As the device shrinks to deep submicron region, W_R is also scaled down proportional to the respective channel length. If W_{RN} is kept the same value regardless of the channel lengths, the ratio of (W_R-2W_{RN})/W_R eventually becomes too small causing the short channel problems. To prevent such deterioration of the short channel effects, the W_{RN} should also be adjusted for the respective channel lengths. Consequently, although the selectively doped channel is advantageous for reducing the lateral electric field in the drain side, short channel characteristics should also be carefully considered.

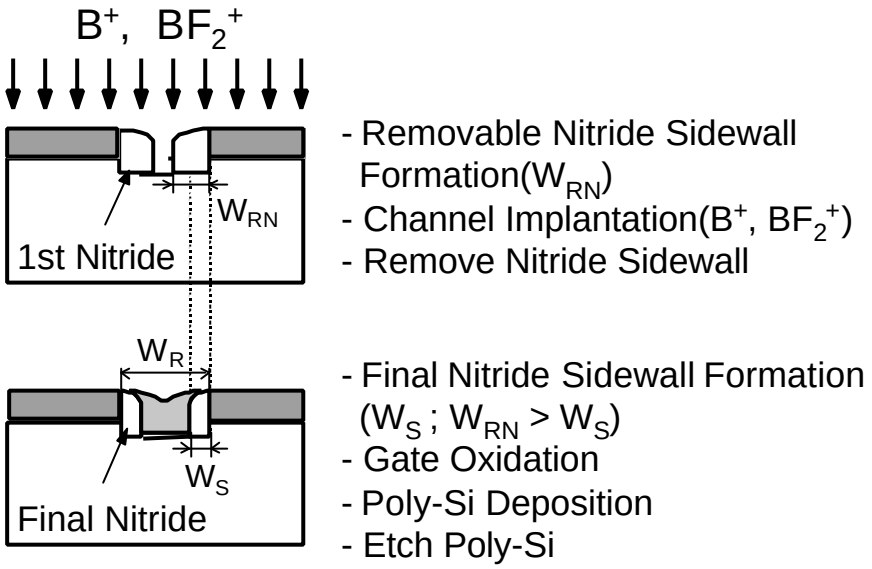


Fig. 3-14. The process for achieving different channel profiles. Removable nitride sidewall spacers are used.

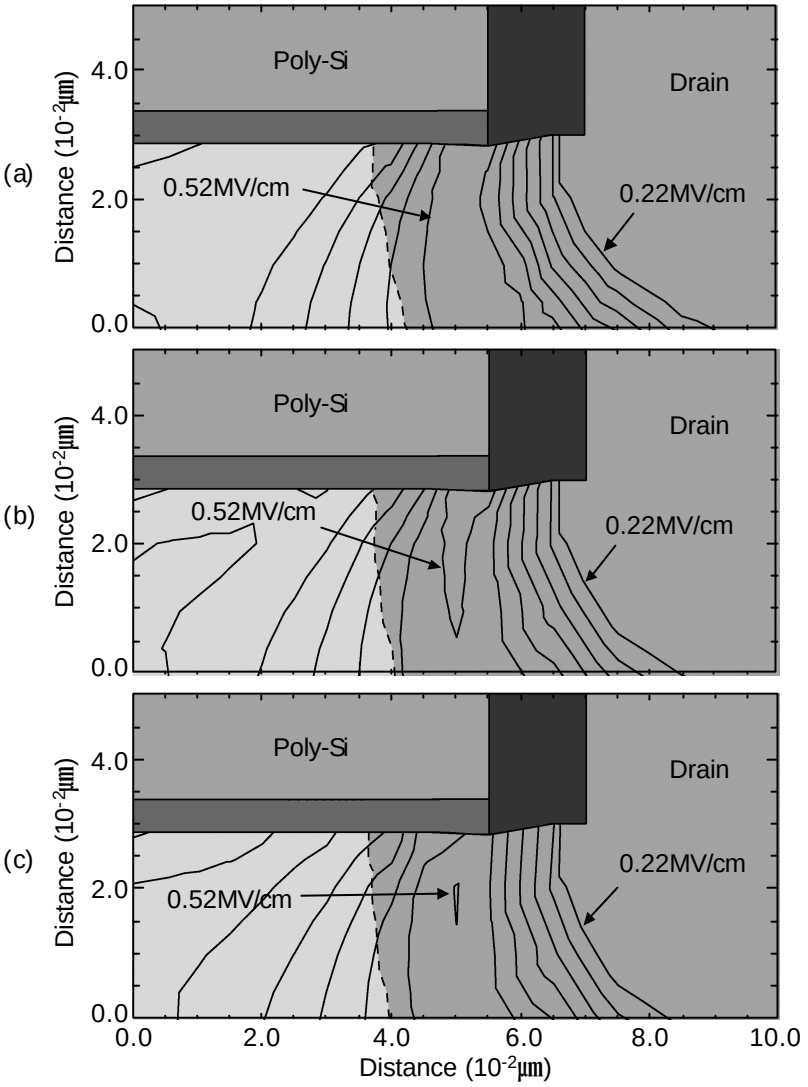


Fig. 3-15. Two-dimensional electric field contours for the proposed E-S/D MOSFETs. V_{DS}=2.5V, V_{GS}=1.3V. L_{EFF}=0.154μm, (a) W_{RN}=15nm, (b) W_{RN}=25nm and (c) W_{RN}=35nm.

Chapter 4 Results and Discussion

In this chapter, the electrical characteristics of proposed E-S/D MOSFET are extensively investigated. Conventional LDD and SEG MOSFETs are also analyzed for comparison and discussion. For the analysis, two dimensional process and device simulators TSUPREM-4 and MEDICI are used [53],[55].

4.1 Models Used in the Simulations

Some of important models are described that were used for the device simulations. Incomplete ionization effect, band-to-band tunneling, mobility models are described more in detail.

4.1.1 Incomplete Ionization of the Impurities

The impurities are implanted to form n or p type semiconductors. Usually, it is assumed that all the implanted impurities are fully ionized during the device simulations. However the ionized donor density (N_D^+) and the ionized acceptor density (N_A^-) has dependence on temperature. According to [57], the dependence are modeled using Fermi-Dirac statistics with the appropriate factors for conduction and valence band degeneracy and with the introduction of quasi-Fermi levels for electrons and holes. N_D^+ and N_A^- can be described as [55], [57]

$$N_D^+ = \frac{N_D}{1 + GCB \exp\left(\frac{E_{Fn} - E_D}{kT}\right)} \quad (4\text{-}1)$$

$$N_A^- = \frac{N_A}{1 + GVB \exp\left(\frac{E_A - E_{Fp}}{kT}\right)} \quad (4\text{-}2)$$

where

N_D : net compensated n-type doping.

N_A : net compensated p-type doping.

E_A : acceptor impurity level.

E_D : donor impurity level.

E_{Fn} : electron quasi-Fermi level

E_{Fp} : hole quasi-Fermi level

GCB : degeneracy factors for the conduction bands.

GVB : degeneracy factors for the valence bands.

In the MEDICI [55] models, the incomplete ionization of impurities are modeled based on the equations stated above. By default, GCB and GVB are selected 2 and 4 for the silicon devices. And $E_D=E_C$-EDB and E_A=EAB+E_V. Where EDB is the donor ionization energy referenced to the conduction band energy and EAB is the acceptor ionization energy referenced to the valence band energy. By default EDB and EAB are selected 0.044eV and 0.045eV for the silicon devices. Fig. 4-1 shows the I_{DS}-V_{DS} characteristics of a sample E-S/D MOSFET with fully ionized case and incomplete ionized case.

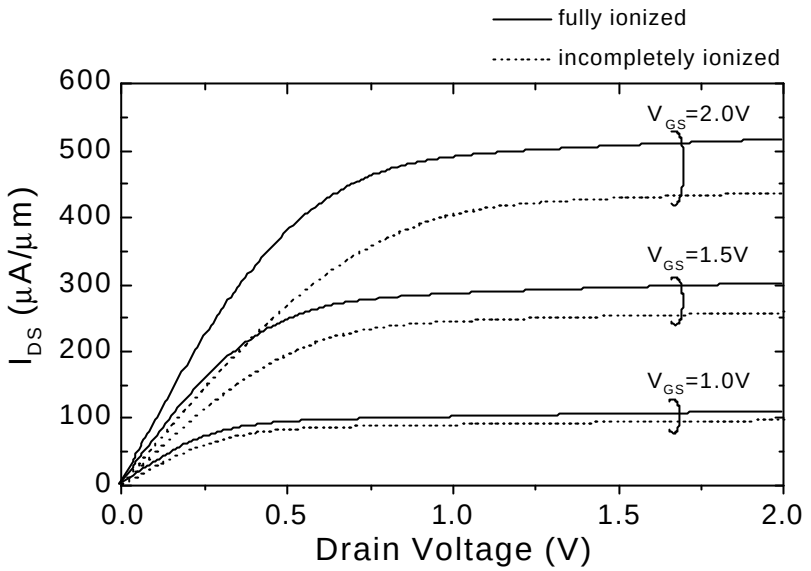


Fig. 4-1. I_{DS}-V_{DS} characteristics of a sample E-S/D MOSFET. The solid line and the dashed line indicate the cases when fully ionization of the impurities and incomplete ionization are assumed.

4.1.2 Band-to-Band Tunneling Model

The phenomenon of a valence band electron tunneling through the forbidden energy gap to the conduction band is known as band-to-band tunneling. It occurs in regions of high electric field where the local band bending causes the tunneling probability to become significant. In the model used by simulation has the form [55],

$$G^{BB} = A.BTBT \frac{E^2}{E_g^{1/2}} \cdot \exp\left(- B.BTBT \frac{E_g^{3/2}}{E} \right) \qquad (4\text{-}3)$$

where,

A.BTBT = 3.5×10^{21} $eV^{1/2}/cm\text{-}s\text{-}V^2$

B.BTBT= 22.5×10^{6} $V/cm\text{-}(eV)^{3/2}$

4.1.3 Mobility Models

In the simulations, Lombardi surface mobility model is used which is an empirical model that combines mobility expressions for semiconductor-insulator interfaces and for bulk silicon [58]. The basic equation is given by Mathiessen's rule:

$$m_S = \left[\frac{1}{m_{ac}} + \frac{1}{m_b} + \frac{1}{m_{sr}} \right]^{-1} \qquad (4\text{-}4)$$

where

μ_S : total electron or hole mobility accounting for surface effects

μ_{ac} : mobility degraded by surface acoustical phonon scattering

μ_b : mobility in bulk silicon

μ_{sr} : mobility degraded by surface roughness scattering.

For the parallel mobility calculations, Caughey-Thomas Expression for both electron and hole mobility is used [59]. This model can account for

effects due to high electric field in the direction of current flow. In this model, the carrier drift velocity saturates at high fields. The model can be described as,

$$\mu_n = \frac{\mu_{S,n}}{\left[1+\left(\frac{\mu_{S,n}E_{||,n}}{v_n^{sat}}\right)^{\mathbf{BETAN}}\right]^{1/\mathbf{BETAN}}} \tag{4-5}$$

$$\mu_p = \frac{\mu_{S,p}}{\left[1+\left(\frac{\mu_{S,p}E_{||,p}}{v_p^{sat}}\right)^{\mathbf{BETAP}}\right]^{1/\mathbf{BETAP}}} \tag{4-6}$$

where $\mu_{S,n}$ and $\mu_{S,p}$ are the low field mobilities and v_n^{sat} and v_p^{sat} are the saturation velocities for electrons and holes, respectively. $E_{||}$ is the component of electric field paralled to the current direction. EBETAN and BETAP are the fitting parameters that can be obtained from the experimental data taken in the appropriate experimental conditions. Values for v_n^{sat} and v_p^{sat} are computed by default from the following expression. In these simulations BETAN=2.0, BETAP=1.0, $v_n^{sat}=1.035\times10^7$cm/s, and $v_p^{sat}=1.035\times10^7$cm/s are selected for the silicon material [55].

$$v_{n,p}^{sat}(T) = \frac{2.4\times10^7}{1+0.8\cdot\exp\left(\frac{T}{600}\right)} \tag{4-7}$$

4.2 Design of Conventional LDD MOSFET

Conventional n-channel LDD MOSFETs with varying doping concentration are analyzed in comparison with the proposed E-S/D MOSFET. HL, ML and LL represent LDD MOSFETs with SDE implantation dose of $5\times10^{14}cm^{-2}$, $1\times10^{14}cm^{-2}$, $5\times10^{13}cm^{-2}$, respectively. Very low acceleration energy of 10keV is used for the SDE implantation. The main fabrication steps for the conventional LDD MOSFETs are shown in Fig. 4-2. The SDE implantation is performed after the formation of a thin offset spacer. By varying the thickness of the offset spacer, the effective channel length can be adjusted to have the same value regardless of the SDE implantation dose as shown in Fig. 4-3. The nitride sidewall is formed to have final sidewall thickness of 80nm. After the final sidewall formation, As^+ ($5\times10^{15}cm^{-2}$, 20keV) implantation is performed for n^+ source/drain regions [60]. The process conditions are kept the same to those of the E-S/D MOSFETs for fair comparison. The detailed process conditions are listed in Table 4-1. For the analysis of their electrical characteristics, two-dimensional process simulator TSUPREM-4 [53] and device simulator MEDICI [55] are used.

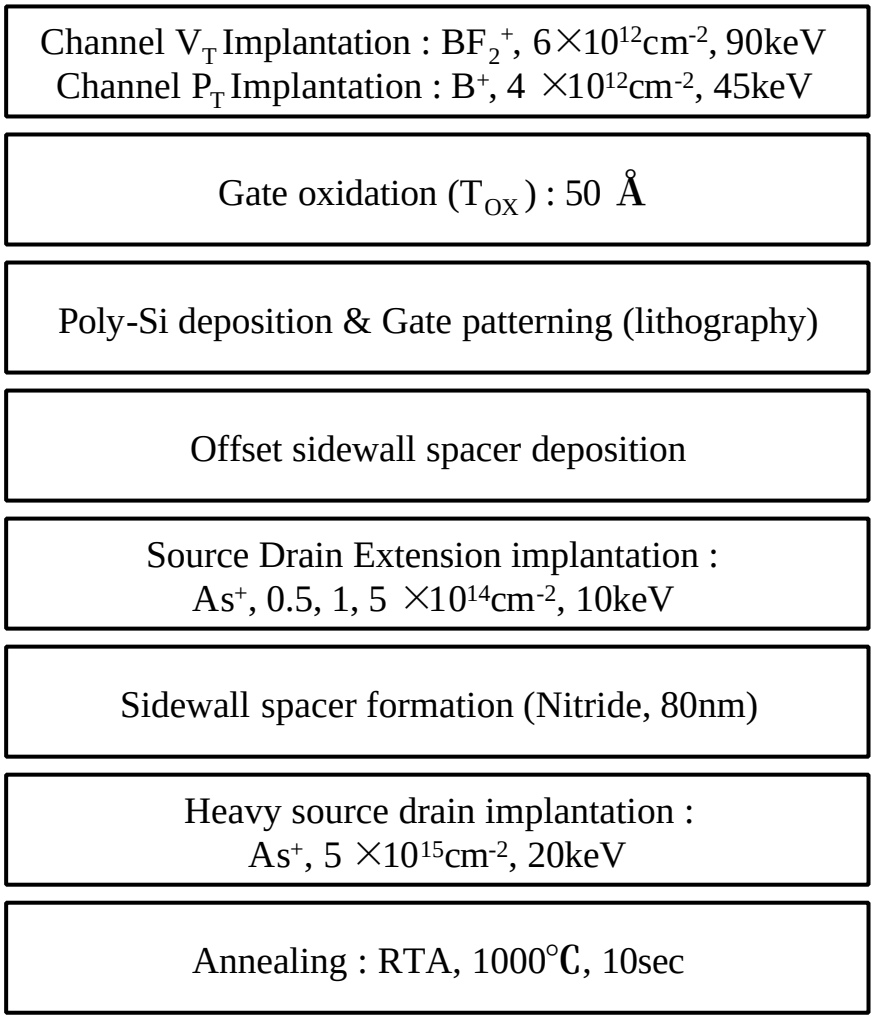


Fig. 4-2. Main fabrication steps of the conventional LDD MOSFETs.

Table 4-1. Process parameters of the conventional LDD MOSFETs.

Process Parameter	**HL**	**ML**	**LL**
Channel Implantation	B^+, 4×10^{12}, 45keV BF_2^+, 6×10^{12}, 90keV		
Gate Oxide Thickness (T_{OX})	50Å		
Offset Sidewall Width (W_{OFF})	15nm	7.5nm	5nm
SDE Implanatation	$5\times10^{14}cm^{-2}$	$1\times10^{14}cm^{-2}$	$5\times10^{13}cm^{-2}$
Final Sidewall Width (W_S)	80nm		
Poly Gate Length (L_{POLY})	0.19μm		
Effective Channel Length	0.1542μm	0.1541μm	0.1541μm
Annealing	1000℃, 10sec		

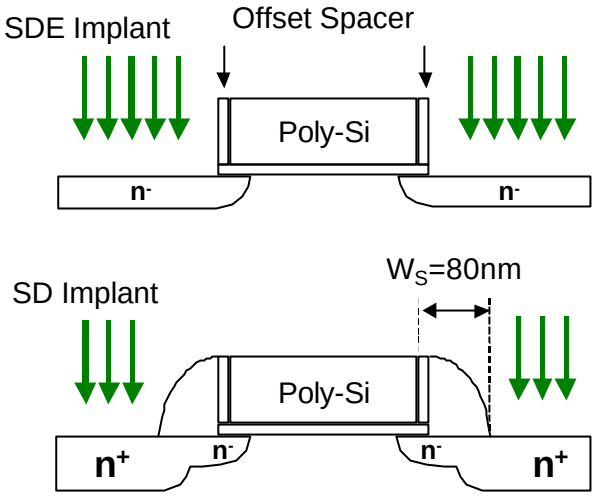


Fig. 4-3. Control of the effective channel length by help of the offset spacer in LDD MOSFET.

4.3 GIDL Characteristics of E-S/D and LDD MOSFETs

The Gate-Induced Drain Leakage (GIDL) current is one of major leakage current observed in off-state MOSFETs. The influence of SDE dose on the GIDL characteristics are analyzed. Figure 4-4 shows the GIDL characteristics of the LDD MOSFETs according to the SDE dose. The GIDL current is obtained from MEDICI simulation that includes band-to-band tunneling effect [28]. LL1 and LL2 represent LDD MOSFETs with SDE implantation dose of $3\times10^{13}cm^{-2}$, $1\times10^{13}cm^{-2}$, respectively. As reported by Y-H Kim *et al.*[28], increment of the SDE implantation dose increases the GIDL current due to the increased maximum electric field. It is shown that the GIDL current is

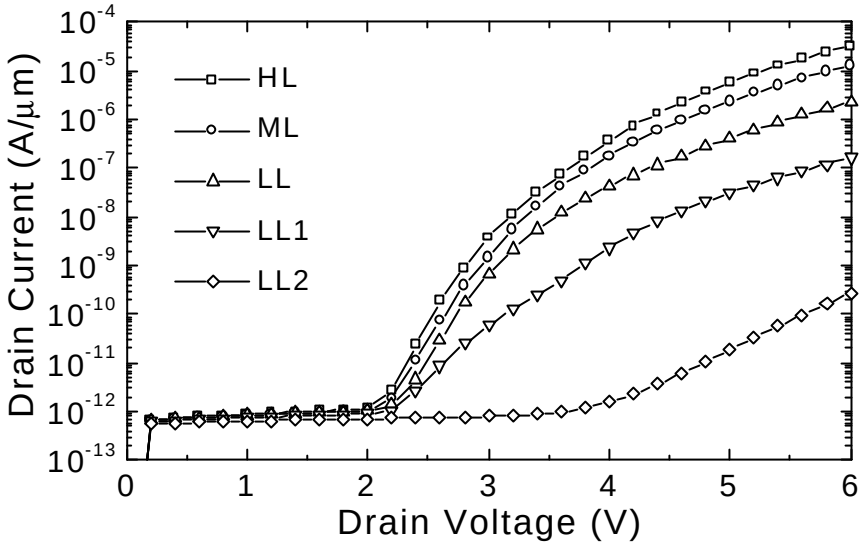


Fig. 4-4. GIDL currents for LDD MOSFETs as a function of drain voltage. V_{GS}=0V. HL: $5\times10^{14}cm^{-2}$, ML: $1\times10^{14}cm^{-2}$, LL: $5\times10^{13}cm^{-2}$, LL1: $3\times10^{13}cm^{-2}$, LL2: $1\times10^{13}cm^{-2}$.

decreased more rapidly for the lower dose of LDD MOSFETs. In other words, the variation of GIDL current is more severe in case of lower dose LDD MOSFETs.

Figure 4-5 shows the lateral electric field profiles at 2nm away from the SiO_2/Si interface for the LDD MOSFETs. It is known that the surface field at the point of maximum band-to-band tunneling is proportional to $V_{GD}/3T_{OX}$, where V_{GD} is the voltage difference between V_G and V_D and T_{OX} is the oxide thickness at the dominant tunneling point in the overlap region [36]. Therefore increase in T_{OX} reduces the vertical electric field in the gate-to-drain

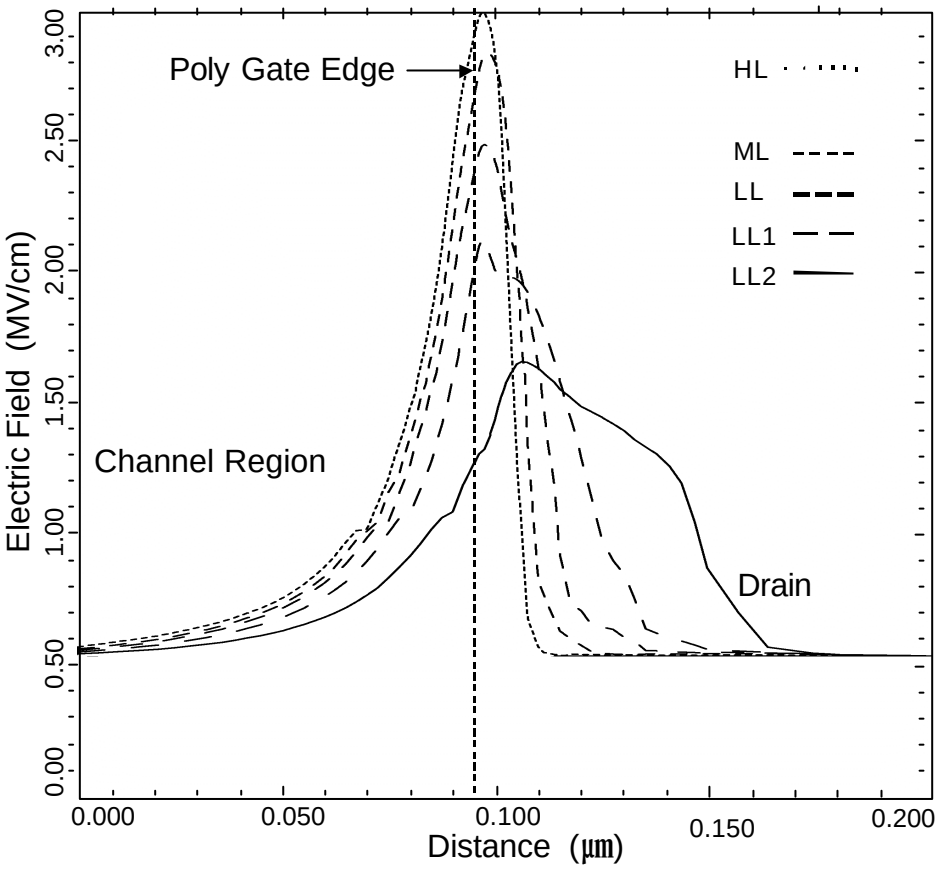


Fig. 4-5. Simulated lateral electric field profiles for LDD devices at 2nm away from the SiO_2/Si interface. V_{DS}=6.0V and V_{GS}=0V.

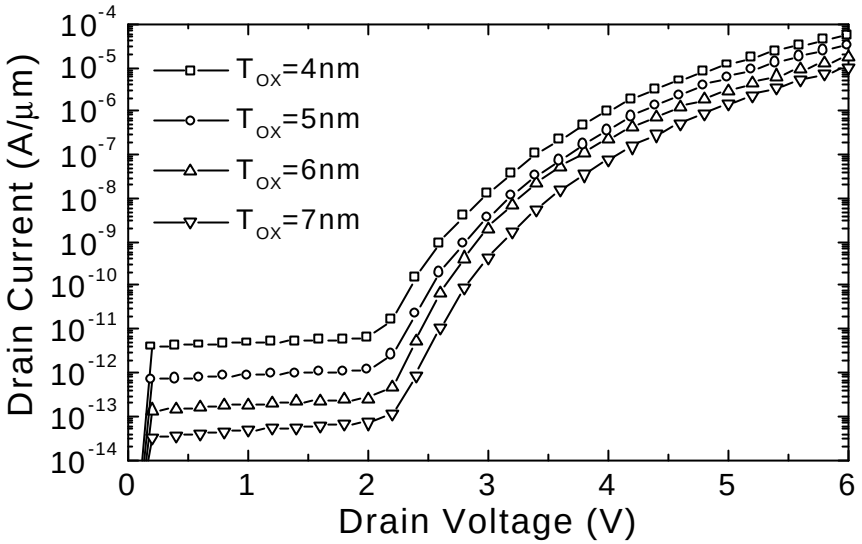


Fig. 4-6. GIDL currents for HL according to the gate oxide thickness (T_{OX}). V_{GS}=0V. SDE dose: $5\times10^{14}cm^{-2}$ (HL).

overlap region resulting in the lower GIDL current. Figure 4-6 shows the GIDL current of HL according to the gate oxide thickness (T_{OX}). It is clearly shown that by increasing T_{OX}, the GIDL current generation can be effectively suppressed. However, increasing T_{OX} significantly degrades the short channel characteristics and driving capability. As shown in Fig. 4-5, the location of the maximum electric field is shifted toward the drain side for LL2. As the distance between the point of maximum electric field and the poly gate edge is increased, the effective T_{OX} of LDD MOSFET is increased. This has an effect of reducing the electric field at the dominant tunneling point without physically increasing T_{OX}. As a result, the GIDL current is reduced. From the

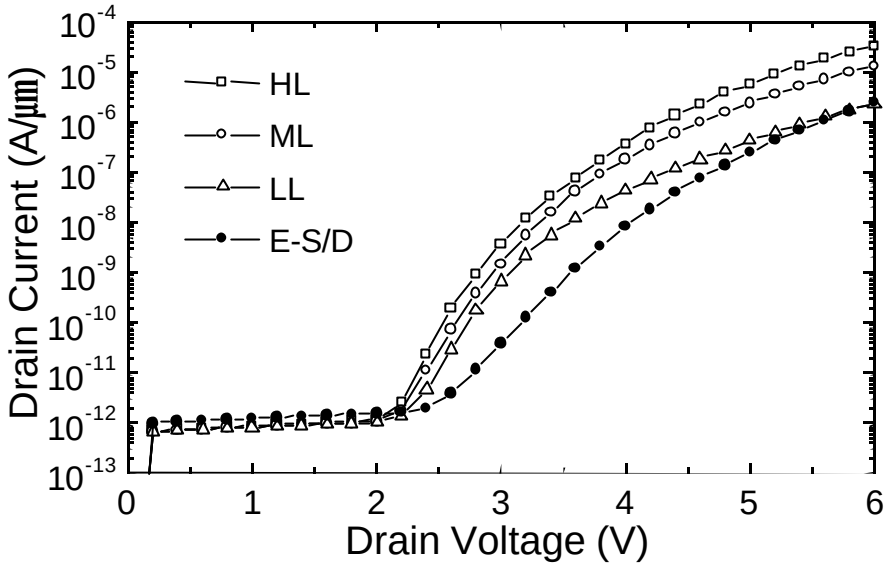


Fig. 4-7. GIDL currents for E-S/D and LDD MOSFETs as a function of drain voltage. V_{GS}=0V. HL: $5\times10^{14}cm^{-2}$, ML: $1\times10^{14}cm^{-2}$, LL: $5\times10^{13}cm^{-2}$.

results, decreasing the SDE dose causes the electric field to be decreased and eventually leads to the reduction of GIDL current. Furthermore, if the SDE dose is decreased below $3\times10^{13}cm^{-2}$, the point of maximum electric field is likely to be shifted toward the drain side resulting in the increment of the effective T_{OX}. This makes the variation of the GIDL current much larger for the lower dose LDD MOSFETs.

Figure 4-7 shows the GIDL characteristics of the proposed E-S/D and the conventional LDD MOSFETs. The poly gate length is 0.19μm. As the SDE dose is increased, GIDL current is also increased. On the other hand, the E-S/D MOSFET shows approximately one orders of magnitude lower GIDL

current than that of HL having the same SDE implantation dose condition ($5\times10^{14}cm^{-2}$).

The two-dimensional electric field and doping concentration contours for HL and the E-S/D MOSFET are compared in Fig. 4-8. The contours of electric field are plotted from 0.5MV/cm in steps of 0.2MV/cm for a drain bias of 6V. The contours of doping concentration for arsenic are plotted from $1\times10^{18}cm^{-3}$ to $1\times10^{20}cm^{-3}$ for both structures. Although the SDE implantation dose condition is the same for both cases, the SDE region of E-S/D MOSFET has a different doping distribution from that of HL. Because the peak of SDE implantation is positioned farther away from the surface in case of E-S/D, the SDE region has more gradually varying doping distribution compared to that of HL resulting in the reduced electric field as shown in Fig. 4-8. It is known that most of the band-to-band tunneling occurs at the surface of the high field region where the gate overlaps the drain. From Fig. 4-8(b), the E-S/D MOSFET has its peak field position farther away from the poly gate edge as indicated by the bold arrow. Figure 4-9 shows the lateral electric field profiles at 2nm away from the SiO_2/Si interface for the proposed E-S/D and LDD MOSFETs. It is shown that the peak of electric field is located more toward the drain side in case of the E-S/D MOSFETs.

As shown in Figs. 4-8 and 4-9, the high field region of the E-S/D MOSFET is shifted more toward the drain side compared to those of LDD MOSFETs. It makes the effective T_{OX} of E-S/D MOSFET larger than those of LDD MOSFETs at the point of the maximum field as shown in Fig. 4-10. This has an effect of reducing the electric field at the dominant tunneling point without physically increasing T_{OX}. Consequently, the GIDL current is reduced.

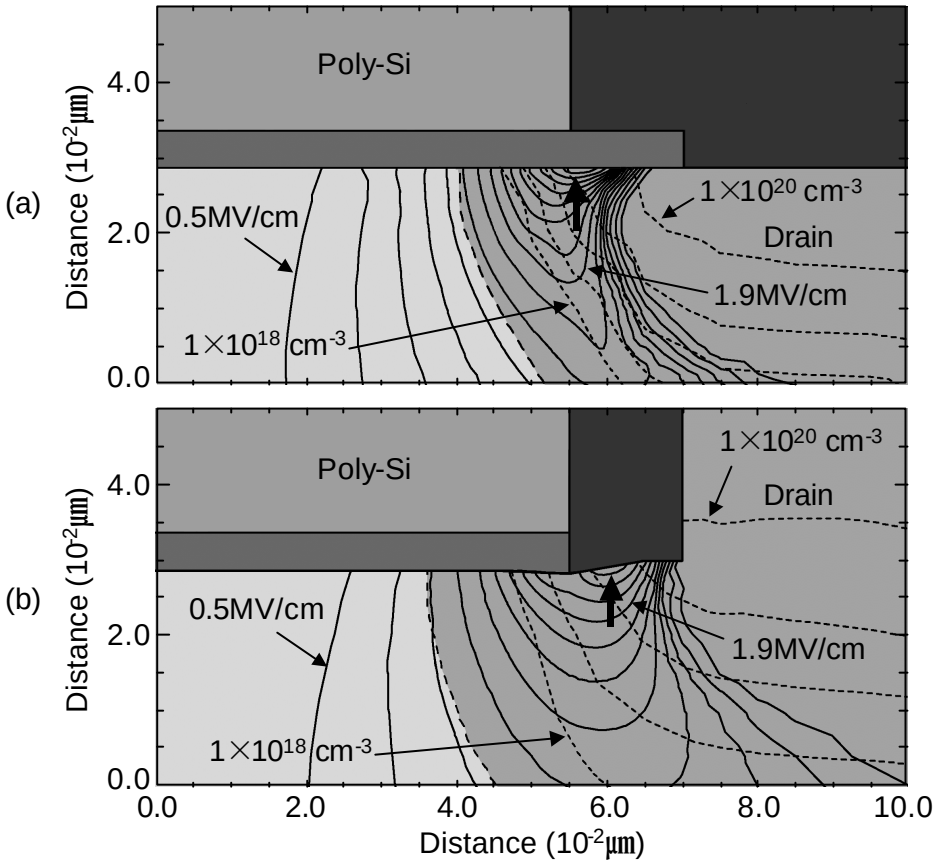


Fig. 4-8. Contours of electric field and doping concentration for (a) HL and (b) E-S/D MOSFET. V_{DS}=6.0V and V_{GS}=0V.

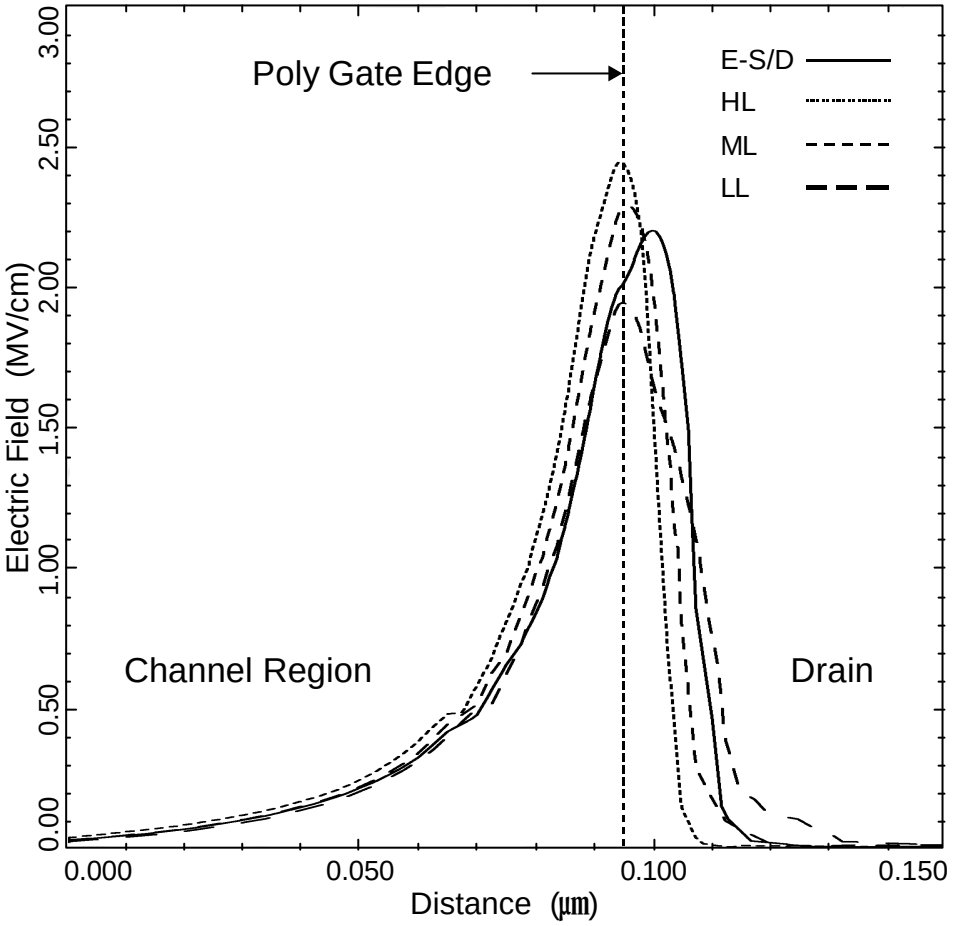


Fig. 4-9. Simulated lateral electric field profiles for E-S/D and LDD devices at 2nm away from the SiO_2/Si interface. V_{DS}=6.0V and V_{GS}=0V. The insert shows the region where the maximum electric field appears.

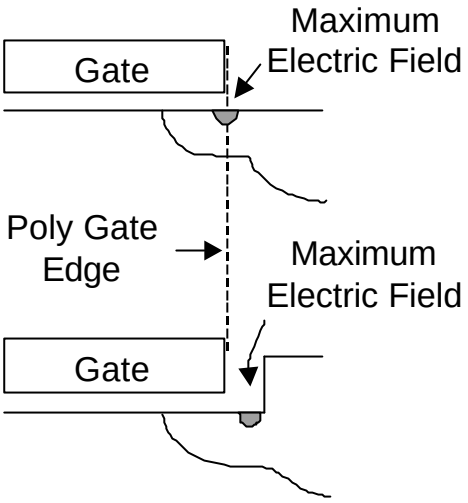


Fig. 4-10. Cross sectional schematic of conventional LDD MOSFET and the proposed E-S/D MOSFET showing the different location of the maximum electric field. The effective T_{OX} is increased for the E-S/D MOSFET.

Figure 4-11 shows the GIDL current of HL and proposed E-S/D structure according to the gate oxide thickness (T_{OX}). Solid symbol lines in the figure indicate the E-S/D MOSFET and the HL with the same conditions (SDE implantation dose: $5\times10^{14}cm^{-2}$ and T_{OX}: 5nm). It is shown that the GIDL current is decreased as T_{OX} is increased. Note that the E-S/D structure can suppress the GIDL current more effectively without physically increasing T_{OX}. Since the increased T_{OX} significantly degrades the short channel characteristics and the driving capability, the use of E-S/D structure can be advantageous for suppressing the GIDL current.

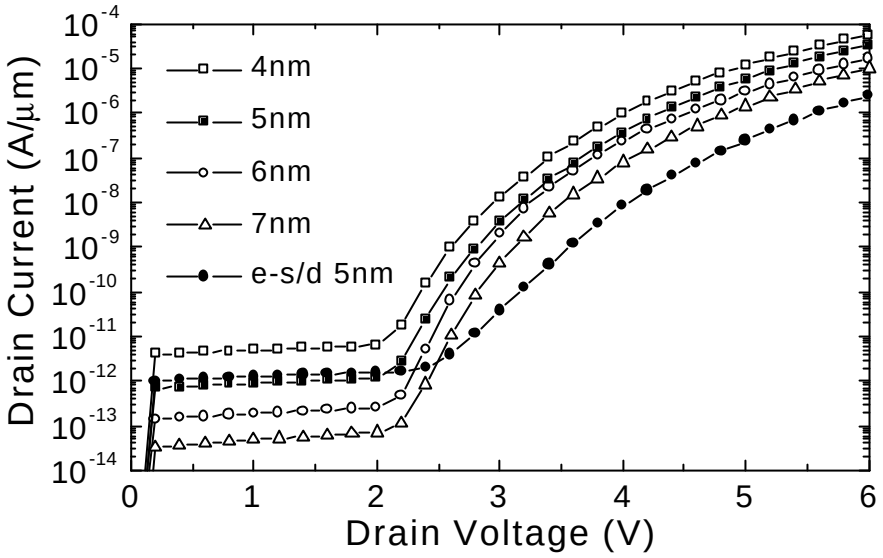


Fig. 4-11. GIDL currents for HL and E-S/D MOSFET according to gate oxide thickness (T_{OX}). V_{GS}=0V. SDE dose: $5\times10^{14}cm^{-2}$ (HL, E-S/D).

4.4 Short Channel Characteristics

Figure 4-12 shows the Drain-Induced Barrier Lowering (DIBL) characteristics of the E-S/D and the LDD MOSFETs. DIBL is defined as $\triangle V_{TH}=V_{TH}(V_{DS}=0.1V)-V_{TH}(V_{DS}=2.0V)$. It is shown that ML, LL and the E-S/D have the similar DIBL characteristics. In the LDD devices, the increase of the SDE dose results in the deterioration of DIBL characteristics. Although the E-S/D device has the same SDE implantation dose as HL, the more gradually varying SDE doping concentration of the E-S/D device reduces the DIBL.

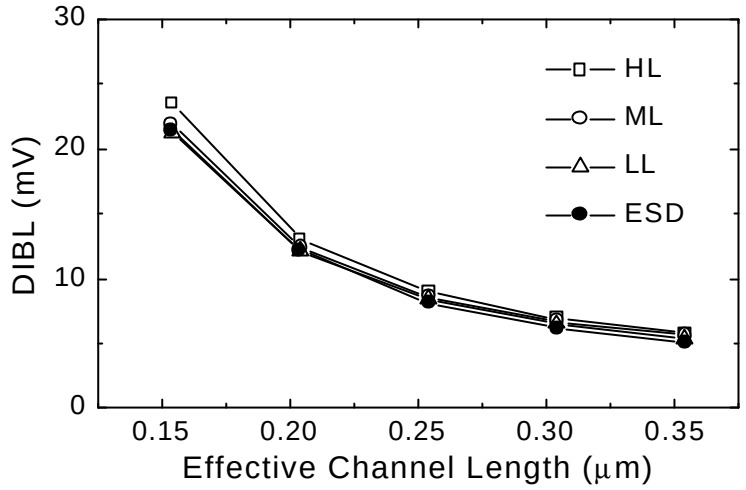


Fig. 4-12. DIBL characteristics of E-S/D and LDD MOSFETs.

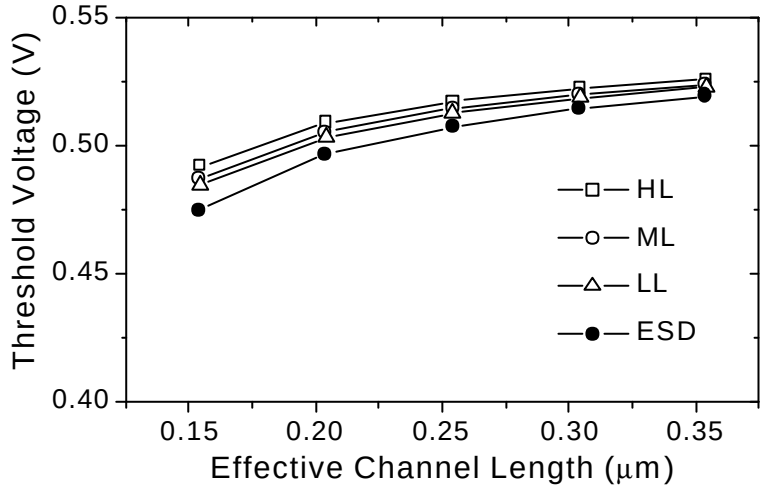


Fig. 4-13. Threshold voltage roll-off characteristics of E-S/D and LDD MOSFETs.

Threshold voltage roll-off characteristics of the E-S/D and the LDD MOSFETs are shown in Fig. 4-13. The LDD devices show V_{TH} roll-off characteristics similar to that of the E-S/D device. As the channel length is scaled down to near 0.15 ㎛, V_{TH} roll-off characteristics degrade slightly in the E-S/D device. It can be attributed to the selectively doped channel as shown in Fig. 3-3. From the figure, there exists the p-type doping concentration gradient between region (I) and (II) that results in the decrease of threshold voltage near channel edges. However, the amount of threshold voltage roll-off ($\triangle V_{TH}=V_{TH}(L_C \cong 0.35$ ㎛$)-V_{TH}(L_C \cong 0.15$ ㎛$)$) of the E-S/D device differs from that of LLs no more than 0.0065V.

Figure 4-14 shows the breakdown characteristics of E-S/D and LDD MOSFETs. Breakdown voltage (BV_{DSS}) is defined as the drain voltage that drain current reaches at 0.1nA/㎛ at gate bias of 0V. The breakdown voltages are obtained from MEDICI simulation that includes impact ionization and bandgap narrowing effect [55]. For LDD devices, increasing the SDE dose results in the decrease of breakdown voltage. However, the E-S/D device which has the same SDE dose condition ($5\times10^{14}cm^{-2}$) as that of HL, shows higher breakdown voltages. In case of E-S/D MOSFET, selectively doped channel reduces both the impact ionization near drain and the emitter injection efficiency of the parasitic bipolar transistor near the source [61]. The simulation result also verifies such fact that the breakdown of E-S/D device is more effectively suppressed.

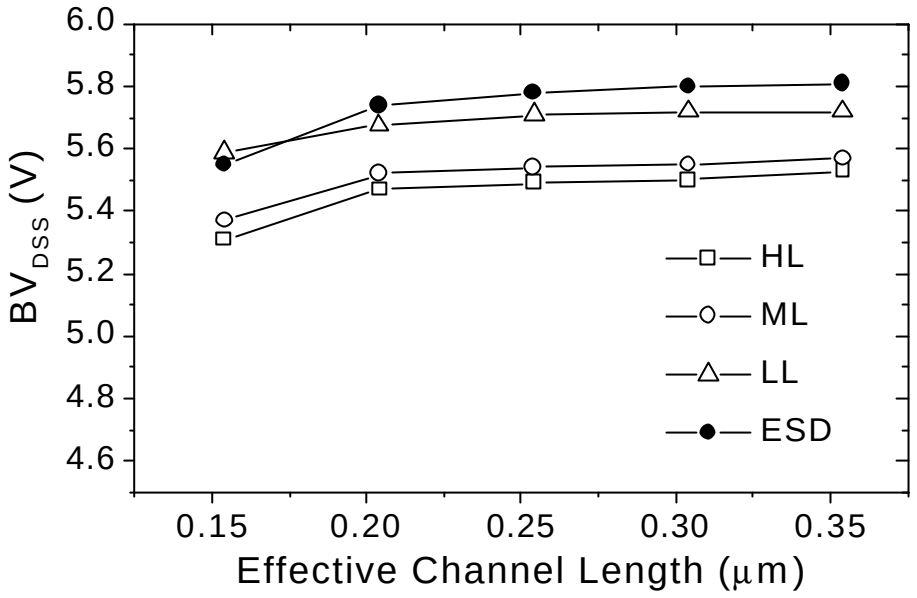


Fig. 4-14. Breakdown characteristics of E-S/D and LDD MOSFETs.

4.5 Current Driving Capability

Figure 4-15 shows I_{DS}-V_{DS} characteristics of the proposed E-S/D and LDD MOSFETs. The parasitic resistance and impurity scattering should be minimized for enhanced driving capability. Low energy implantation increases the sheet resistance of LDD devices due to the low-activation effect [26]. Despite of increase in the GIDL current, a larger SDE implantation dose is required to improve the driving current. The E-S/D MOSFET has the largest I_{DSAT} values among the structures investigated. This can be attributed to the

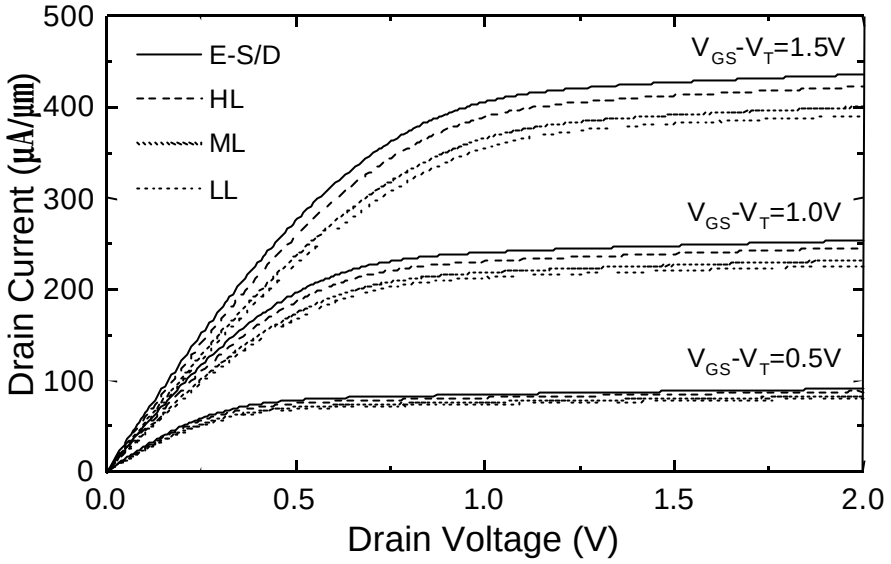


Fig. 4-15. I_{DS}-V_{DS} characteristics of E-S/D and LDD MOSFETs.

elevation of the SDE region. Relatively high energy(25keV) implantation is performed to form the SDE region by large-angle-tilted implantation. Consequently, very low energy implantation can be avoided. Figure 4-16 shows the maximum transconductance ($g_{m,max}$) characteristics of the E-S/D and LDD MOSFETs. The transconductance is obtained under the drain bias of 2.0V. Figure 4-17 shows the I_{DSAT} characteristics of the E-S/D and LDD MOSFETs. V_{DS}=2.0V and V_{GS}-V_T=2.0V. The trends of the curves are very similar to those of $g_{m,max}$.

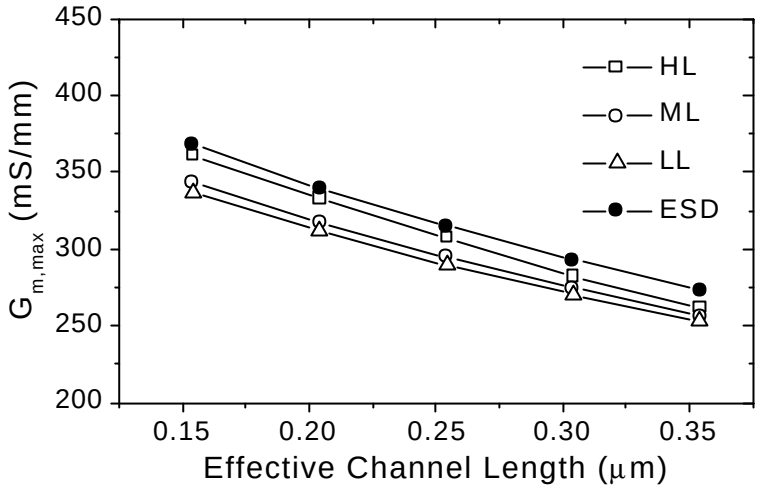


Fig. 4-16. $G_{m,max}$ characteristics of E-S/D and LDD MOSFETs.

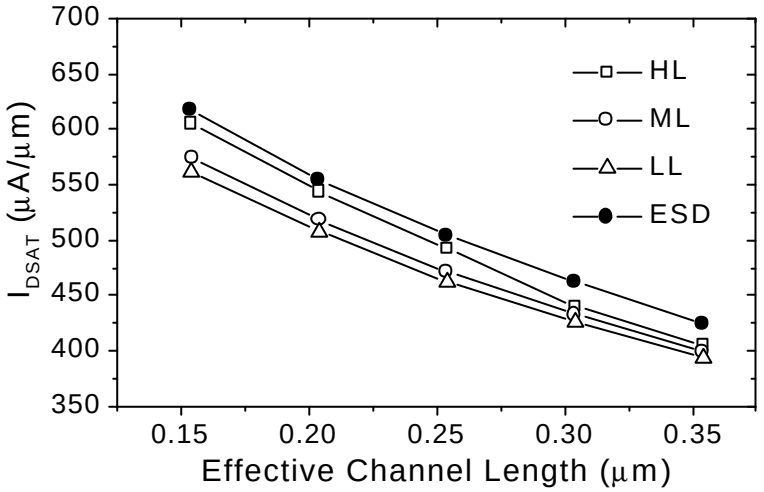


Fig. 4-17. I_{DSAT} characteristics of E-S/D and LDD MOSFETs.

$V_{DS}=V_{GS}-V_T=2.0V$.

4.6 Hot-Carrier Characteristics

To investigate the hot-carrier characteristics, the lateral electric field distribution is compared. Conventional method for analyzing the substrate current is based on the impact ionization model and has the problem of overestimating the substrate current [55]. Therefore, existing papers also regard the simulated substrate current values not as exact solutions. The simulations are mainly used for design guidelines and comparisons between the different structures with the same simulation conditions [14]. In the simulations, the energy balance equations are used for analyzing the hot-carrier characteristics [55],[62]. The energy balance equations are used for modeling the local carrier heating when there are high, spatial and rapidly varying electric fields.

Figure 4-18 shows the lateral electric field distribution of E-S/D and LDD MOSFETs. For the maximum substrate current condition (worst condition), the drain is biased at 2.5V and the gate at 1.3V. The LDD devices show similar lateral electric field distribution under worst conditions. However the E-S/D device shows significantly reduced (~25%) lateral electric field compared to those of LDD devices. It can be attributed to the selectively doped channel profile and gradually varying doping profile of SDE region. Figure 4-19 shows the contours of electric fields for the three LDD (LL, ML, HL) and E-S/D devices. The contours of electric field are plotted from 0.25MV/cm in steps of 0.04MV/cm for V_{DS}=2.5V and V_{GS}=1.3V. As the SDE implantation dose is increased, the electric field is gradually increasing. It is clearly seen that E-S/D device has much lower electric field under worst case condition.

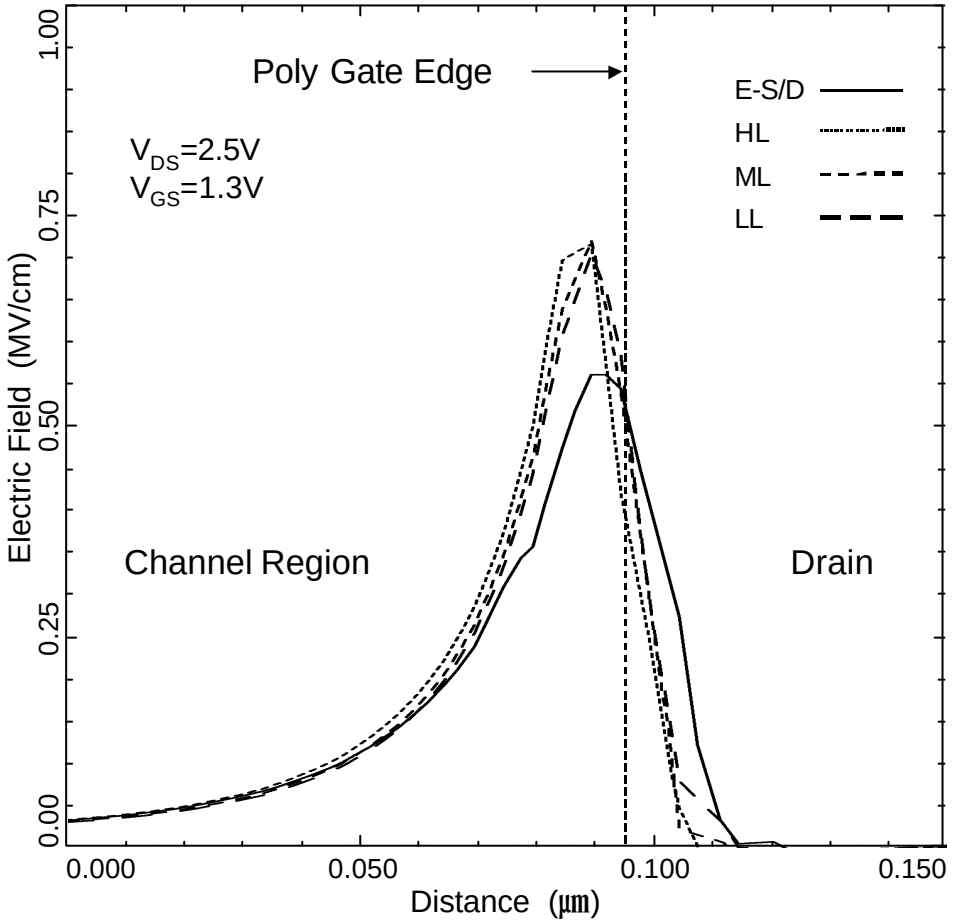


Fig. 4-18. Lateral electric field distribution of E-S/D and LDD MOSFETs. V_{DS}=2.5V and V_{GS}=1.3V.

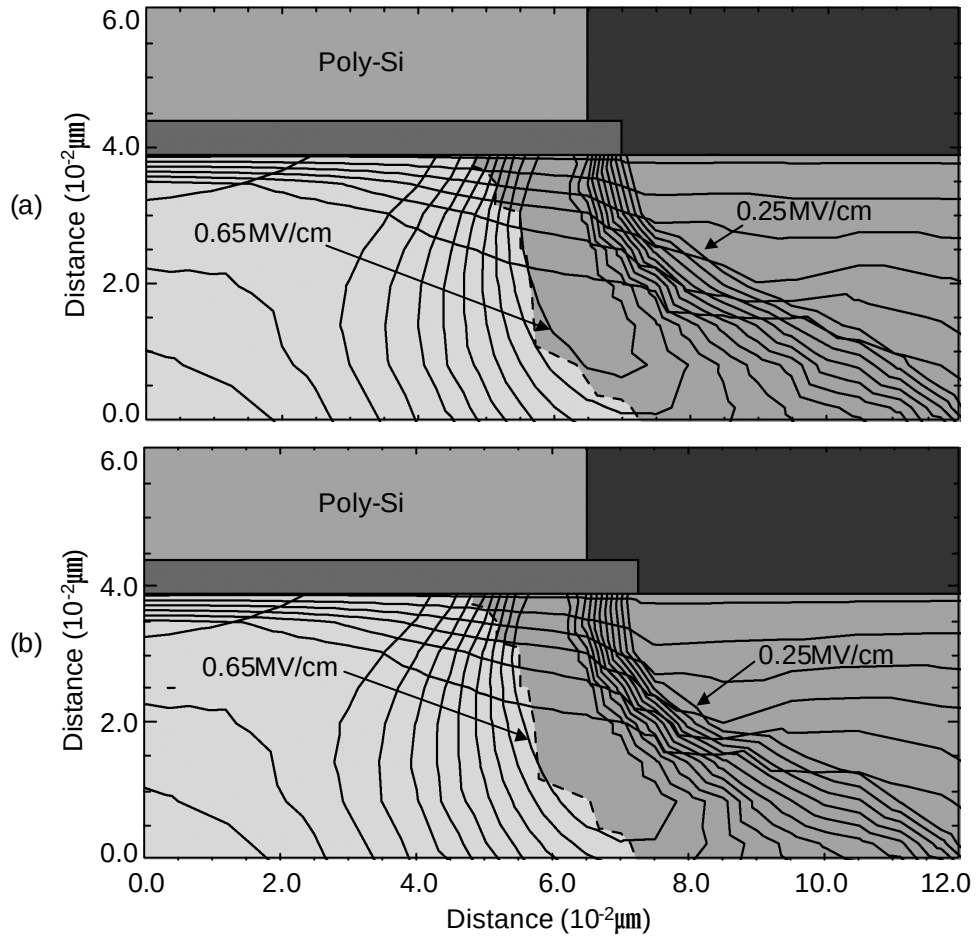


Fig. 4-19. Contours of electric field for (a) LL and (b) ML. V_{DS}=2.5V and V_{GS}=1.3V. (continued)

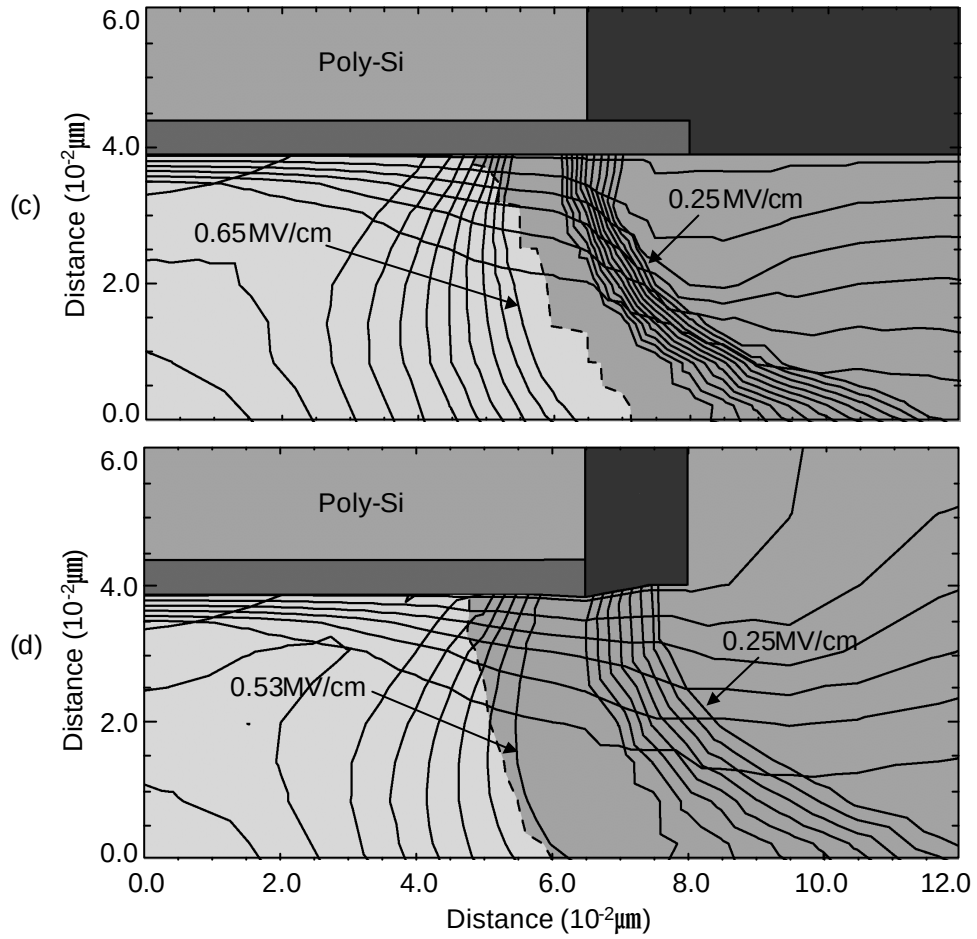


Fig. 4-19. Contours of electric field for (c) HL and (d) E-S/D. V_{DS}=2.5V and V_{GS}=1.3V.

4.7 E-S/D MOSFET with Selective Epitaxial Growth: Design & Electrical Characteristics

E-S/D MOSFETs with Selective Epitaxial Growth (SEG) Process (here after SEG MOSFETs) are designed for comparison with the proposed E-S/D MOSFET. Figure 4-20 shows the fabrication process of the SEG MOSFET. The offset spacers are used for the control of the effective channel length as previously shown in Fig. 4-3. The epi-layer is grown to have thickness of 80nm under 850°C, 1.2min [14]. The SDE implantation is performed prior to the epitaxial growth of silicon. The facet angle is about 28°, corresponding to {113} growth plane [32]. The epi thickness at the nitride sidewall spacer edge was taken as 30nm if the epi layer thickness at plain Si surface is assumed to be 100nm [32]. Applying such relationships, the epi thickness at the sidewall spacer edge can be calculated regardless of the epi layer thickness. The heavy source drain implantation is performed to have the same junction depth with that of conventional LDD MOSFETs. Several SEG structures are used for the simulations as shown in Fig. 4-21. Large-angle-tilted implantation for the heavy source/drain is adopted for SEG MOSFET with dual (2nd) sidewall spacers and its influences on the device performance are analyzed. All the SEG structures are designed to have the same junction depth (referenced from the channel interface) regardless of the epi-layer thickness and the angle (θ) of tilted implantations. The process parameters of the simulated SEG MOSFETs are listed in Table 4-2.

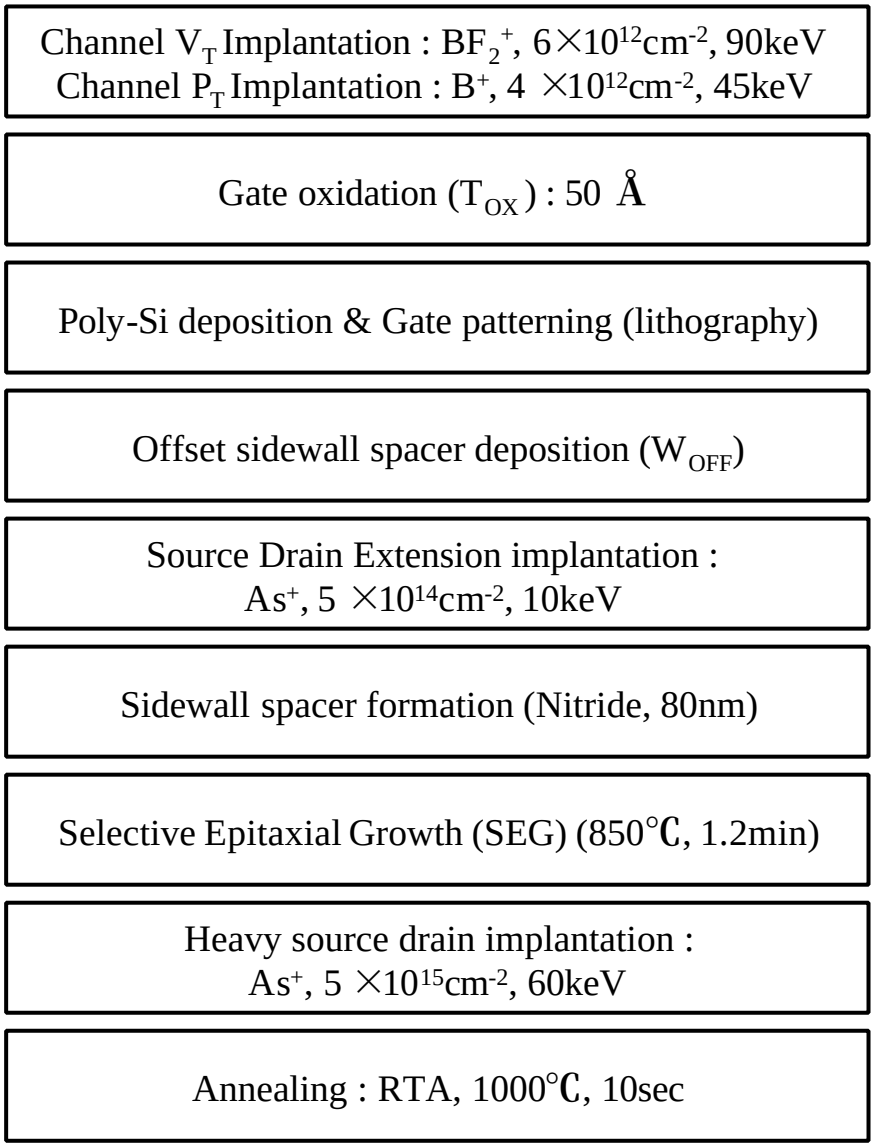


Fig. 4-20. Main fabrication steps of the conventional SEG MOSFETs

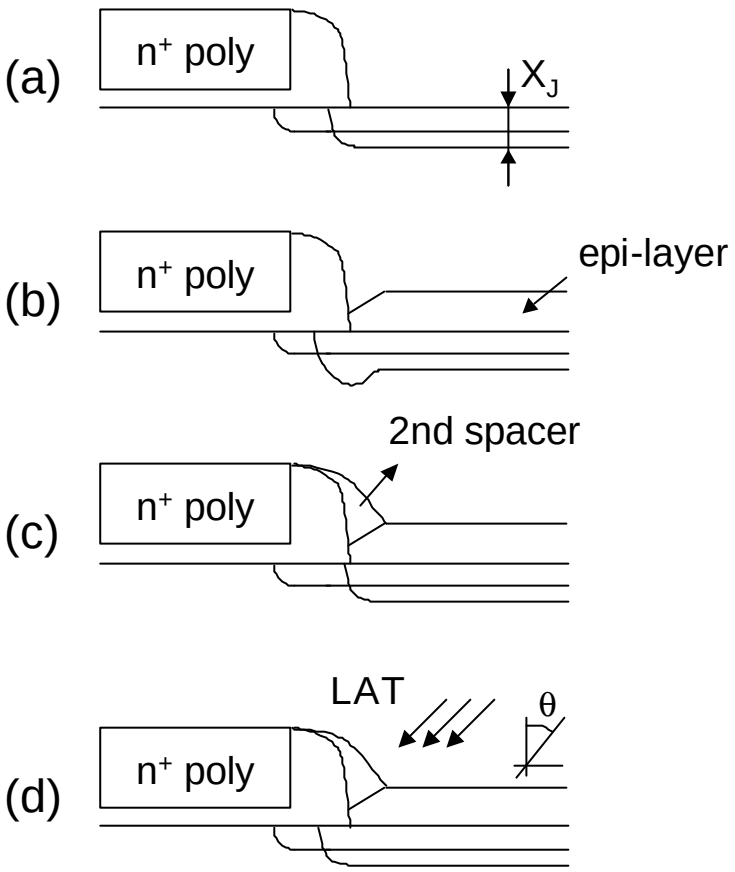


Fig. 4-21. SEG MOSFET structures used for the simulation. (a) conventional LDD structure (HL), (b) conventional SEG structure with facet (HL-S), (c) SEG structure with dual (2nd) spacers used (HL-SD), (d) structure (c) with large-angle-tilted n^+ S/D implantation (HL-SDT).

Table 4-2. Process parameters of the simulated SEG MOSFETs.

Process Parameter	**HL-S**	**HL-SD**	**HL-SDT**
Channel Implantation	B^+, 4×10^{12}, 45keV BF_2^+, 6×10^{12}, 90keV		
Gate Oxide Thickness (T_{OX})	50Å		
Offset Sidewall Width (W_{OFF})	15nm		
SDE Implantation	$5\times10^{14}cm^{-2}$, 10keV		
S/D Implanatation	$5\times10^{15}cm^{-2}$	$5\times10^{15}cm^{-2}$	$5\times10^{15}cm^{-2}$, (θ=30°, 45°)
Final Sidewall Width (W_S)	80nm		
Epi-layer Thickness	80nm (850℃, 1.2min)		
Effective Channel Length	0.1538μm	0.1538μm	0.1538μm
Poly Gate Length (L_{POLY})	0.19μm		
Annealing	1000℃, 10sec		

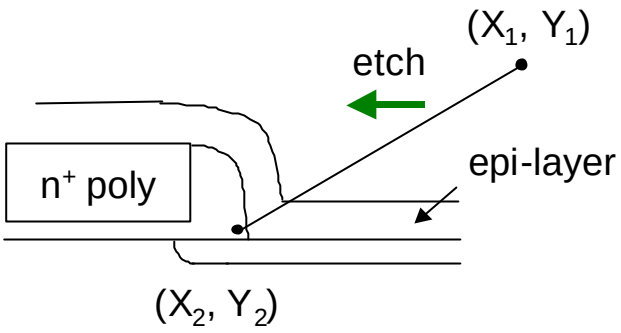


Fig. 4-22. Removal of the epi-layer by ETCH command. Etch all material to the left or right of the line between (X_1, Y_1) and (X_2, Y_2) is possible.

In the TSUPREM-4 simulations, epitaxial growth of Si is supported for the simulations. However, the selective epitaxial growth of Si is not supported. Epi-layers are formed on the material regardless of the material whether it is crystalline Si or not. And the facets are not automatically generated. To take the facets into account, the ETCH command is used to construct the real shape of the SEG MOSFETs. The epi-layer is partly removed by ETCH command as shown in Fig. 4-22. In TSUPREM-4, it is possible to etch all material to the left or right of the line between (X_1, Y_1) and (X_2, Y_2).

Figure 4-23 and 4-24 show the threshold voltage roll-off and DIBL characteristics of SEG MOSFET and conventional LDD MOSFETs, respectively. The threshold voltage roll-off characteristics show very similar trends each other. DIBL is degraded for HL-S due to the facet effect. HL-SD has the lowest DIBL values among the structures investigated meaning that the dual spacers can be used to fully suppress the short channel degradations. In case of HL-SDT, DIBL increases with increasing tilt angle θ.

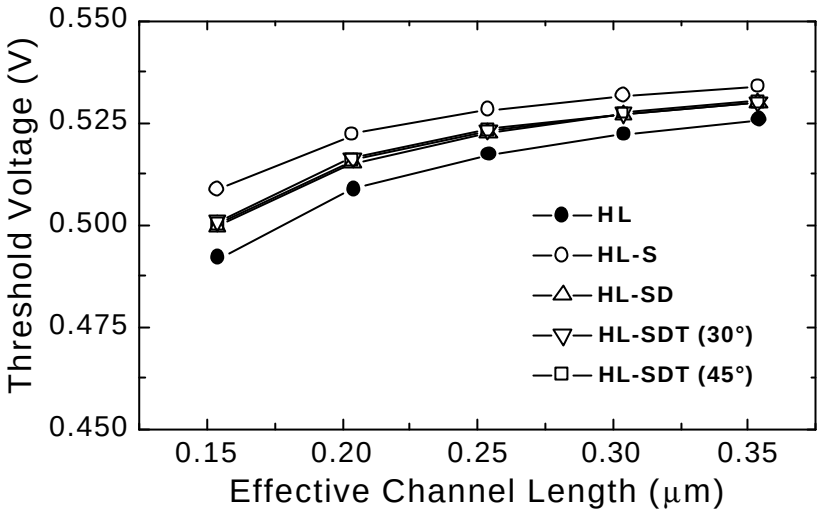


Fig. 4-23. Threshold voltage roll-off characteristics of HL and SEG MOSFETs

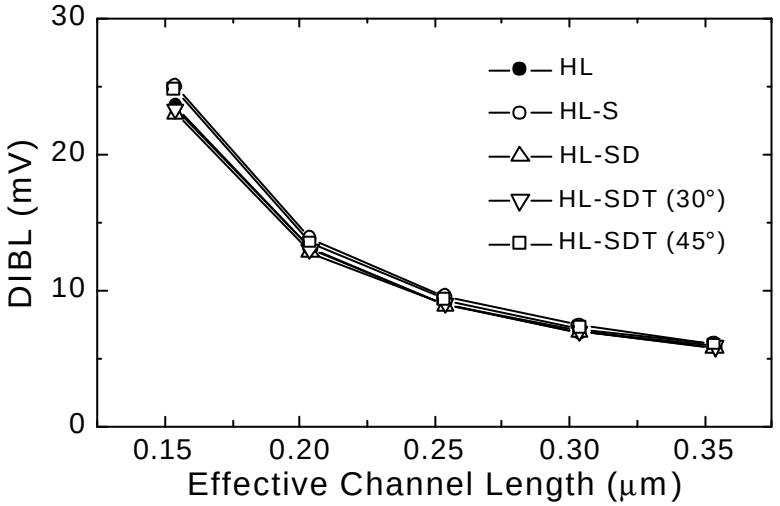


Fig. 4-24. DIBL characteristics of HL and SEG MOSFETs.

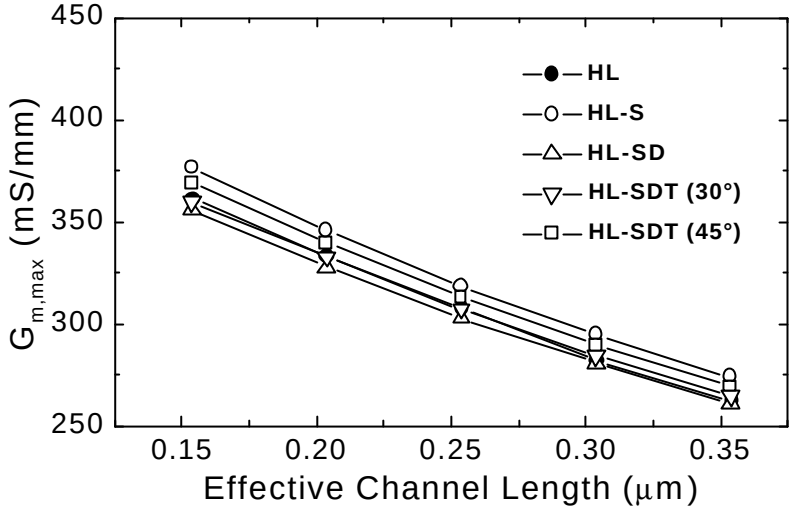


Fig. 4-25. $G_{m,max}$ characteristics of HL and SEG MOSFETs.

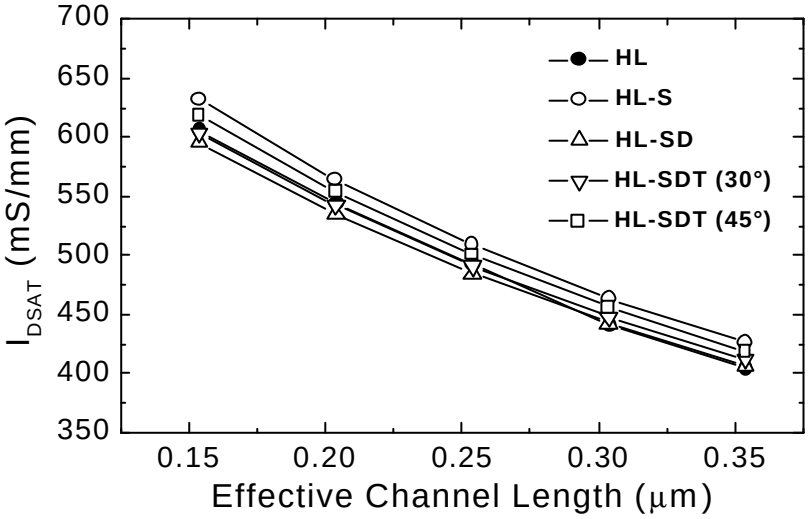


Fig. 4-26. I_{DSAT} characteristics of HL and SEG MOSFETs.

Figure 4-25 and 4-26 show the $G_{m,max}$ and I_{DSAT} characteristics of HL and SEG MOSFETs, respectively. Although HL-S shows poor short channel characteristics, the driving current is increased due to increased junction depth near channel edges. SEG MOSFET with dual spacers (HL-SD) has the poorest driving capability among the structures simulated. This is because the HL-SD covers the facet region resulting in the increased spacer width. In case of HL-SDT, driving current increases with increasing the tilt angle, θ.

The impact of facet on the short channel effect was not severe due to the sufficiently large width of the sidewall spacer width (W_S). HL-SD shows excellent immunity against the short channel effects but has poor driving capability. It is shown that the driving capability of HL-SD device can be enhanced by adopting the large-angle-tilted implantation method.

Figure 4-27 shows the GIDL currents of HL-S, the proposed E-S/D MOSFET and the conventional LDD MOSFETs. The HL-S shows the largest GIDL current among the simulated structures. Although the current driving capability is increased for HL-S, GIDL current is also increased showing the significant trade-off relationships.

Simulated lateral electric field profiles for HL-S, HL and the E-S/D devices are shown in Fig. 4-28. Unlike the E-S/D device, HL-S shows similar lateral electric field profiles to that of HLs. Such fact indicates that the SDE implantation method plays major role in the determination of GIDL current.

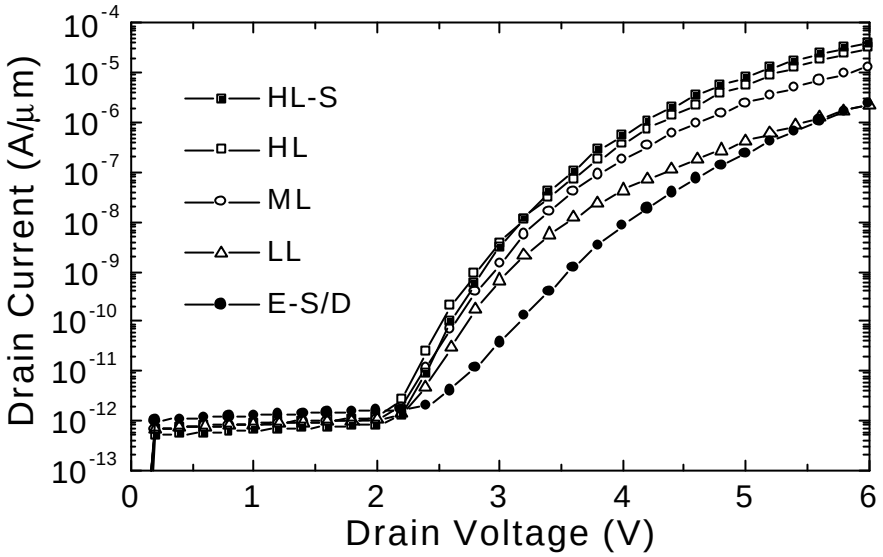


Fig. 4-27. GIDL current for HL-S compared with those of E-S/D and LDD MOSFETs as a function of drain voltage. V_{GS}=0V. HL: $5\times10^{14}cm^{-2}$, ML: $1\times10^{14}cm^{-2}$, LL: $5\times10^{13}cm^{-2}$.

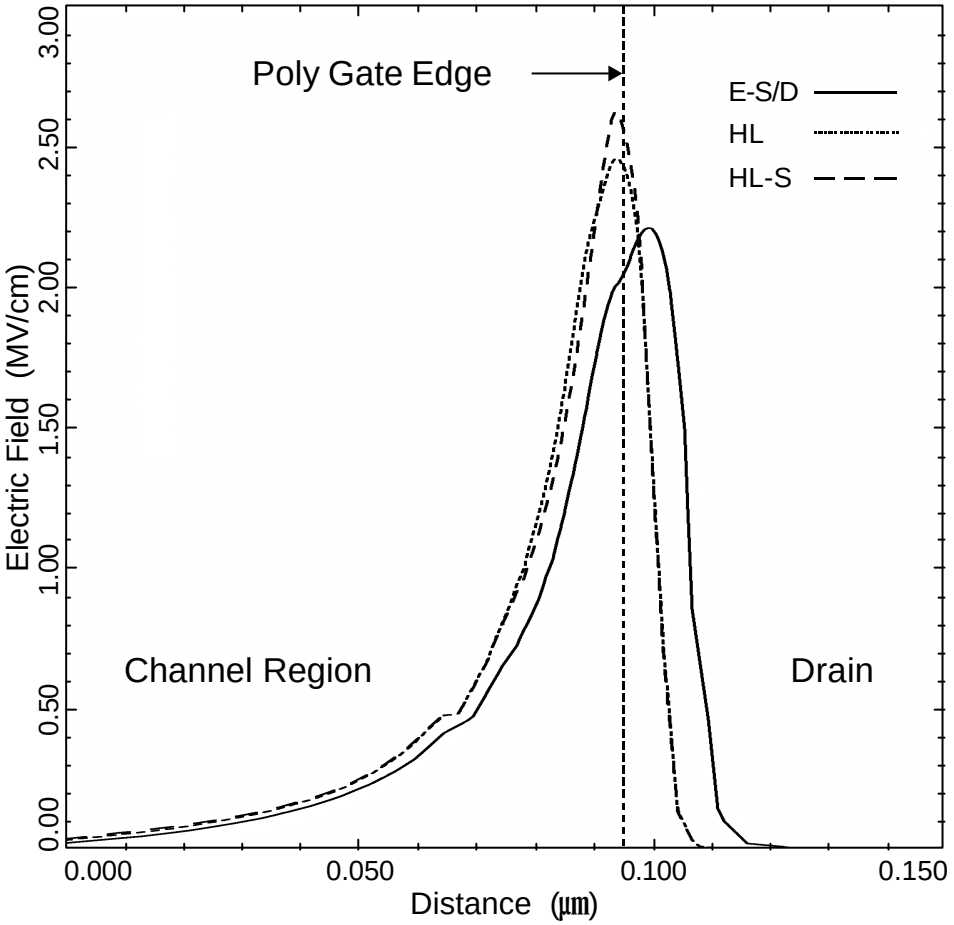


Fig. 4-28. Simulated lateral electric field profiles for HL-S, HL and E-S/D devices at 2nm away from the SiO_2/Si interface. V_{DS}=6.0V and V_{GS}=0V.

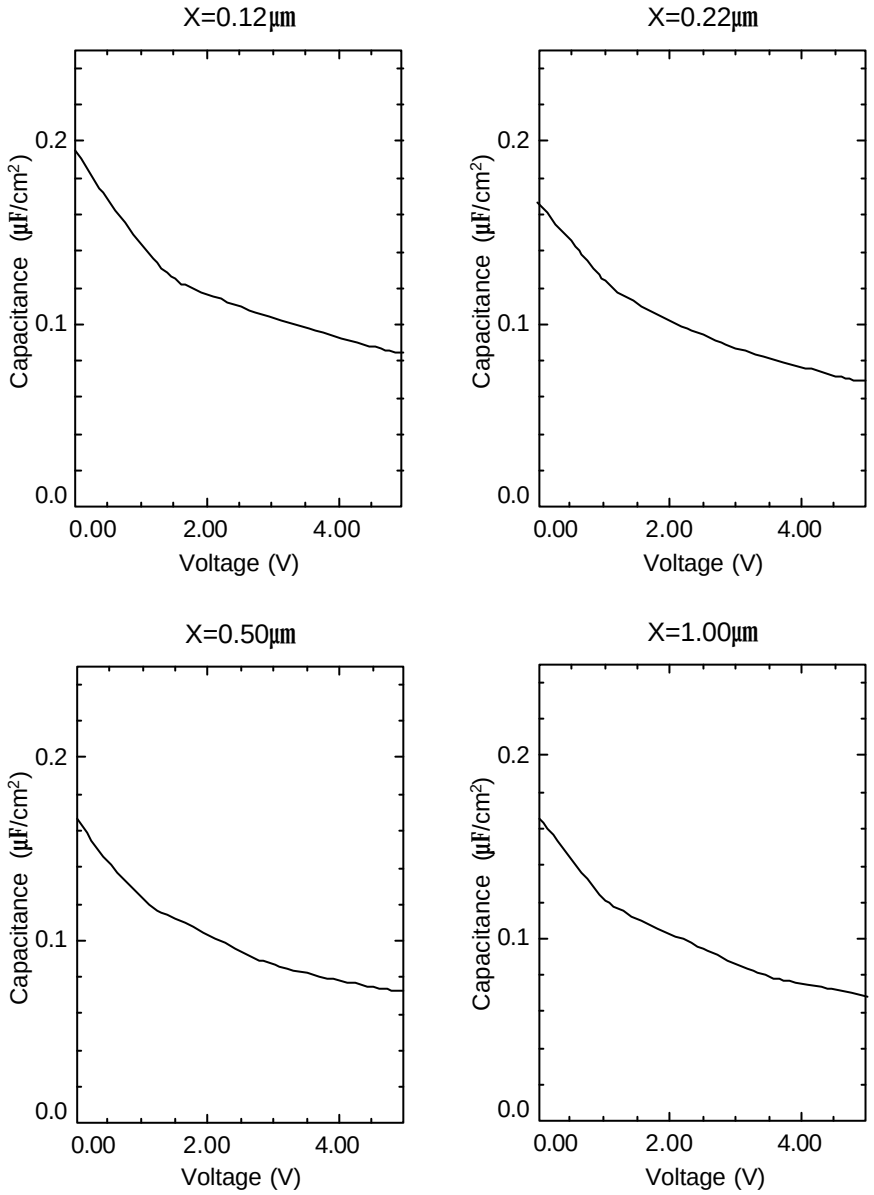
4.8 Junction Capacitance

The junction capacitance between the source/drain and the substrate can be treated as that of p-n junction diodes. The p-n junction diodes differ from a standard capacitor in that the diode capacitance monotonically decreases with increasing reverse bias. The junction capacitance can be described by analogy to be [56],

$$C_J = eA\left[\frac{q}{2e(V_0 - V)}\frac{N_d N_a}{N_d + N_a}\right]^{1/2} = \frac{K_S e_0 A}{W} \qquad (4\text{-}1)$$

where W is the depletion layer width. From the equation, C_J can be reduced if W is increased. In case of an asymmetrically doped junction, the depletion layer extends primarily into the less heavily doped side, and the capacitance is determined by only one of the doping concentrations. Increasing the reverse bias or decreasing the doping concentration at the less heavily doped part of the p-n junction, C_J is decreased.

Figure 4-29 shows the reverse-bias junction capacitance of HL and E-S/D MOSFET. X indicates the distance from the center of the channel. As the reverse bias applied to n^+-p junction is increased, the junction capacitance is decreased. For X=1μm, the E-S/D MOSFET shows approximately 0.5 times lower value of capacitance than HL at reverse bias of 0V. Due to the selectively doped channel structure, E-S/D device offers reduced junction capacitance and the device switching speed can be effectively enhanced.



-

Fig. 4-29. Junction capacitance of HL. X indicates the distance from the center of the poly-gate. The poly-gate length is 0.19 ㎛. (continued)

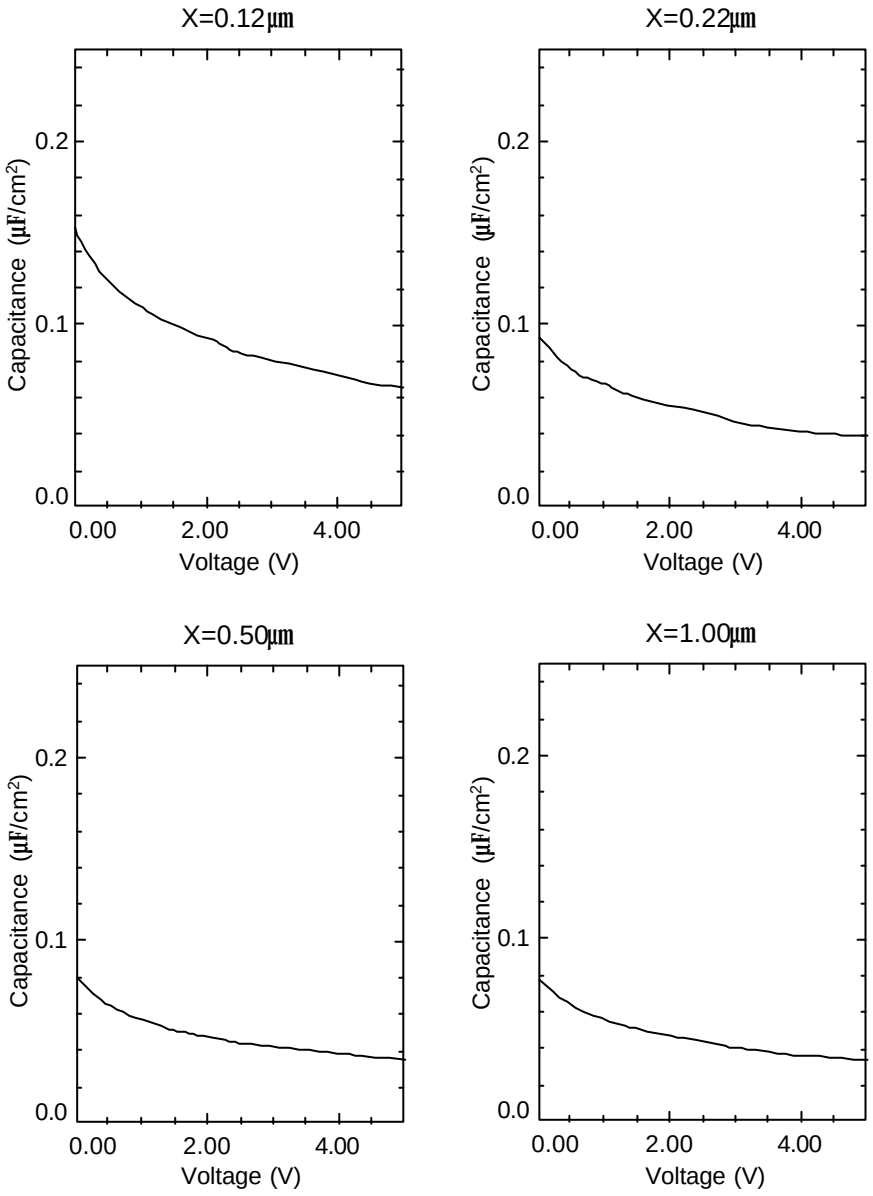


Fig. 4-29. Junction capacitance of the proposed E-S/D MOSFET.

Chapter 5. Conclusion

In this thesis work, a new self-aligned E-S/D structure is proposed and its electrical characteristics are analyzed. The proposed structure has simple fabrication steps compared with those of the previously reported E-S/D MOSFETs. The self-aligned gate is formed on the recessed channel so that the self-alignment is realized for both the source/drain and the gate on the recessed channel. Only one lithography step is needed for the recessed channel and gate definition making the process much simpler. Furthermore, the limitation of lithography process due to the minimum gate length is less severe in case of the proposed fabrication method. Since the poly gate is formed after the inverted sidewall spacers are formed inside the recessed channel region, there is no need to define the gate length in the lithography step. The recessed channel area is defined in the lithography step instead of the gate area.

The proposed structure is elevated in the source drain extension region so that very low energy implantation, which can be the cause of the low-activation effect, can be avoided. Large-angle-tilted implantation is performed to guarantee the sufficient gate-to-drain overlap area and to decrease the junction depth. Because the peak of SDE implantation is located farther away from the surface in case of E-S/D device, the SDE region has more gradually varying doping distribution compared to that of LDD MOSFETs (HL) resulting in the reduced electric field.

The proposed structure has selectively doped channel doping profiles. From the simulation results, it is shown that both the lateral electric field and the junction capacitance are reduced. Since the channel implantation is performed

selectively through the open area (W_R-$2W_{RN}$), the channel doping profiles can be controlled according to the removable nitride sidewall width (W_{RN}). Two dimensional device simulations verify that the lateral electric field is reduced as W_{RN} is increased. However, W_{RN} should be carefully selected considering the recessed channel width (W_R), so that the insufficient channel implantations can be prevented. As the device scales down, the inevitably increased channel doping concentration causes the junction capacitance to be increased in the uniformly doped channel structures. On the other hand, the selectively doped channel structure has reduced junction capacitance because the doping concentration beneath the source/drain is not affected by the channel implantations.

From the GIDL simulations, the E-S/D MOSFET showed approximately one orders of magnitude lower GIDL current than that of LDD MOSFET (HL) having the same SDE implantation dose condition ($5\times10^{14}cm^{-2}$) while maintaining the higher saturation current levels. The main reason for reduction of the GIDL current is the decreased electric field at the point of the maximum band-to-band tunneling as the peak electric field is shifted toward the drain side. Simulation results show that the position of the peak electric field plays major role in the determination of GIDL current.

From the short channel effect simulations, the Drain-Induced Barrier Lowering (DIBL) and Breakdown characteristics are enhanced compared with those of LDD devices. The selectively doped channel reduces both the impact ionization near drain and the emitter injection efficiency of the parasitic bipolar transistor near the source. The gradually varying doping distribution of SDE region further reduces the lateral electric field at drain side suppressing

the short channel effects. The V_T roll-off characteristics were slightly degraded due to the lack of impurities near the channel edges. However the difference between the E-S/D and LDD devices was comparable.

From the hot-carrier simulation results, the lateral electric field of the E-S/D device is significantly reduced compared with those of conventional LDD devices under worst bias condition. The selectively doped channel combined with the gradually varying SDE region helps to reduce the electric field near the drain edge alleviating the impact ionization rate.

Various kinds of SEG MOSFET structures are also included for comparison and discussion. The conventional SEG MOSFET with facet is designed based on the conventional LDD MOSFET. Although the facet has the effect of aggravating the short channel effects (SCE), the degradation of SCE was less severe if the sidewall width was kept sufficiently large. The SEG MOSFET which has dual sidewall spacers combined with the large-angle-tilted n^+ implantation technique is also proposed and analyzed. From the simulation results, the proposed scheme can be beneficial for improving the device performance in the dual spacer SEG MOSFETs without sacrificing the short channel characteristics. In the GIDL simulation, unlike the proposed E-S/D MOSFET, SEG MOSFETs showed larger GIDL currents compared with those of conventional LDD MOSFETs with the same SDE implantation dose conditions. Since the SDE region of SEG MOSFETs is formed the same way as that of LDD MOSFETs, they showed similar GIDL current characteristics.

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국문 요약

누설전류 성분을 줄인 새로운 구조의 고성능 Elevated Source Drain MOSFET 에 관한 분석

감소된 누설전류 특성 및 향상된 전류 구동력을 갖는 새로운 구조의 Elevated Source Drain (E-S/D) MOSFET 을 제안하고 이를 분석하였다. 제안된 구조는 건식 식각 공정을 사용하여 함몰된 채널을 형성한다. 소자의 특성은 함몰된 채널 깊이와 측벽 길이에 의해 결정되며 이는 건식 식각 공정과 직접적으로 연관된다. 제안된 구조의 주된 장점은 소오스/드레인 확장 영역이 들려진 형태를 갖는 점과 선택적인 채널 도핑 구조를 갖는 것이다. 들려진 소오스/드레인 확장 영역은 매우 낮은 에너지 이온주입으로 인해 발생되는 저활성화 효과를 해결할 수 있다. 소오스/드레인 확장 영역을 형성하기 위한 이온주입 공정으로 큰 경사각 이온주입 방법이 적용되었다. 선택적으로 도핑된 채널 구조는 수평전계 및 접합 커패시턴스를 줄일 수 있는 효과를 갖는다. 또한 제안된 구조는 함몰된 채널내에 존재하는 반전된 측벽을 사용하여 자기 정렬된 폴리 게이트를 형성함으로써 함몰된 채널내에 정확하게 폴리 게이트를 자기 정렬시킬 수 있는 장점이 있다. 제안된 구조에서, 들려진 소오스/드레인 확장 영역은 소오스/드레인 확장 영역을 형성시킬 때 상대적으로 높은 에너지의 이온주입을 가능하게 함으로써 기생저항 성분을 크게 감소시킬 수 있다. 또한 제안된 구조에서는, 기존의 LDD MOSFET 구조에서 소오스/드레인 확장 영역의 불순물 도즈(dose)가 커짐에 따라서 Gate-Induced Drain Leakage (GIDL) 전류가 증가되는 문제가 크게 경감되었다. 즉, 기존의 구조들에서 GIDL 전류를 감소시킬 때 소자 성능도 함께 심하게 저하되는 것과는 달리, 소자 성능의 저하를 최소화하면

서 GIDL 전류를 효과적으로 감소시킬 수 있다. 시뮬레이션 결과, 제안된 구조는 같은 소오스/드레인 확장 도즈를 갖는 LDD (HL) 소자에 비해 전류 구동력은 더 크게 유지하면서도 약 10 배 정도 줄어든 누설전류 특성을 나타내었다. GIDL 전류가 줄어드는 주된 이유는 밴드간 터널링이 최대가 되는 전계의 위치가 드레인 방향으로 이동되면서 결과적으로 최대 전계가 줄어드는 효과를 보이기 때문이다. 핫캐리어 특성 시뮬레이션 결과, 핫캐리어 특성이 최악이 되는 바이어스 조건하에서 제안된 구조의 최대 수평전계값이 LDD 구조의 경우에 비해 약 25% 감소된 수치를 나타냄을 확인하였다. 이는 선택적으로 도핑된 채널 구조와 도핑 농도가 더욱 점차적으로 변화되는 형태를 갖는 소오스/드레인 확장 영역으로 인하여 드레인과 접하는 채널쪽의 수평 전계가 효과적으로 감소되기 때문이다. 단채널 특성 분석의 결과, Drain-Induced Barrier Lowering (DIBL) 및 항복전압 특성은 제안된 구조의 경우가 단채널 효과에 더 우수한 저항력을 나타내었다. 반면에 문턱전압의 감소현상은 미세하게 저하되는 현상을 나타내었다. 이는 선택적인 채널 도핑의 특성상 채널의 양끝 부분에서 불순물이 충분히 도핑되지 않을 수 있기 때문이다.

제안된 E-S/D 구조는 단순한 제작 공정을 갖고, 향상된 성능과 감소된 누설전류 특성을 동시에 보장하는 장점을 보이므로 0.25μm 이하의 초미세 소자 구조로서 유력한 대안이 될 수 있을 것으로 기대된다.

핵심되는 말 : Elevated Source Drain, 건식 식각, 자기 정렬, GIDL, 소오스/드레인 확장 영역, 수평전계, 선택적인 채널 도핑