Analysis of Feedforward Ring Oscillators and Its Application to High-Speed Multiphase Clock Generation

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To my family and friends

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Abstract

A ring oscillator (RO) has a great advantage over other types of oscillator. Multiphase clock generation is simple and easy with a RO because of its symmetric loop structure. Also, a RO usually occupies very smaller die areas than any other types of oscillator.

However, a ring RO generally suffers from its low oscillation frequency, especially when it is implemented with CMOS inverters with large numbers of stage. To increase a RO's oscillation frequencies, several new structures and design techniques have been proposed. Some of them suggest that adding feedforward paths to a conventional RO makes it oscillate at much higher frequencies. These types of RO are called feedforward ring oscillators (FROs).

In this dissertation, a simple modeling and analyzing method of FRO are presented. Also, it is found that FROs as well as ROs have more than one oscillation mode, where the clock phase relationship is unique from one another. It is also shown that the oscillation mode of FRO is determined by the strength of the feedforward paths.

Using proposed FRO model, the theoretical limitation of FRO's oscillation frequencies are investigated. A five-stage resistor loaded FRO is optimized for the maximum oscillation frequency. The optimized FRO was fabricated using a typical 0.18μm CMOS technology. The FRO's oscillation frequency was measured to be from 9GHz to 16GHz, which is the highest among the 0.18μm FROs ever reported.

Then, the FRO model is extended to have more than one feedforward paths, namely, MFRO. Following the similar procedure, design

equations for MFRO model were derived. With the equations, the dominant oscillation mode and the oscillation frequency were predicted. The calculation results matched with the simulated MFRO's behavior very well.

Finally, a 10Gbps clock and data recovery circuit is designed using an eight-phase MFRO, and its measurement results are shown.

Keywords: Ring oscillator, feedforward ring oscillator, feedforward path, ring oscillator model, CDR, clock and data recovery

Chapter 1. Introduction

Electrical oscillators can be categorized into two groups by observing their structural formations; Oscillators with or without an explicit resonating device. The two groups of oscillators have very different characteristics in many aspects, for instance, oscillation frequency range, phase noise, die area, power consumption, etc. For that reason, they rarely share applications.

RF engineer prefers LC-tank oscillators over ring oscillators for their projects, because LC-tank oscillator generates very clean carrier signals while a ring oscillator is noisy [1]. In the other hand, for clock multiplier units of microprocessor clocked in a moderate speed, a tiny ring oscillator is preferred because the phase noise requirement for a microprocessor is not that strict [2]. Also, for a clock multiplying unit, only a small die area is permitted since highly efficient area utilization is usually important for low fabrication cost.

In this chapter, the two types of oscillators mentioned are briefly overviewed.

1-1. Oscillators with an explicit resonator

A resonator is a device that exhibits oscillation behavior at some frequencies, called its resonance frequencies. A tuning fork is one of the best examples of resonator. A tuning fork is a mechanical resonator, and when it is hit, it generates a tone in its resonance frequencies [3, 4].

Hitting a tuning fork makes the forks bend slightly, that is, some amount of kinetic energy transferred into the tuning fork and is stored in the fork's stressed structure as a form of potential energy. Then, the

potential energy makes the forks restore into their original shapes, that is, the potential energy is transferred into kinetic energy back again. As a result, the forks vibrate and generate acoustic waves. The resonance frequency depends on the fork's physical characteristics, for instance, mass, elasticity, and so on.

In an electrical resonator, electrical energy is stored in forms of electrical voltage and current (or electric and magnetic fields) [4]. LC-tank circuit or cavity resonator is a good example. Varying voltage (electric field) in a resonator induces current (magnetic field) and vice versa, implying that the energy stored in one form is transferred to the other. If we assume that there is no loss in the energy transfer, this energy transferring process can be modeled and described using a simple second-order differential equation:

$$\frac{d^2V(t)}{dt^2} + kV(t) = 0 \qquad (1\text{–}1)$$

, where k is a proportional constant. In fact, equation (1–1) is a famous equation in analysis of electrical oscillators as well as mechanical oscillators, known as harmonic oscillators. The natural response of V in (1–1) is sinusoidal function with an angular frequency of square root of k. Indeed, the solution implies an oscillatory output V, and it may represents voltage, current, electric field or magnetic field.

In reality, every energy–transfer accompanies some degree of energy loss proportional to the total amount of energy transferred. Equation (1–1) is modified to include energy loss:

$$\frac{d^2V(t)}{dt^2} + c\frac{dV(t)}{dt} + kV(t) = 0 \quad . \tag{1–2}$$

If the coefficient c, accounting for the energy loss, is small enough to satisfy an inequality 4k–c2>0, the natural response of V in equation (1–2) becomes an under-damped sinusoidal function with a slightly lower oscillation frequency than that of equation (1–1), square root of k:

$$V(t) = Ae^{-\frac{c}{2}t}\sin(\frac{\sqrt{4k-c^2}}{2}t + \phi) \quad . \tag{1–3}$$

If the energy loss is so large that it does not satisfy the inequality 4k–c2>0, the natural response of V becomes an exponentially decaying function and does not show any oscillatory response.

Generally, quality factor, denoted as Q, is popularly used for a measure of energy loss in a resonator. The quality factor is defined as

$$Q = \frac{2\pi \times Energy\ stored}{Energy\ dissipated\ \ per\ cycle} = \frac{\sqrt{k}}{2c} \quad . \tag{1–4}$$

Because of the energy loss, a resonator itself can be an oscillator. The natural response, that is, oscillating voltage and current, of an electrical resonator will eventually die out if additional energy is not supplied. The energy stored in the resonator will be dissipated on every oscillation cycle. To achieve a continuous oscillation with a resonator, some energy supplement is required to compensate the energy lost.

In most cases, electronic resonator can be modeled as parallel or series lumped RLC circuit as shown in figure 1–1 [5]. It consists of a

resistor R, an inductor L and a capacitor C. The electrical energy stored in a resonator is repeatedly transferred between the two energy storage devices, the inductor L and the capacitor C, while some fraction of the energy is dissipated in the resistance R.

The resistance R in an electrical resonator model can be neutralized by a negative–resistance circuit as shown in figure 1–2. It pumps up and drains out some electric charges to compensate the energy dissipated in R and to maintain the total amount electric energy stored in the resonator to a certain level.

To study electrical resonator and its resonance behavior, frequency–domain analysis is usually preferred over time-domain analysis. It is because an electrical resonator is essentially a frequency–domain filter. More specifically, it is a band–pass filter whose bandwidth is determined by the quality factor, Q.

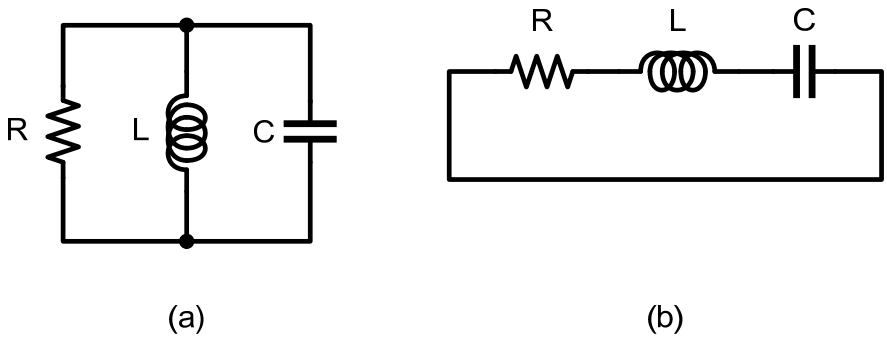

Figure 1-1. (a) Parallel RCL circuit. (b) Series RLC circuit.

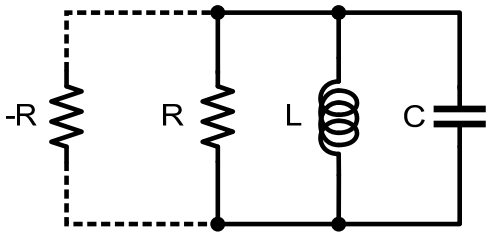

Figure 1-2. A resonator based oscillator model. Energy supplement circuit is depicted as a negative resistance.

1-2. Oscillators without an explicit resonator

There is another type of widely-used oscillator. It is generally called ring oscillator (RO) [2]. A RO do not need a resonator device, instead, it consists of delay elements which are connected back-to-back to form a loop structure as shown in the figure 1–3. The delay elements can be implemented in differential-ended structure in figure 1–3(a) as well as in single-ended structure in figure 1–3(b).

Basically a RO is a delay line whose output is positively feed-backed into its input terminal. The signal travelling through the delay line is added to its feed-backed component. If the open loop delay is the same to a half period of the traveling signal and the loop gain in larger than one, the signal builds up in its amplitude and results in oscillation. Consequently, a RO's oscillation frequency can be predicted using the delay element's propagation delay, t_d.

$$f_{OSC} = \frac{1}{2Nt_d} \tag{1–5}$$

, where N is the number of delay elements in the RO. Usually simple first-order buffer circuit or CMOS inverter circuit are utilized for the delay elements, and their schematic diagrams are shown in figure 1–4.

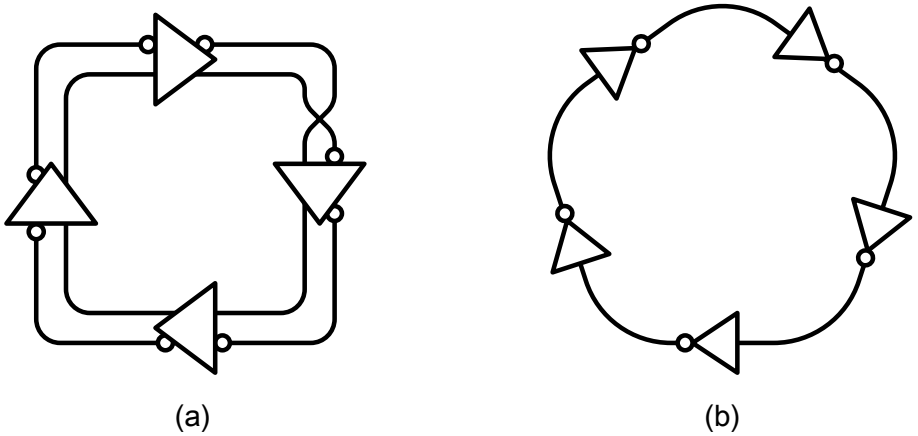

Figure 1-3. Schematic diagram of typical ROs. (a) A four-stage differential-ended RO. (b) A five-stage single-ended RO.

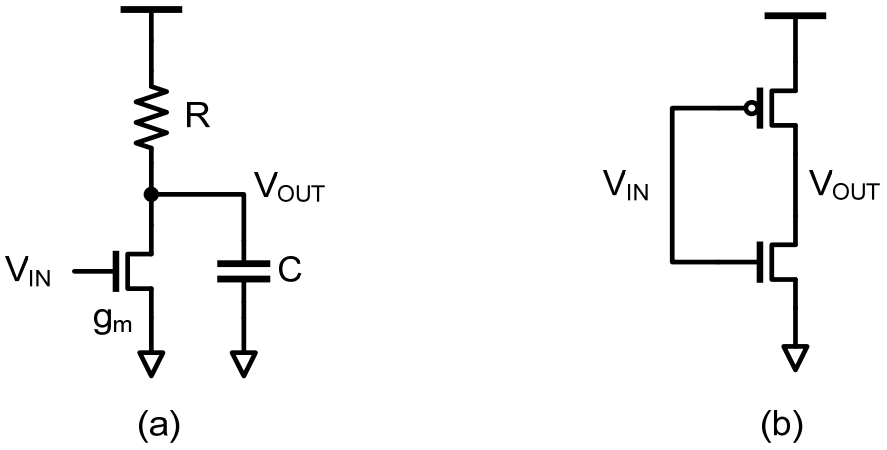

Figure 1-4. Simple first-order inverter circuits. (a) A resistor-loaded inverting amplifier with load resistance C. (b) CMOS inverter.

Assuming the output resistance of the NMOS transistor r_{ds} is much larger than R, the propagation delay of the inverting amplifier in figure 1–4(a) is the same to the RC time constant at the output terminal. Then, the oscillation frequency is found as

$$f_{OSC} = \frac{1}{2NRC} . \qquad (1–6)$$

The oscillation frequency also can be determined by the delay element's frequency response. The transfer function of the first-order amplifier is

$$H(\omega) = \frac{-g_m R}{1 + j\omega RC} \qquad (1–7)$$

The negative sign of the numerator shows that the transfer function H(ω) is for an inverting amplifier. In an N–stage RO, each delay element has to contribute a frequency dependent phase shift of π/N, from the transfer function's denominator 1+jωRC, to the total loop delay of 2π. That is,

$$\tan^{-1}(\omega_0 RC) = \frac{\pi}{N} \quad \text{and} \quad \omega_0 RC = \tan(\pi/N) \qquad (1–8)$$

Another phase shift of π comes from the inversed polarity of the feed-backed signal to complete the total phase shift of 2π. Note that the four-stage differential-ended RO in figure 1-3(a) has a twisted signal path to invert the signal polarity. In the five-stage single-ended RO in figure 1-3(b), the signal polarity is inversed odd number of times during a loop trip, leading a phase shift of π.

The oscillation frequency is determined using (1–8).

$$f_{OSC} = \frac{\tan(\pi/N)}{2\pi RC} \tag{1–9}$$

If N is large enough, f_{OSC} in (1–9) can be approximated to (1–6).

For a high frequency oscillator, R, C and N should be minimized. The minimum value of N is limited to three. The load capacitor C typically consists of output and input capacitances of the inverter. They can be minimized by using optimized layout but there exist a hard limit which depends on the process technology. The only parameter we can control with ease is the load resistance R, and it is commonly used for control the oscillation frequency of RO with resistor–loaded inverting amplifier.

The minimum value of R to achieve the maximum oscillation frequency f_{MAX} with N–stage RO can be determined as follows.

$$\begin{aligned} \left|H(\omega_{MAX})\right| &= \frac{g_m R_{MIN}}{\sqrt{1+(\omega_{MAX} RC)^2}} = 1 \\ R_{MIN} &= \frac{\sqrt{1+(\omega_{MAX} RC)^2}}{g_m} = \frac{\sqrt{1+\tan^2(\pi/N)}}{g_m} = \frac{1}{g_m \cos(\pi/N)} \end{aligned} \tag{1–10}$$

Then, substituting R in (1–9) with R_{MIN} in (1–10), we have

$$f_{MAX} = \frac{g_m \sin(\pi/N)}{2\pi C} \sim f_T \sin(\pi/N). \tag{1–11}$$

Finally, the maximum achievable oscillation frequency given by (1–11) and the required minimum DC gain per delay element for N=3~10 are plotted in figure (1–5).

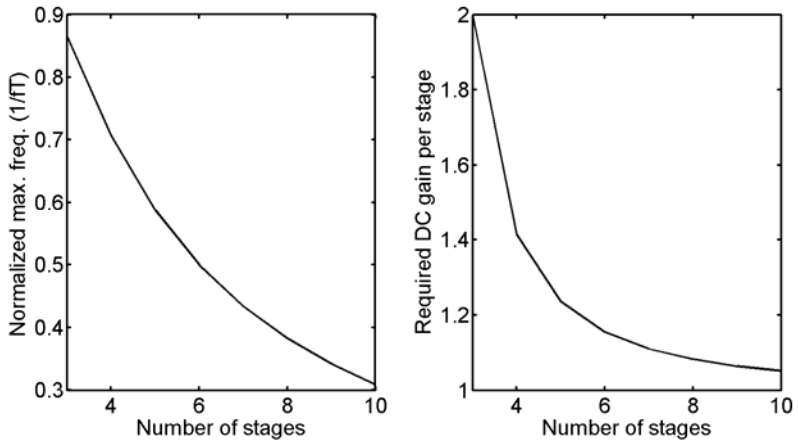

Figure 1-5. Maximum achievable oscillation frequency and the required minimum DC gain per delay element.

The oscillation frequency f_{OSC} in equation (1–11) firmly limit the maximum oscillation frequency achievable with conventional ROs f_{MAX}.

In the other hand, when a CMOS inverter in figure 1–4(b) is utilized for the delay element, the load resistance R is not a controllable design parameter and is determined by the MOS transistors' output resistances, r_{ds}, which is inversely proportional to the channel length of the MOS transistor. We will call this type of RO CMOS RO, hereafter. Then, the minimum value of R is limited by the minimum channel length that the fabrication process can support. In a typical 0.18-μm CMOS processes, the minimal–sized inverter's DC gain is around 15, which is much larger than those for the high frequency RO in figure 1–5(b). In this case, choosing small N is an only way to make it oscillate at high frequencies. Figure 1–6 and table 1–1 show the calculated oscillation frequency of CMOS RO, assuming that the CMOS inverter's DC gain is 15. The maximum achievable oscillation frequency is much lower than that of ROs with resistor–loaded inverting amplifiers.

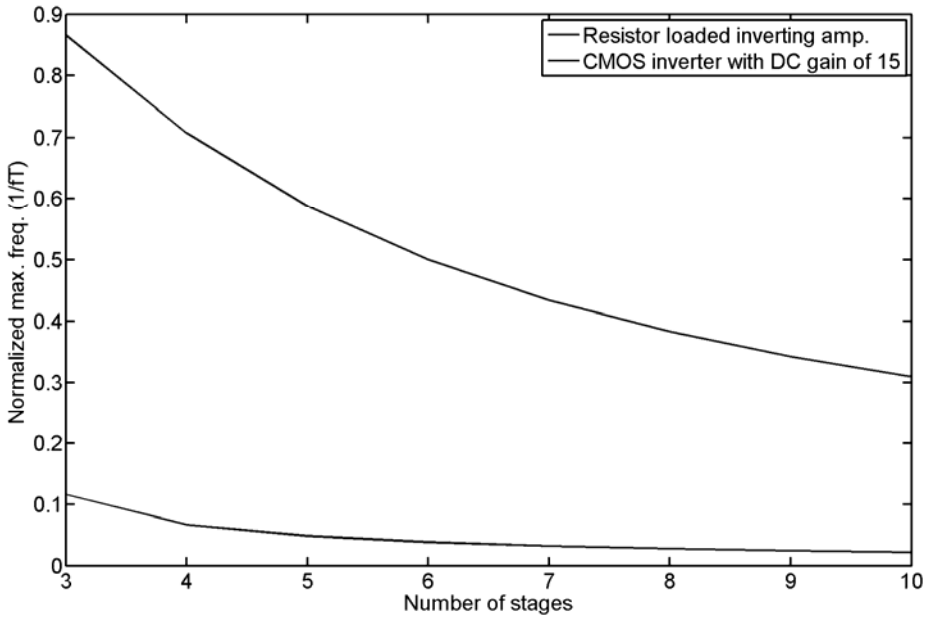

Figure 1-6. Calculated oscillation frequency of CMOS RO. The CMOS inverter's DC gain is assumed to be 15.

Table 1–1. Maximum achievable oscillation frequency of RO and CMOS RO.

N	3	4	5	6	7	8	9	10
Maximum achievable oscillation frequency, resistor-loaded SPRO, $(1/f_T)$.	0.866	0.707	0.588	0.5	0.434	0.383	0.342	0.309
Max. achievable oscillation frequency, CMOS SPRO with DC gain of 15, $(1/f_T)$.	0.116	0.067	0.048	0.039	0.032	0.028	0.024	0.022

In general, RO is regarded to be much slower than resonator-based oscillator. It is because a resonator is a passive device and its resonance frequency is not limited by the active devices, in this case, MOS transistors.

1-3. Comparison

ROs and resonator-based oscillators have very distinctive characteristics; required die area, phase noise, oscillation frequency, etc. For those reasons, they usually do not share many applications. For example, resonator-based oscillators are used for RF systems and high speed clock generation and ROs are used for low frequency clock generation where clock jitter requirement is moderate.

A major advantage of RO over an LC-tank oscillator is that it is much smaller. It is simply because it does not require a bulky resonating device that is sometimes occupies almost entire area of the oscillator. There is also another great advantage of RO, and that is it naturally produces a set of multiphase clock signal. Multiphase clock is highly useful especially for clock recovery, and other various applications.

Unfortunately, a RO usually has much larger phase noise than a resonator-based oscillator. Consequently, they are hardly used for RF systems where lower phase noise is essential.

Chapter 2. Feedforward Ring Oscillator Analysis

2-1. Introduction

A lot of researches have done to improve RO's oscillation speed, and several new structures of RO have been proposed.[6-15] Although these types of RO are called by several different names, for instance, dual delay path oscillators[7], sub-feedback oscillators[8], feedforward oscillators[14], etc., they make a distinctive feature of having feedforward paths in common. In this dissertation, we will call those RO structures feedforward ring oscillators (FROs), and conventional ROs single path ROs (SPROs).

FROs are very fast even compared with high frequency LC-tank oscillators [12], and some others utilize even-number-stage CMOS ROs[6, 8, 9, 14, 15], which are not realizable with conventional CMOS SPRO structure. Unfortunately, despite their usefulness and potential, FROs have not been analyzed thoroughly so far. In this chapter, a new FRO model is proposed and the analysis results are shown.

2-2. Oscillator structure

A typical structure of N-stage CMOS SPRO is shown in figure 2–1. N CMOS inverters are connected in a loop shape, and each node is named as ck_1~ck_N in a sequential order. If the delay stages are all identical, the structure is symmetric. More specifically, the oscillator structure is symmetric for node index shifting. With symmetry structures, a unit stage can be defined as the smallest identical building block of the oscillator, in this case, a single CMOS inverter. The whole RO can be reconstructed using the unit stages.

Analyzing the unit stage is much easier rather than the whole oscillator, while the analysis result of the unit stage still accounts for the entire RO's operation, therefore, ROs are designed in a symmetric structure almost every time. The unit stage of the oscillator in figure 2–1 is shown in figure 2–2.

The input and the output are noted as ck_{i-1} and ck_i, respectably, where i is an integer number between 1 and N. i=1 is an exception where ck_N becomes the input, since the RO is in a closed-loop form.

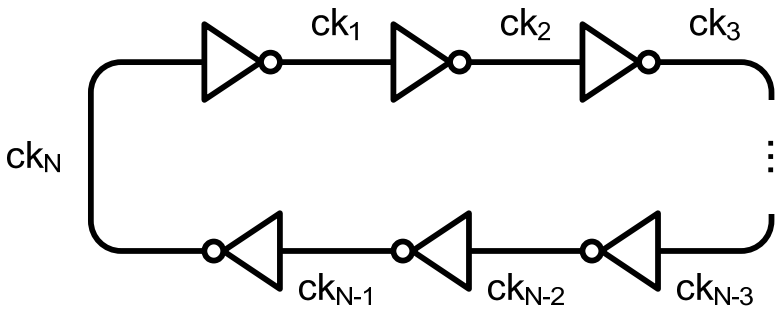

Figure 2-1. Schematic diagram of a typical N-stage CMOS SPRO.

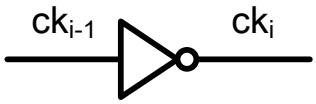

Figure 2-2. Unit stage of CMOS RO

2-3. Oscillation Modes of RO

If the N-stage RO is oscillatory, it implies that there exists at least one non-zero solution for the oscillator's natural response. Since the oscillator is symmetric for node index shifting, the responses of ck_1~ck_N should be also symmetric for the same operation. The simplest solution for the response is sinusoidal function.

$$ck_i = A\sin\left(2\pi f_0 t + \theta i + \varphi\right) \qquad (2\text{–}1)$$

, where f_0 is the oscillation frequency, A is amplitude and φ is an arbitrary phase offset. θ is phase difference between ck_i and ck_{i-1}, that is, output and input of the unit stage. Then, single circular trip around the loop results in a phase shift of 2π or a multiple of 2π.

$$\theta N = 2\pi k \quad \text{and} \quad \theta = \frac{2\pi k}{N} \qquad (2\text{–}2)$$

, where k is an integer number. It should be noted that we have used only the frequency-dependent portion of phase shift, $\tan^{-1}(\omega RC)$, to derive the oscillation frequency in the previous chapter. The frequency independent portion of phase shift π of the unit stage is not explicitly shown in the derived oscillation frequency. In this case, the θ accounts for total amount of phase shift in the unit stage including $\tan^{-1}(\omega RC)$ and all other phase shift. This will be discussed soon in this chapter.

We can find N-1 unique θs, and they are: 2π/N, 4π/N, 6π/N, … , 2(N–1)π/N. The other θs that are larger than 2(N–1)π/N are excluded because they are actually the same to one of those listed above after a modular operation with 2π.

With the N–1 θs, ck_1~ck_N in (2-1) can be rewritten in phasor forms:

$$CK_i = A\angle(\theta i + \varphi) \qquad (2\text{–}3)$$

Since the frequency dependence of CK_i is removed and it has only the amplitude A and the phase $\theta_i+\varphi$, it can be depicted in polar coordinate system. For example, CK_1~CK_5 of a five-stage RO for each θ are shown in figure 2-3. A five-stage RO has four θs: 2π/5, 4π/5, 6π/5, 8π/5.

The four phase relationships in figure 2-3 are all unique and not the same to the others. Then, we can define an oscillation mode for each phase relationship. Each θ corresponds to an oscillation mode. For convenience, we indexed the four oscillation mode in a sequential order; Mode 1 with θ=2π/5, mode 2 with θ=4π/5, mode 3 with θ=6π/5 and mode 4 with θ=8π/5.

Also, this observation can be generalized for an arbitrary number stage RO: an N-stage RO has N–1 unique oscillation modes.

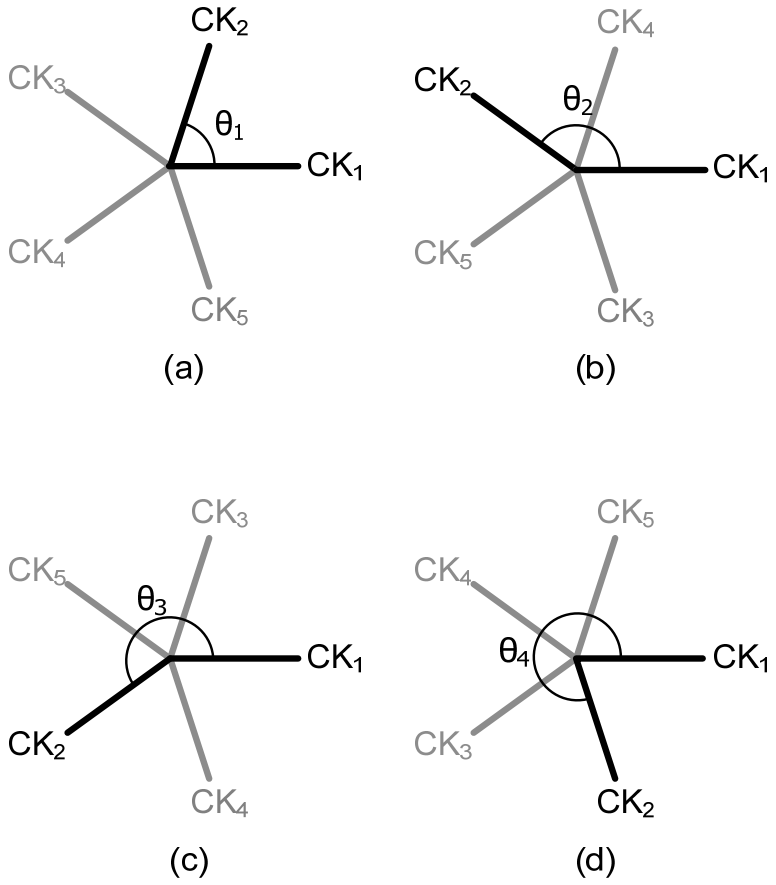

Figure 2-3. Four θs of a five-stage RO.

(a) Oscillation mode 1, θ=2π/5. (b) Oscillation mode 2, θ=4π/5.

(c) Oscillation mode 3, θ=6π/5. (d) Oscillation mode 4, θ=8π/5.

Conventional RO analysis usually does not consider multiple oscillation modes [16]. It is simply because only one oscillation mode appears in a SPRO, but it is worthwhile to have some closer look at RO's multi mode nature.

Figure 2–4 and table 2-1 show possible oscillation modes for N-stage RO. The oscillation mode for SPRO is marked with arrows in the figure and with asterisk in the table. A CMOS inverter provides a limited range of phase shift, π to $\pi/2$, colored in grey in the figure and the table, so the oscillation modes with a phase shift out of this range can never appear in a CMOS SPRO. With N=3 and 5, there is only one oscillation mode each is possible with $\theta=\pi/3$ and $\theta=2\pi/5$ respectably. With N=7 and 9, there are two oscillation modes for each colored in grey, hence two oscillation modes. In this case, only the oscillation mode with smaller oscillation frequency appears in reality, because it has larger amplitude response and it will overwhelm the other mode. For convenience, we will call the very oscillation mode the dominant mode. For an even number N, the $N/2^{th}$ mode with $\theta=\pi$ are always dominant. However, in those cases with even number of stages, since the dominant modes are found at the zero frequency response, the even number stage SPROs will rather latch up than oscillate.

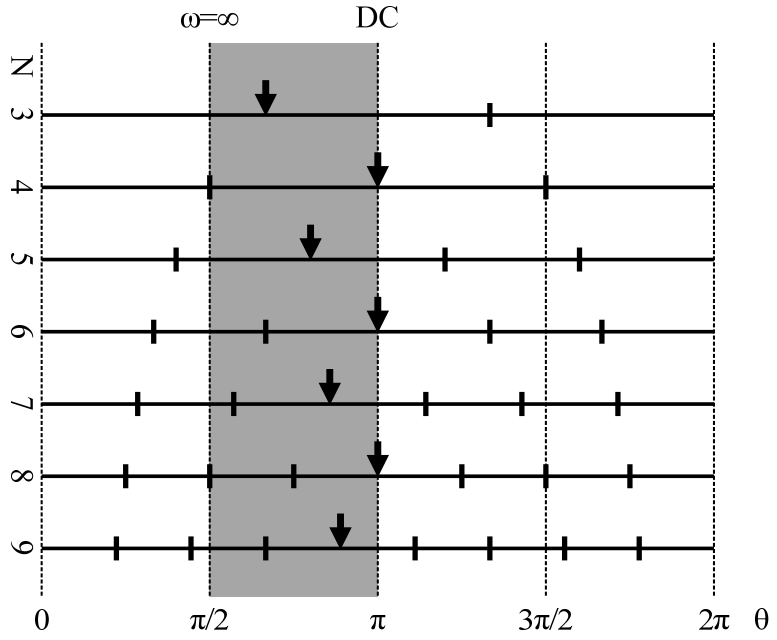

Figure 2-4. Possible oscillation modes of an inverter-based N-stage ROs (N=3~9).

Table 2-1. Possible oscillation modes of an inverter-based N-stage ROs (N=3~9).

N	3	4	5	6	7	8	9
Mode 1	2π/3*	π/2	2π/5	π/3	2π/7	π/4	2π/9
Mode 2	4π/3	π*	4π/5*	2π/3	4π/7	π/2	4π/9
Mode 3	N/A	3π/2	6π/5	π*	6π/7*	3π/4	2π/3
Mode 4	N/A	N/A	8π/5	4π/3	8π/7	π*	8π/9*
Mode 5	N/A	N/A	N/A	5π/3	10π/7	5π/4	10π/9
Mode 6	N/A	N/A	N/A	N/A	12π/7	3π/2	4π/3
Mode 7	N/A	N/A	N/A	N/A	N/A	7π/4	14π/9
Mode 8	N/A	N/A	N/A	N/A	N/A	N/A	16π/9

*represents the dominant mode and the corresponding θ.

This discussion is summarized as follows:

--First, if a SPRO has only one oscillation mode that satisfies the phase and gain conditions, it appears and is the dominant mode.

--Second, if a SPRO has two or more valid oscillation modes that satisfy the phase and gain conditions, the one with the largest amplitude response appears and is the dominant mode.

-- Third, if a SPRO has even number stages, it latches up and does not oscillate because the $N/2^{th}$ mode with $\theta=\pi$ at zero frequency is the dominant mode.

The second and third argument above implies that if the amplitude response of the unit stage is modified to have larger gain at high frequency than at low frequency, the CMOS RO can oscillate at higher frequency than a conventional CMOS RO does. It also suggests that if the amplitude response at zero frequency is lowered below that of the high frequency mode, an even number stage RO can oscillate.

In the next section, it is shown that adding feedforward paths to a SPRO actually changes the amplitude response of the unit stage, and FROs operate in different oscillation mode than SPROs.

2-4. Analysis of FRO

Figure 2–5 shows an example of FRO. It is constructed by adding additional feedforward paths to a five-stage SPRO. The feedforward paths are drawn in dashed lines. This FRO can oscillate at much higher frequency than a five-stage SPRO can.

FROs are sometimes called coupled oscillator, because more than one RO structures are found in the structure, and they are merged into one FRO. For instance, in figure 7, seven closed-loops are found:

--The outer loop (ck_1 - ck_2 - ck_3 - ck_4 - ck_5 - ck_1)

--The inner loop (ck_1 - ck_3 - ck_5 - ck_2 - ck_4 - ck_1)

--Five three-stage loops (ck_1 - ck_3 - ck_4 - ck_1, ck_2 - ck_4 - ck_5 - ck_2, and so on).

It may not be impossible but it will be quite difficult to analyze the oscillator by studying the interaction between the coupled seven SPROs. Instead, we will begin the analysis by defining a unit stage structure.

Recall that an N-stage RO has N nodes, namely, ck_1~ck_N. For a conventional SPRO, a unit stage can be defined as a single delay stage, a CMOS inverter, as shown in figure 2–6(a). ck_i is determined solely by ck_{i-1}.

Unit stage for the FRO in figure 2–5 is found as shown in figure 2–6(b). It consists of two CMOS inverters and has two inputs each from ck_{i-1} and ck_{i-2}. Feedforward path is depicted in dashed line, from ck_{i-2} to ck_i. For convenience, we will call the path from ck_{i-1} to ck_i (solid line) direct path, in contrast with the feedforward path from ck_{i-2} to ck_i (dashed line). Superimposed numbers, 1 and α, over the inverters of each path denote the inverter's scaling factor. The direct path's inverter is assumed to be in the unit size, and then the feedforward path's inverter is scaled by a factor of α. Note that a CMOS inverter's driving strength is proportional to its size, therefore, α also represents the ratio of feedforward path's driving strength to that of the direct path.

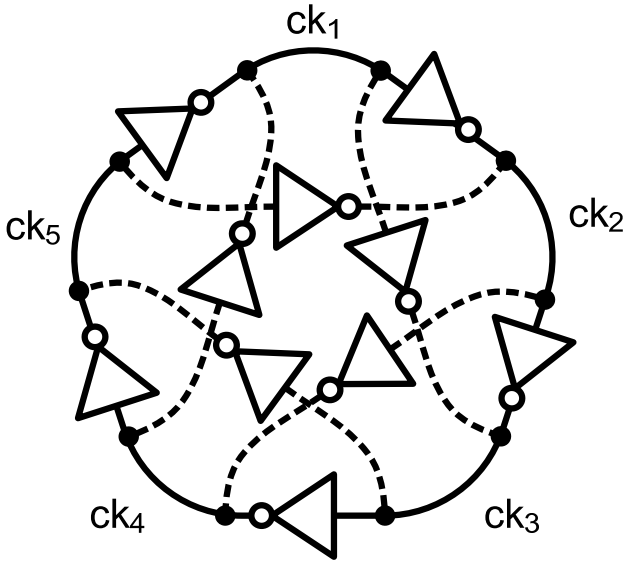

Figure 2-5. Five-stage feedforward ring oscillator

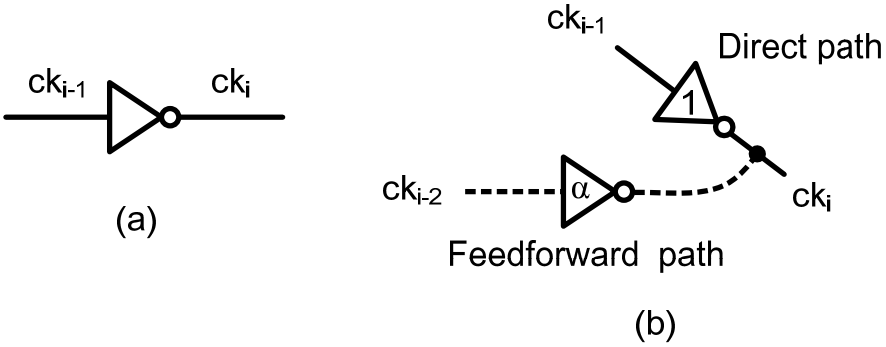

Figure 2-6. Unit stage structures. (a) Conventional single path RO. (b) Five-stage FRO.

A small signal equivalent circuit of a CMOS inverter is shown in figure 2–7. It consists of a transconductance g_m, output resistance R and load capacitance C. Depicted as a single capacitor, the capacitance C includes output capacitance as well as the input capacitance of the next stage.

The transfer function is found as:

$$H(\omega) = \frac{-g_m R}{1 + j\omega RC}. \qquad (2\text{–}4)$$

A small signal equivalent circuit of the unit stage of five-stage FRO in figure 2–6(b) can be easily found using the small signal equivalent circuit of the inverter. It is shown in figure 2–8.

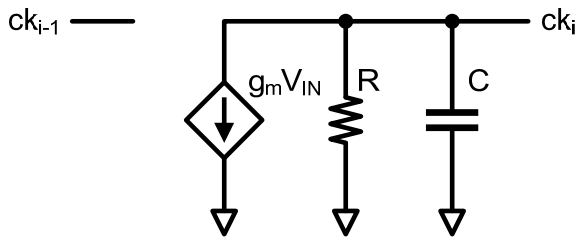

Figure 2-7. A small signal equivalent circuit of an inverter

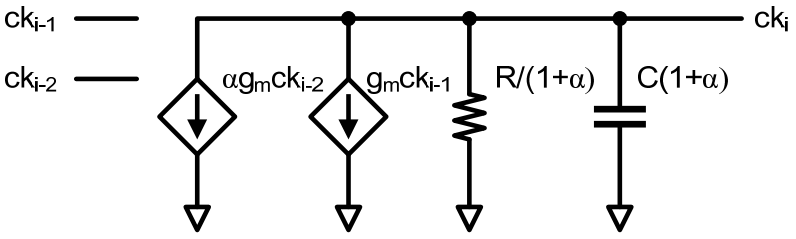

Figure 2-8. A small signal equivalent circuit of an inverter

It has two trans-conductors; g_m from the direct path and αg_m from the feedforward path. The output resistance and the load resistance are connected parallel and their resultant values are R/(1+α) and C(1+α), respectably. Note that the time constant at the output ck_i stays the same to that of the unit-sized inverter, RC.

Total amount of current drawn by the two trans-conductors is:

$$I = -\left(g_m ck_{i-1} + \alpha g_m ck_{i-2}\right) \tag{2–5}$$

The phasor forms of ck_i are:

$$CK_i = A\angle\left(\theta i + \varphi\right) \tag{2–6}$$

CK_i is found by multiplying the output impedance to (2-4):

$$CK_i = \frac{-g_m R\left(CK_{i-1} + \alpha CK_{i-2}\right)}{\left(1+\alpha\right)\left(1+ j\omega RC\right)} \tag{2-7}$$

From (2–6) and (2–7), we have:

$$CK_i = \frac{-g_m R\left(1+\alpha\angle-\theta\right)}{\left(1+\alpha\right)\left(1+ j\omega_0 RC\right)} CK_{i-1}$$

$$= \frac{-g_m R\left(1+\alpha\cos\theta - j\alpha\sin\theta\right)}{\left(1+\alpha\right)\left(1+ j\omega_0 RC\right)} CK_{i-1}, \tag{2–8}$$

$$= \frac{-g_m R_{EQ}\left(X + jY\right)}{\left(1+ j\omega_0 RC\right)} CK_{i-1}$$

, where $X=1+\alpha\cos\theta$, $Y=-\alpha\sin\theta$ and $R_{EQ}=R/(1+\alpha)$. It is interesting to observe that (2–8) describes the unit stage as a single-input amplifier. Because we already have assumed that the oscillation frequency is ω_0, the new transfer function H can be a function of only α.

$$H(\alpha)=\frac{-g_m R_{EQ}(X+jY)}{(1+j\omega_0 RC)} \tag{2–9}$$

The imaginary part in the numerator of H(α) implies an additional phase shift is applied to the output. The phase shift caused by the numerator does not depend on ω_0 but only on α, the feedforward ratio, hence frequency-independent phase shift. The denominator of H(α) also causes a phase shift in output, $-\tan^{-1}(j\omega_0 RC)$, which is dependent on the oscillation frequency, ω_0. Let us define those two phase shifts as β and γ, respectably.

$$\beta=\begin{cases}\tan^{-1}(Y/X), \text{ if } X>0\\ \tan^{-1}(Y/X)+\pi, \text{ if } X<0\end{cases}, \text{ where } \frac{Y}{X}=\left(\frac{-\alpha\sin\theta}{1+\cos\theta}\right) \tag{2–10}$$

$$\gamma=-\tan^{-1}(\omega_0 RC). \tag{2–11}$$

The arch tangent function $\tan^{-1}(Y/X)$ alone cannot provide the correct β when X is negative. In other words, it maps the whole Cartesian plane to only the right half of the polar plane, therefore, the addition with π in (2–10) is required to find a proper β from Y/X. In case of γ, (2–11) gives a proper result since $\omega_0 RC$ is always positive.

The following conditions should be sufficed for oscillation. The oscillation conditions are:

--First, H(α) provides a phase shift of θ.

--Second, Frequency dependent phase shift γ should be within the range that an first-order inverter circuit can produce, namely, 0~–π/2.

--Third, H(α) has amplitude response equal to or larger than one.

From the first condition, we have:

$$\theta = \pi + \gamma + \beta \tag{2–12}$$

, where the π on the right side represents the signal polarity inversion.

From the second condition, we have

$$-\frac{\pi}{2} < \gamma = \theta - \beta - \pi < 0 \tag{2–13}$$

From the last condition, we have

$$\left|H\left(\alpha\right)\right| \geq 1 \tag{2–14}$$

Equation (2-12) and the phase relationship is depicted in figure 2–9. The arrows colored in grey are found by applying the two inputs, CK_{i-1} and CK_{i-2}, individually. Then, the output signal CK_i can be found by adding the two individual grey-colored outputs.

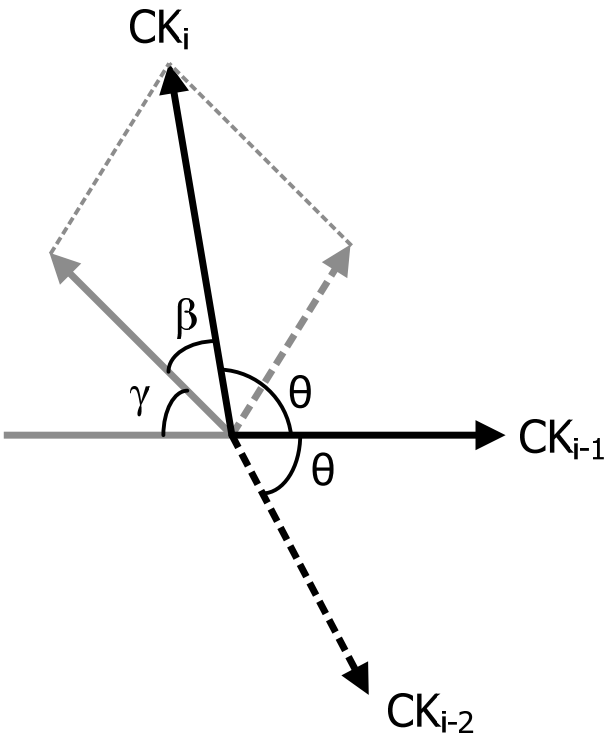

Figure 2-9. The phase relationship of the inputs and the output of the unit stage in oscillation.

From (2–11) and (2–12), we have:

$$\omega_0 RC = -\tan(\gamma) = -\tan(\theta - \beta - \pi) = -\tan(\theta - \beta) \tag{2–15}$$

Note that $-\pi/2 < \gamma < 0$, therefore $-3\pi/2 < \theta - \beta < -\pi$. In other words, γ is on the fourth quad and $\theta - \beta$ is on the second quad of the Cartesian plane.

To find $|H(\alpha)|$ in a simplified form, substituting ω_0 in (2–9) with (2–15) gives:

$$\begin{aligned} |H(\alpha)| &= g_m R_{EQ} \sqrt{\frac{X^2 + Y^2}{1 + \tan^2(\theta - \beta)}} \\ &= -g_m R_{EQ} \sqrt{(X^2 + Y^2)} \cos(\theta - \beta) \\ &= -g_m R_{EQ} \sqrt{(X^2 + Y^2)} (\cos\beta\cos\theta + \sin\beta\sin\theta) \\ &= -g_m R_{EQ} (X\cos\theta + Y\sin\theta) \end{aligned} \tag{2–16}$$

, where the negative sign is added since $\cos(\theta - \beta)$ has a negative value. Restoring X and Y in (2–16) with $X = 1 + \alpha\cos\theta$ and $Y = -\alpha\sin\theta$, we have

$$\begin{aligned} |H(\alpha)| &= -g_m R_{EQ} [(1 + \alpha\cos\theta)\cos\theta - \alpha\sin\theta\sin\theta] \\ &= -g_m R_{EQ} (\cos\theta + \alpha\cos 2\theta) \\ &= -\frac{g_m R}{1 + \alpha} (\cos\theta + \alpha\cos 2\theta) \end{aligned} \quad . \tag{2–17}$$

Interestingly, a very simple description of |H(α)| can be found as a function of only α. Equation (2–15) can be modified to give a simple description of the oscillation frequency f_0.

$$f_0 = \frac{-\tan(\theta-\beta)}{2\pi RC} = \frac{\tan(\beta-\theta)}{2\pi RC} = \left(\frac{1}{2\pi RC}\right)\left(\frac{\tan\beta-\tan\theta}{1+\tan\beta\tan\theta}\right)$$
$$= \left(\frac{1}{2\pi RC}\right)\left[\frac{(Y/X)-\tan\theta}{1+(Y/X)\tan\theta}\right] = \left(\frac{-1}{2\pi RC}\right)\left(\frac{\sin\theta+\alpha\sin 2\theta}{\cos\theta+\alpha\cos 2\theta}\right) \quad (2\text{–}18)$$

|H(α)| and γ are calculated and plotted to find the range where they satisfy the oscillation conditions we suggested. Figure 2–10 shows the frequency dependent phase shifts γ and the amplitude responses of the four oscillation modes at the oscillation frequency ω_0. A typical DC gain of CMOS inverter, 15, is assumed. The horizontal dashed lines show the boundaries for oscillation conditions.

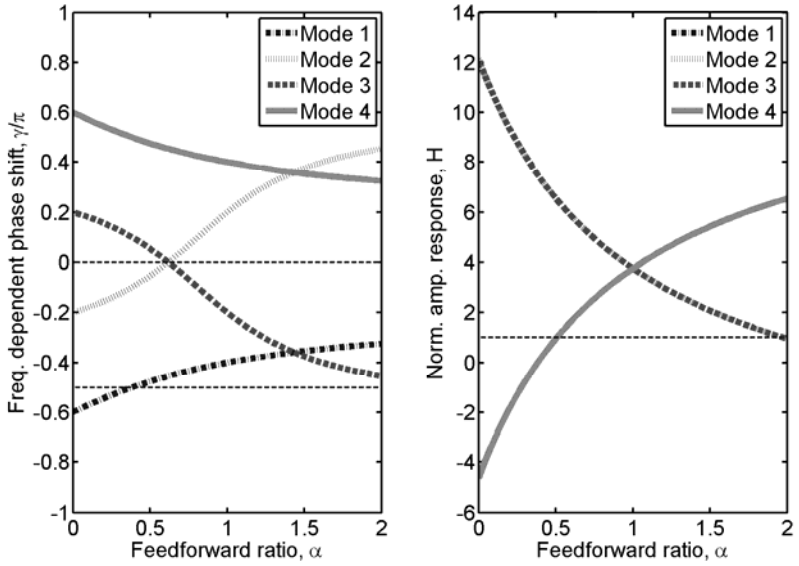

Figure 2-10.

Left: Frequency dependent phase shifts of the unit stage at the oscillation frequency ω_0. Phase shifts are normalized by π.

Right: Amplitude responses of the unit stage at the oscillation frequency ω_0. CMOS inverter's DC gain is assumed to be 15.

We have already made an assumption that is the FRO is oscillating at a certain frequency of ω_0. If there is invalid oscillation mode among the four oscillation modes at a given α, figure 2-10 will show some violations against the phase and gain conditions. Figure 2–11 shows the procedure in detail.

On the left side in figure 2–11, the oscillation modes which violate the phase shift condition are excluded. The frequency dependent phase shift γ should be in a range of $-\pi/2 \sim 0$. Then, we have mode 2 for $0 < \alpha < 0.35$, mode 1 and 2 for $0.35 < \alpha < 0.6$, mode 1 and 3 for $0.6 < \alpha < 1.2$ and mode 1 for $\alpha > 1.2$. On the right side, the gain conditions are examined. The amplitude response should be larger than one. In this case, we have mode 2, 3 for $0 < \alpha < 2$ and mode 1, 4 for $0.5 < \alpha$.

Then, by comparing the amplitude responses, the dominant oscillation mode can be determined. They are: mode 2 for $0 < \alpha < 0.6$, mode 3 for $0.6 < \alpha < 1$ and mode 1 for $\alpha > 1$. Mode 4 cannot satisfy the phase condition with α over a range of 0~2, therefore it can never appear.

Finally, the oscillation frequency can be calculated using (2–18). On the left side in figure 2–12 shows the calculated oscillation frequency and the dominant oscillation modes. The frequency is normalized with f_T, which is $g_m/2\pi C$ by our definition. On the right side in the figure, the simulated oscillation frequency is shown. The simulation was performed using HSPICE with a typical 0.18μm CMOS parameter.

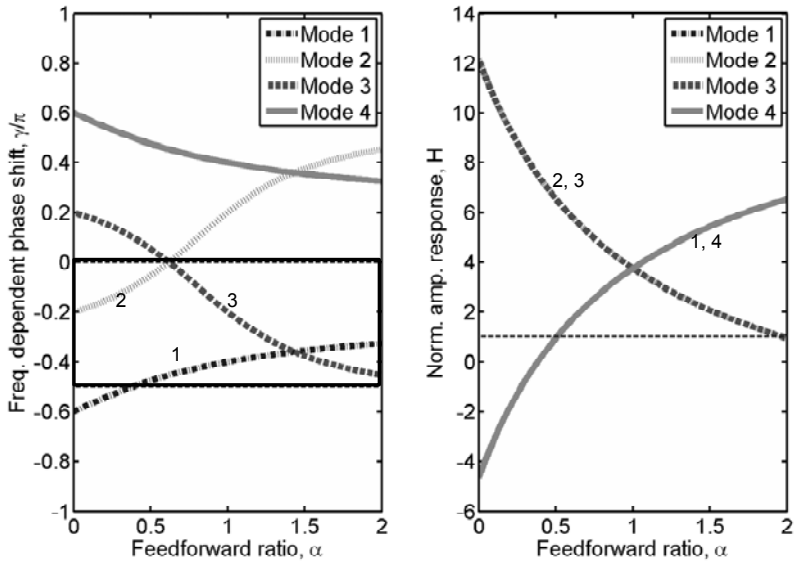

Figure 2-11. Left: The frequency dependent phase shift γ should be in a range between 0 and $-\pi/2$.

Right: Checking the gain condition. H(α) should be larger than one. If there are more than one oscillation modes satisfy the gain condition, choose the one with the largest gain

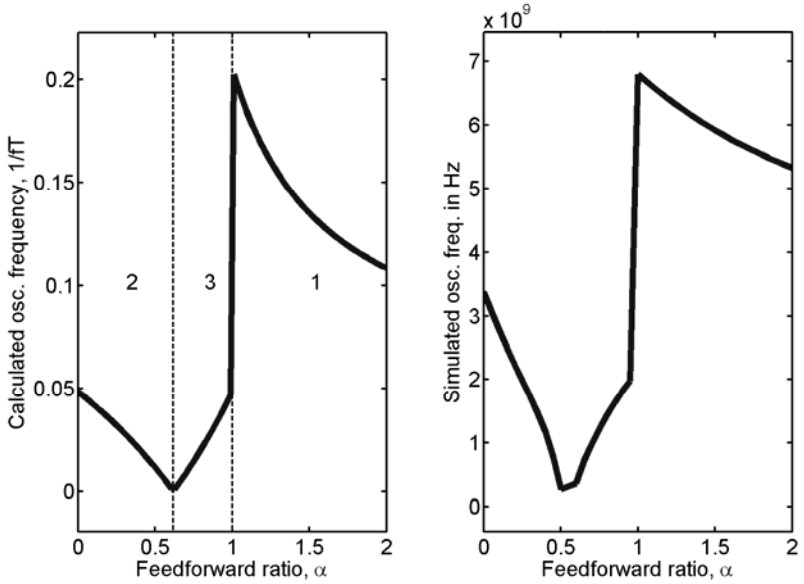

Figure 2-12.

Left: Determined dominant oscillation modes and corresponding oscillation frequency at a given α. The oscillation frequency is normalized by f_T.

Right: Simulated oscillation frequency at a given α. A typical 0.18-μm CMOS technology is used.

Chapter 3. More FRO analysis

The FRO model and analysis method we have discussed in the previous chapter is not limited to the five-stage FRO, and it can be applied to FRO with an arbitrary-number-stage. In this chapter, it is shown that the proposed model and analysis can successfully predict FROs behavior.

3-1. Even-number-stage FRO

ROs are usually constructed with simple inverters. One major disadvantage of SPRO is that the number of stage should be an odd integer. Otherwise, as we noted earlier, its output signal will rather be latched than oscillate. To avoid latching with even-number-stage ROs, the unit stage should have differential structure to achieve additional phase shift. For example, figure 3–1 shows a typical four-stage RO utilizes differential buffers as its unit stage. The signal polarity is inversed at the grey-colored fourth stage. Inverting signal polarity gives additional phase shift of π, consequently, each stage contributes a phase shift of $\pi/4$, which is an available phase shift achievable from a first-order buffer, to make a total phase shift around the loop 2π.

This observation implies that if an extra phase shift is achieved somehow, it becomes possible to realize an even-number-stage RO with inverter circuits. Adding feedforward paths to a conventional single path RO is one of the simplest solutions.

Four-stage FRO using single ended inverter circuit is shown in figure 3–2. The similar FRO structures have been shown in several publications [7-9, 15]. Although some of them provide good

explanation for its high-speed operation, they do not give quantitative guide lines with mathematical equations but only qualitative understanding about their oscillation principle. For example, the authors of [15] claims that the feedforward ratio of four stage FRO should be larger than 0.7 without explanation, which is true and agrees well with our calculation results shown below.

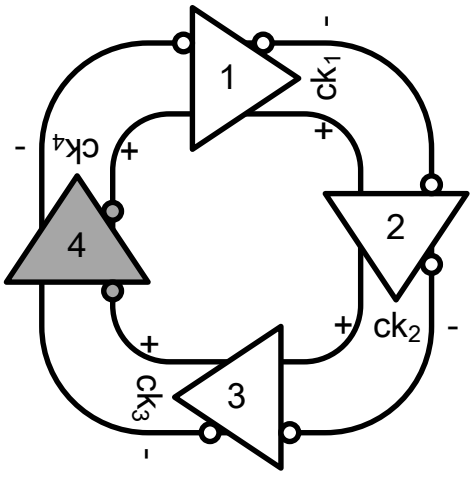

Figure 3-1. Schematic diagram of typical four-stage RO. It has differential buffer as its unit stage. The signal polarity is switched at the grey-colored stage.

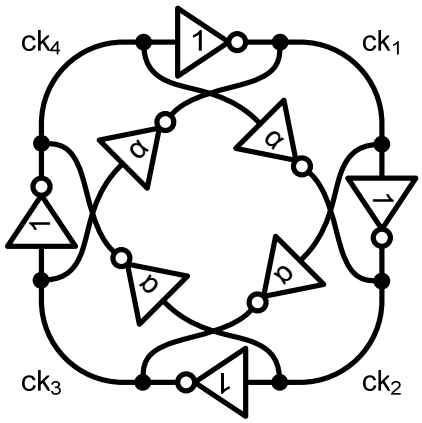

Figure 3-2. Schematic diagram of four-stage FRO.

Since the four-stage FRO in the figure has four delay elements, from the analysis method suggested in the previous section, it has three oscillation modes. The unit stage is the same to that of five-stage FRO we have analyzed. The phase relationship of the output signal CK_1~CK_4 in three oscillation modes are depicted in figure 3–3.

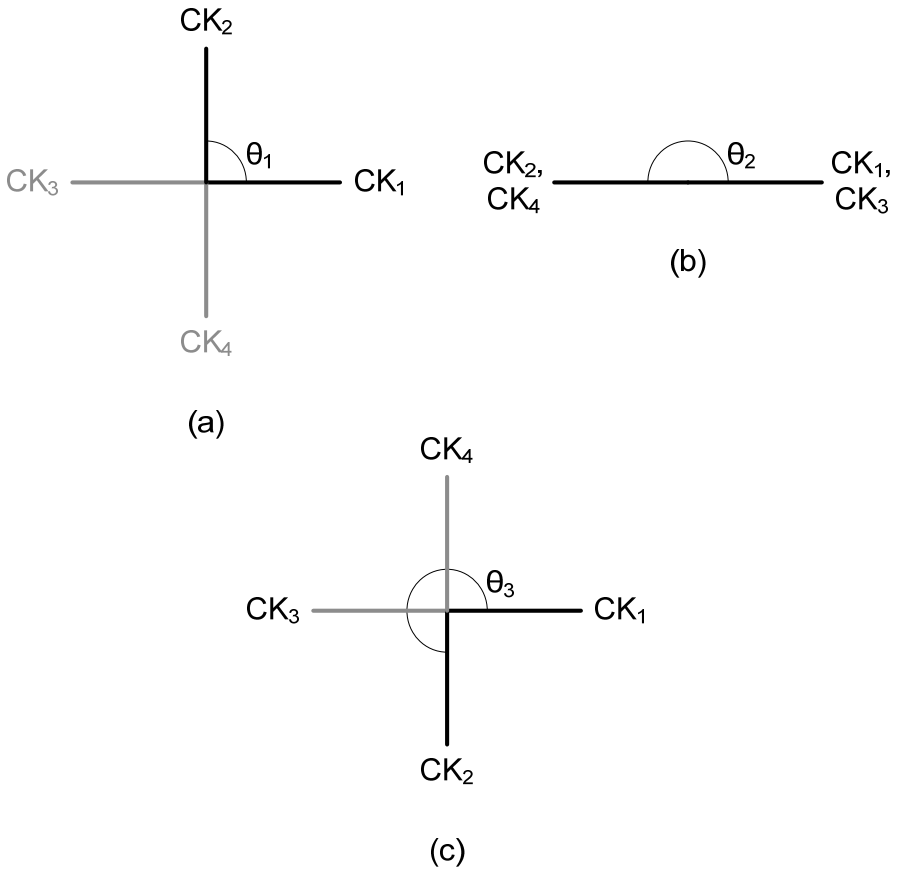

Figure 3-3. Possible oscillation modes of four-stage FRO. (a) Mode 1, θ=π/2. (b) Mode 2, θ=π. (c) Mode 1, θ=3π/2.

With each oscillation mode's θ, the unit stage's phase shift and gain response are calculated and plotted in figure 3–4.

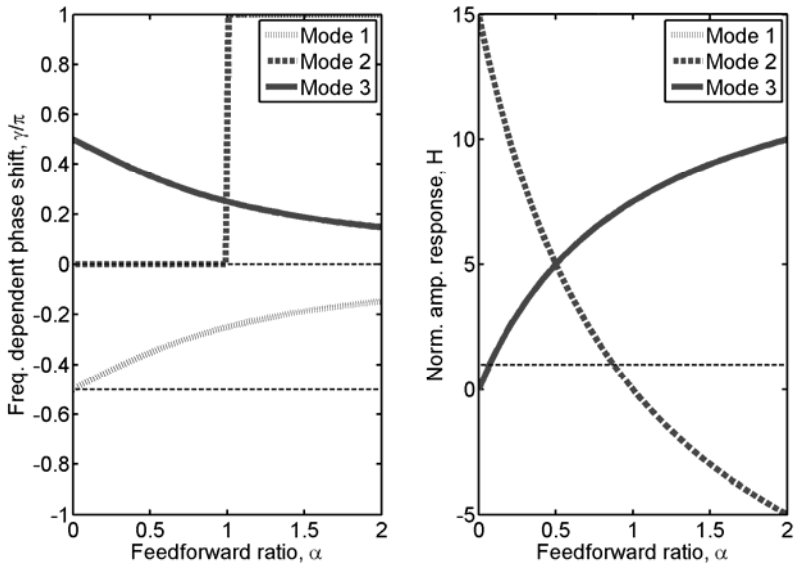

Figure 3-4.

Left: Phase shift in the unit stage of four-stage FRO. Zero phase shift of mode 2 implies that the oscillator latches up its output signal, hence no oscillation. Right: Unit stage gain of four-stage FRO. For an α larger than 0.5, mode 1 and mode 3 has a larger gain than that of mode 2.

Since an even number stage FRO can to latch up rather than oscillate, the latch-up conditions should be investigated carefully.

As shown in the figure, the frequency dependent phase shift γ is zero for $0 < \alpha < 1$ and π for $\alpha > 1$ in mode 2. The zero γ implies that the FRO does not oscillate at all, and it latches up the output signals.

In the other hand, if γ is π, it also implies that the FRO can latch up but it a different fashion. Figure 3–5(a) and (b) show that the two types of latch-ups that can possible occur in the four-stage FRO.

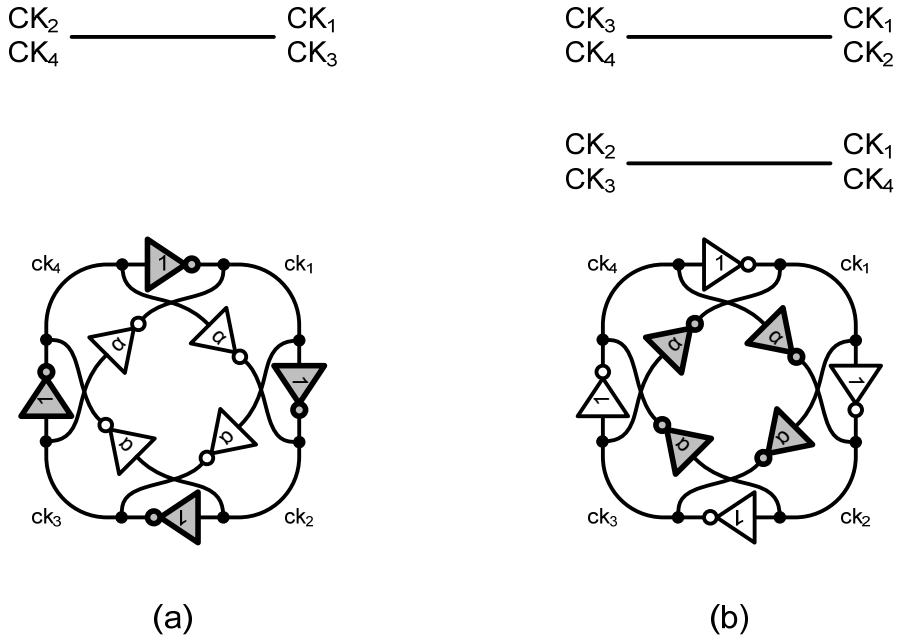

Figure 3-5. Two types of latch up
(a) Direct path latch up when the feedforward ratio α is smaller than 0.5.
(b) Feedforward path latch up when the feedforward ratio α is much greater than 1.

As shown in the figure, if feedforward paths are so strong that the FRO latches up, the assumption of symmetry that we have made is not valid any longer, since the phase difference θ between adjacent nodes are not uniform. Although it reveals the limitation of the proposed FRO model, it will be shown that a limited range of α over 0~2 does not cause feedforward path latch-ups and the proposed model still works very well.

The dominant oscillation mode can be determined following the procedure suggested in the previous chapter. On the left side in figure 3–6, the only mode that satisfies the phase shift condition is mode 1 and mode 2.

On the right side in the figure shows the comparison of unit stage's gain response in mode 1 and mode 2. When α is smaller than 0.5, mode 2 is dominant and when α is larger than 0.5, mode 1 is dominant, therefore, if α is larger than 0.5, the four-stage FRO will oscillate.

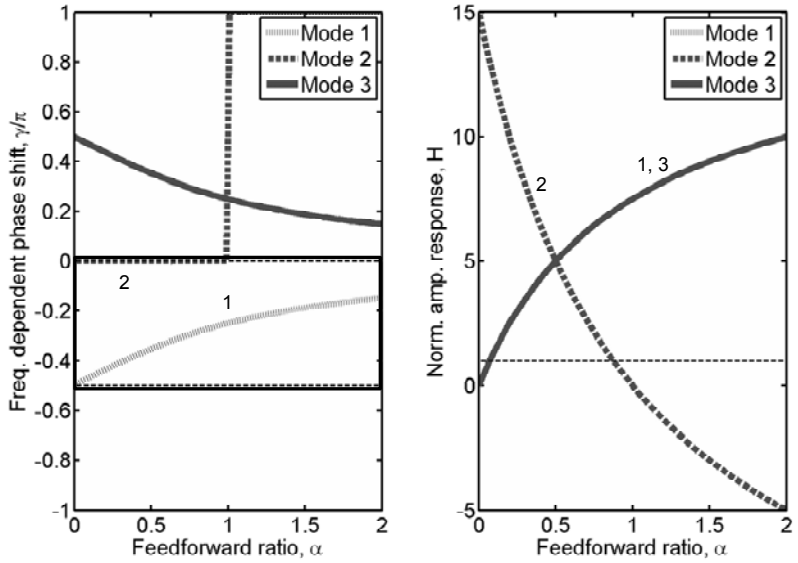

Figure 3-6.

Left: The frequency dependent phase shift γ should be in a range between 0 and π/2.

Right: Checking the gain condition. H(α) should be larger than one. If there are more than one oscillation modes satisfy the gain condition, choose the one with the largest gain.

Four-stage FRO is simulated with a standard 0.18–μm CMOS parameter and the simulation results are compared with the calculated oscillation frequency as shown in figure 3–7. In the simulation, with a proper initial node voltage set, the FRO successfully generate four-phase clock signal with α around 0.6.

The calculation predicts that α larger than 0.5 guarantee that mode 1 is dominant and the FRO will oscillate. But it does not agree with the simulation result where α should be larger than 0.6 to do so. It is because when the FRO once latches up, the bias condition of the MOS transistors are changed. More specifically, half of the MOS transistors will be turned off and the others will be in linear region.

One of the best strategy to solve this problem is to make the gain response of mode 2 zero by letting α to be one, then the FRO will not have any tendency to latch up by itself at all, although it will make the FRO slower.

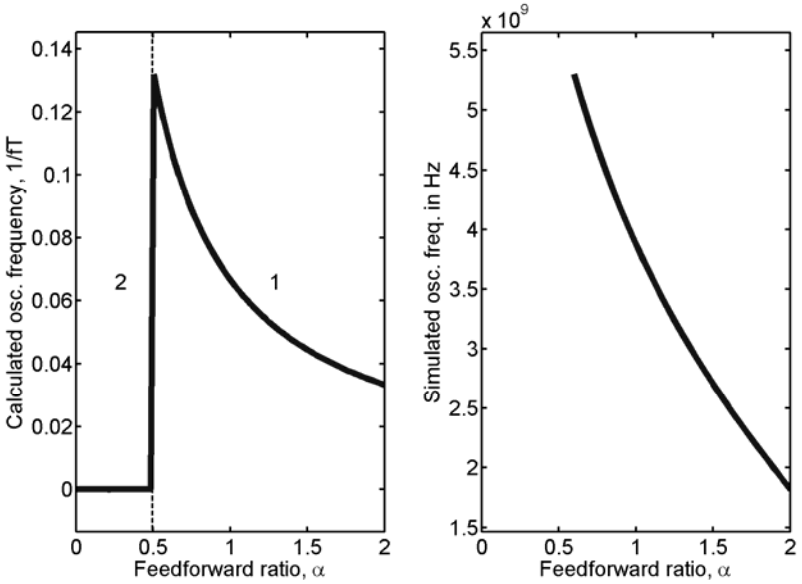

Figure 3-7. Calculated and simulated oscillation frequency of four-stage FRO.

3-2. Various-number-stage CMOS FROs

In this section, calculated and simulated oscillation frequencies of various-number-stage CMOS FROs are compared. The proposed model and analysis method were used to predict simulated CMOS FROs' behavior and specific corners of α where the oscillation mode switches. The calculation matches to the simulation results very well. Figure 3–8 through figure 3–15 compares the calculated and simulated oscillation frequencies for CMOS FROs with N=3~10 stage FRO with α over a range from 0 to 2. The phase and amplitude response calculation and the dominant decision are performed automatically by a MATLAB code.

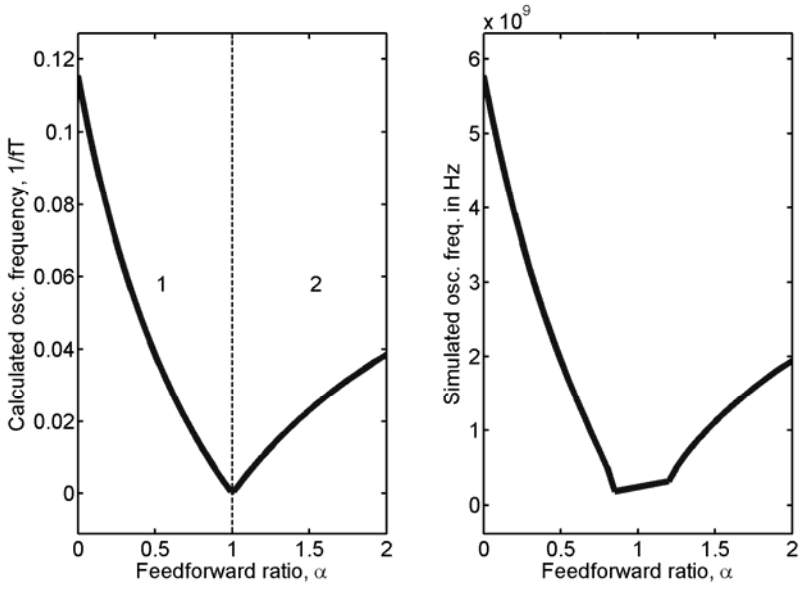

Figure 3-8. Calculated and simulated oscillation frequency of three-stage CMOS FRO.

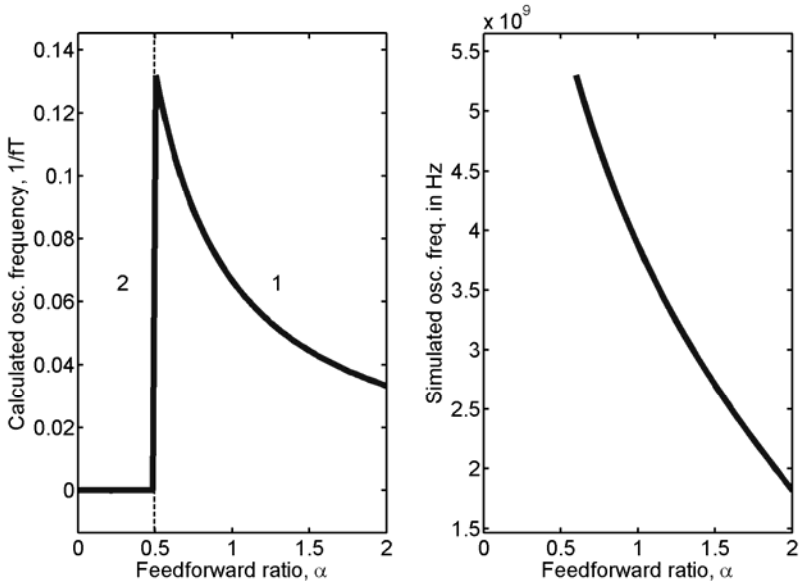

Figure 3-9. Calculated and simulated oscillation frequency of four-stage CMOS FRO.

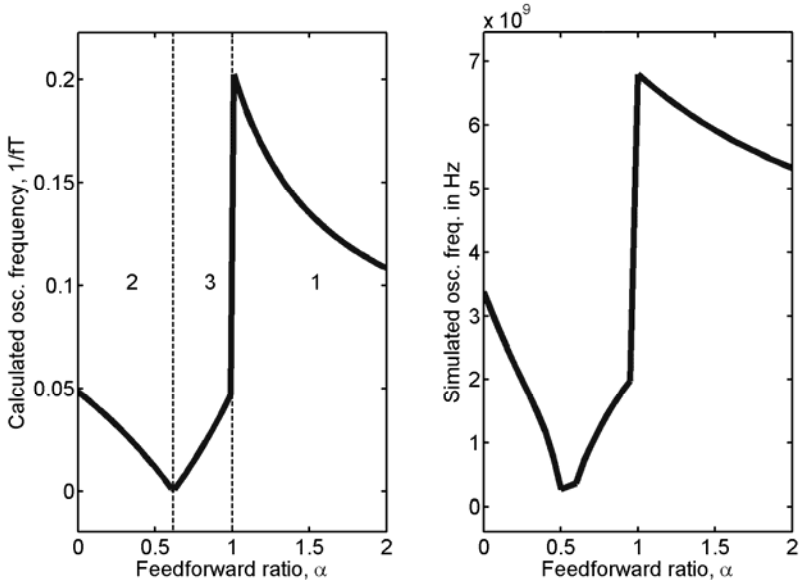

Figure 3-10. Calculated and simulated oscillation frequency of five-stage CMOS FRO.

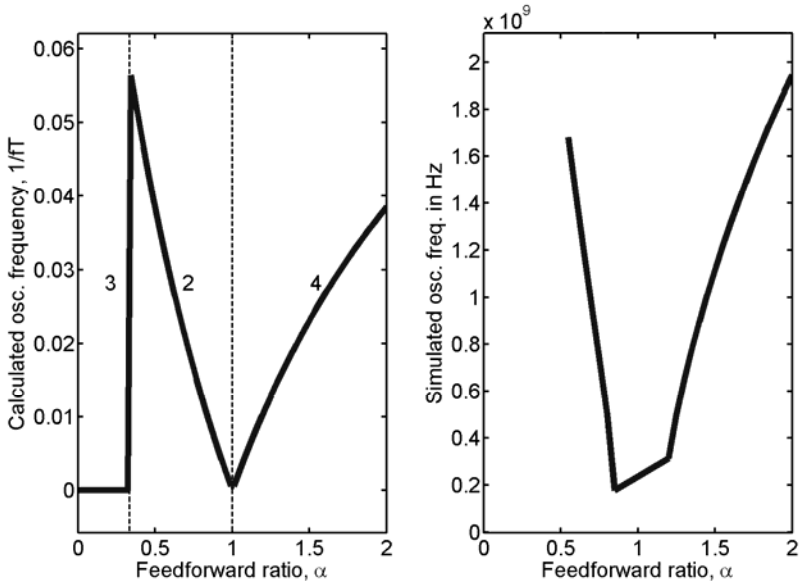

Figure 3-11. Calculated and simulated oscillation frequency of six-stage CMOS FRO.

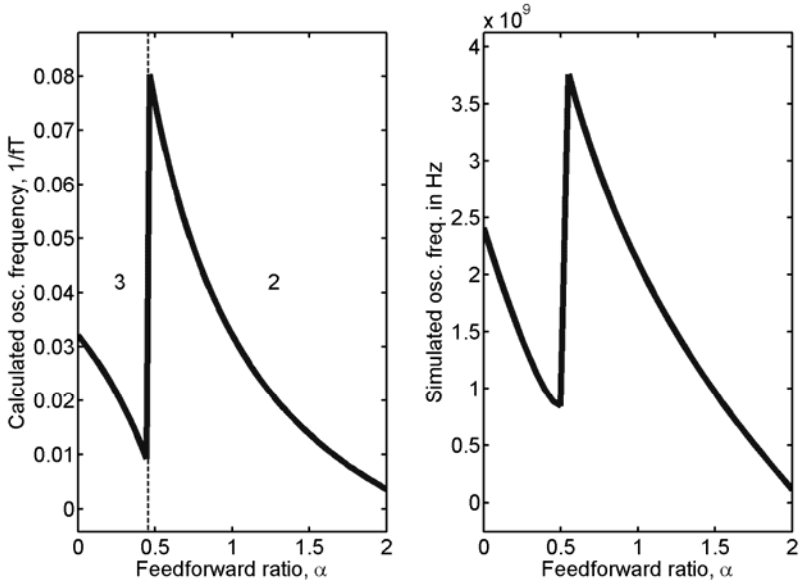

Figure 3-12. Calculated and simulated oscillation frequency of seven-stage CMOS FRO.

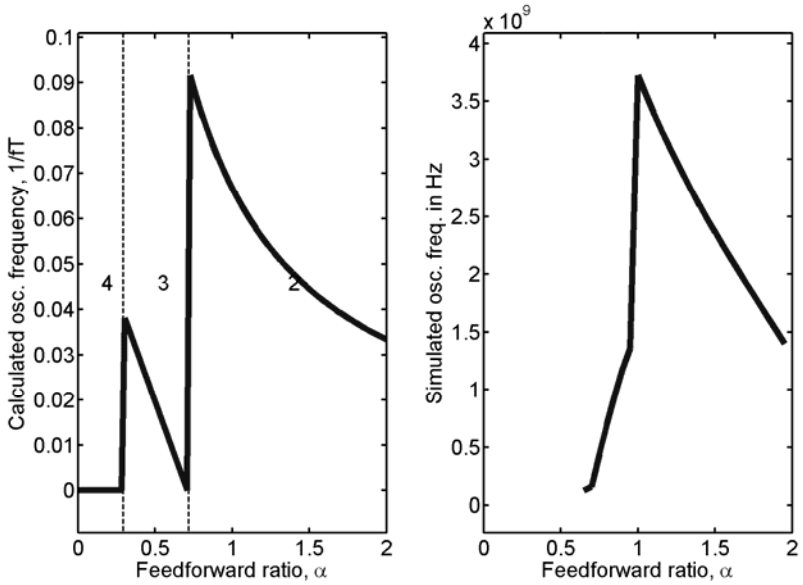

Figure 3-13. Calculated and simulated oscillation frequency of eight-stage CMOS FRO.

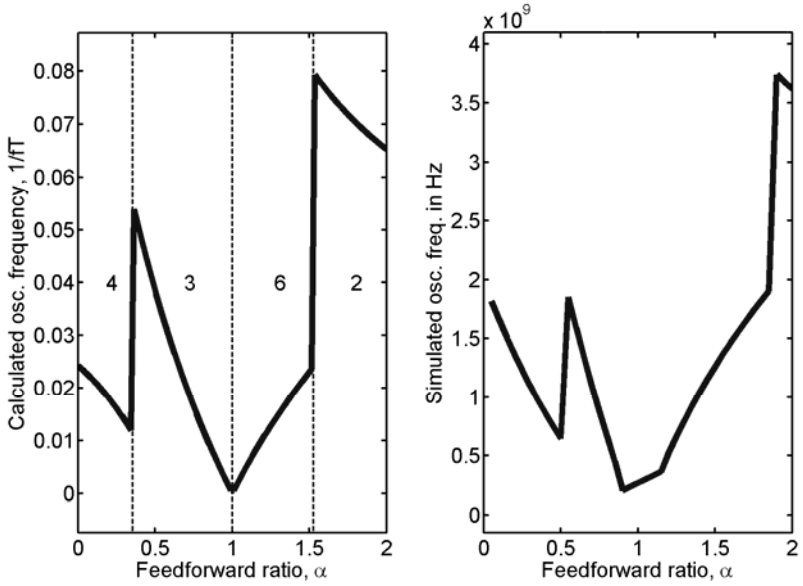

Figure 3-14. Calculated and simulated oscillation frequency of nine-stage CMOS FRO.

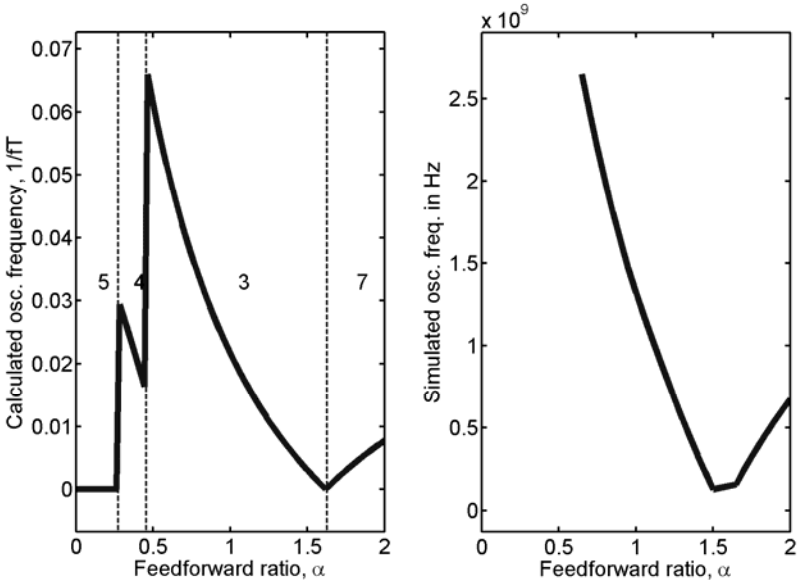

Figure 3-15. Calculated and simulated oscillation frequency of ten-stage CMOS FRO.

In figure 3–13, eight-stage FRO's dominant mode and the oscillation frequencies are shown. On the left side of figure 3–13 predicts that the dominant oscillation modes are;

--Oscillation mode 4(latch-up) with α=0~0.3.

--Oscillation mode 3(eight-phase) with α=0.3~0.7.

--Oscillation mode 2(four-phase) with α=0.7~2.

Because it consists of even number stages, the simulation results can be a little different with different initial node voltages. In our simulation results, the eight-stage FRO does not generate eight phase clocks at all, but only four phase clocks, unfortunately, whose frequency is much slower than that of the four-stage FRO.

This observation implies that the eight-stage FRO that we have shown in figure 3-13 does not have any advantage over the four-stage FRO, because it is bulkier and slower. Also, the similar argument can be applied for the six-stage FRO in figure 3–11. The six-stage FRO does not generate six phase clocks but three phase clocks. In fact, those problems can be addressed by adopting multiple feedforward paths, that will be explained in chapter five.

Finally, figure 3–16 compares the oscillation frequency plot of CMOs FROs with N=3~10. In the figure, it is clearly shown that the five-stage CMOS FRO generates the highest oscillation frequency. Figure 3–17 shows the maximum achievable oscillation frequency of CMOS FROs with N=3~10.

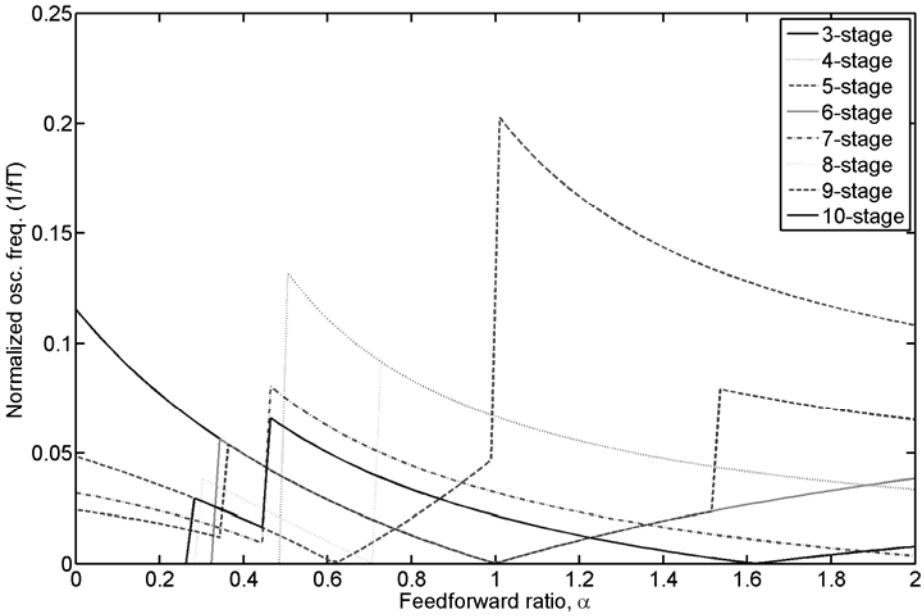

Figure 3-16. Oscillation frequency comparison of various number stage CMOS FROs.

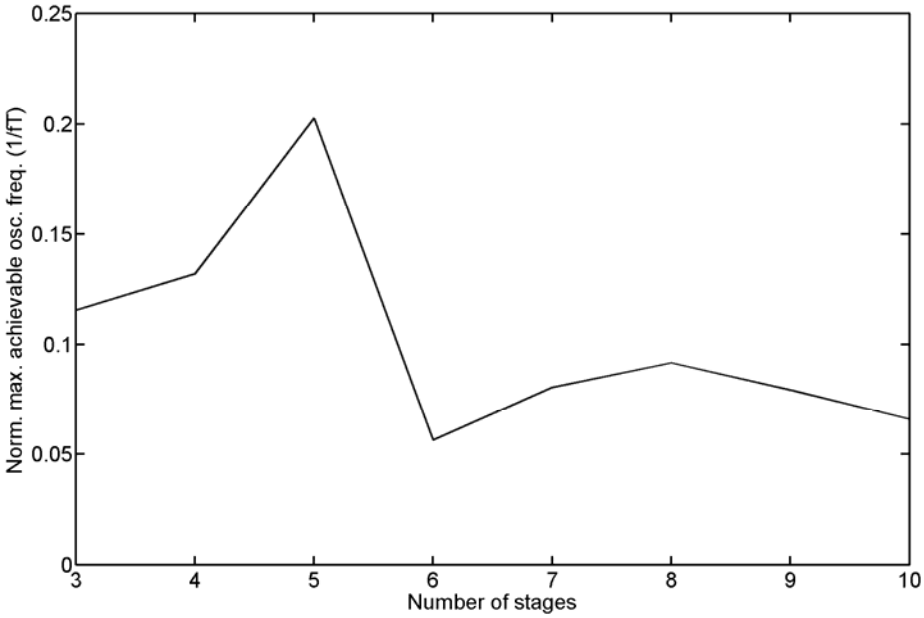

Figure 3-17. Maximum achievable oscillation frequency of CMOS FROs with N=3~10. The CMOS inverter's DC gain is 15. The oscillation frequency is normalized by f_T.

3-3. Monte-Carlo analysis

In calculation and simulation, geometric dimensions and of MOS transistor is precisely controllable and so their resultant electrical characteristics are. In real chip however, there are usually some amount of variations in the MOS transistors and other devices' characteristics and those variations can lead the fabricated chip to different results from the calculation and simulation predicted. In our case, if a FRO is designed having a feedforward ratio α which is very close to its critical boundary, the actual FRO have may fail to operate in the oscillation mode where it is supposed to operate because even a slight variation in the fabrication process can make mismatches between devices, causing actual α move across the critical boundary.

To achieve robust design, those effects must be considered carefully and included in design procedure. One possible solution is to choose α far away from the critical boundary so that deviation of α does not reach the boundary. In this case, too large margin of α will degrade the performance of the FRO, while too small margin will increase the possibility of failure. Statistical analysis such as Monte-Carlo analysis can help to find the appropriate value of α.

Figure 3-18 shows Monte-Carlo simulation results of five-stage FRO. Statistical parameters for deviation of device characteristic used in the simulation can be usually found in the fabrication vender supplied spice library. The x-axis represents feedforward ratio α and the y-axis oscillation frequency. The FRO is simulated a thousand times at each point on x-axis, and the resultant distribution of the oscillation frequencies are depicted in contour lines. The expected oscillation frequency without process variation is shown in the thick broken line.

In the figure, two distinctive groups of oscillation frequency are shown. The one in lower left part of the figure shows that the FRO is operating in oscillation mode 3, which is low frequency mode, and the other in upper right shows that it is operating in oscillation mode 1, which is high speed mode. With feedforward ratio α between 1 and 1.3, the FRO can either have oscillation mode 3 and 1 according to the amount of α deviation, therefore with the CMOS technology used in the simulation, it should be avoided to choose α in that range.

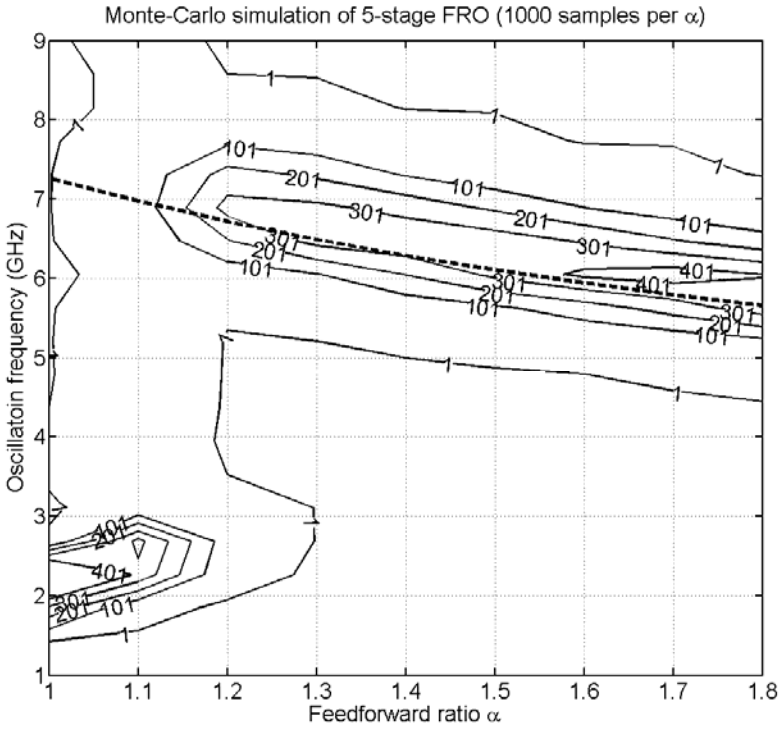

Figure 3-18. Monte-Carlo simulation results of five-stage FRO.

The histogram in figure 3-19 shows the distribution of oscillation frequencies with α=1.2 and α=1.3 in more detail. With α=1.2 in the

upper part of the figure, two peaks appear, which represent different oscillation modes.

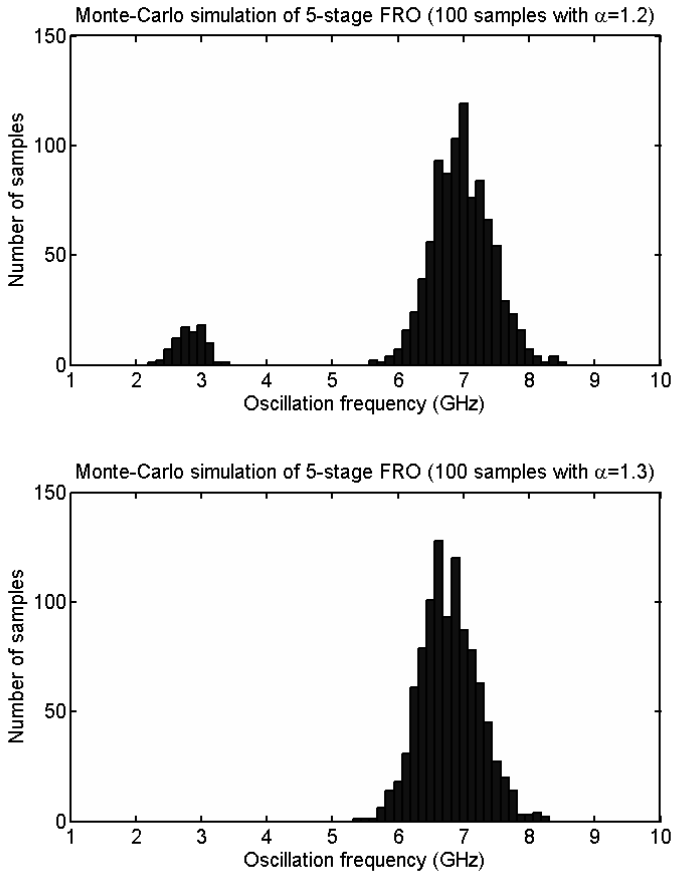

Figure 3-19. Distribution of oscillation frequencies when α is 1.2 and 1.3

In the lower part of the figure, it clearly shows that the all frequency sample is confined in one group, which is high speed oscillation mode.

Following the estimation method suggested in [17], we can easily estimate the probability of failure with a certain confidence level using (3-1)

$$np = -\ln(1-CL) + \ln\left[\sum_{k=0}^{N}\frac{(np)^k}{k!}\right] \quad (3\text{-}1)$$

, where n is required number of total samples, CL is confidence level, N is number of failure sample and p is expected failure probability. Equation (3-1) gives the minimum number of total samples required to guarantee that the actual probability of failure is less than p with confidence level of CL. Since we have no failure sample with α=1.3, N becomes zero and the right side of the equation (3-1) is 4.61. Since we have one thousand samples, the actual probability of failure is lower than 0.461% with 99% of confidence.

According to the figure 3-18, the oscillation frequency degradation from having α=1.3 rather than a feedforward ratio α close to 1 is about -8%, which is a quite good trade-off for 0.461% of failure chance.

Chapter 4. FRO speed optimization

In the previous chapter, we have shown that the proposed FRO model successfully predicts simulated FROs behavior. We have assumed that CMOS inverter is utilized for the delay element. It is also shown that CMOS FRO's oscillation frequency can be maximized by choosing number of stages N=5 and the feedforward ratio α=1. The CMOS inverter's DC gain is around 15, and as we noted earlier, and it is limited by the channel length of the MOS transistors and cannot be controlled. In the other hand, if a resistor-loaded inverting amplifier is used for FROs, the load resistance R also can be optimized as well as the feedforward ratio to achieve even higher oscillation frequency.

In this chapter, an example of speed maximization procedure of five-stage FRO is shown.

4-1. Speed maximization procedure of resistor loaded five–stage FRO

The design goal is to find optimum load resistance R and feedforward ratio α for the maximum oscillation frequency of five-stage FRO. Also we will make the FRO oscillate in mode 1.

Schematic diagram of a resistor-loaded inverting amplifier is shown in figure 4–1. The amplifier shown in the figure is utilized for the unit stage of FRO. The NMOS transistor's channel length and width are 0.18μm and 1μm, respectably.

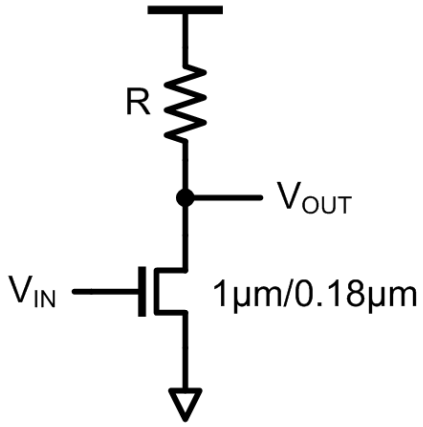

Figure 4-1. Schematic diagram of a simple inverting amplifier

Assuming that the NMOS transistor's output resistance r_{ds} is infinitely large, the maximum achievable oscillation frequency can be easily determined by following the procedure described below.

--With a given feedforward ratio α, the smaller R gives the higher oscillation frequency. The lower bound of R can be determined by letting the amplitude response of the unit stage be unity.

$$\left|H(\alpha)\right| = \frac{-g_m R}{1+\alpha}\left[\cos\theta + \alpha\cos(2\theta)\right] = 1$$

$$R > \frac{1+\alpha}{-g_m\left[\cos\theta + \alpha\cos(2\theta)\right]} = R_{MIN} \qquad (4\text{–}1)$$

--The oscillation frequency with R_{MIN} is calculated as

$$f_0 = \frac{-1}{2\pi RC}\left(\frac{\sin\theta + \alpha\sin 2\theta}{\cos\theta + \alpha\cos 2\theta}\right)$$

$$f_{MAX} = \frac{-1}{2\pi R_{MIN} C}\left(\frac{\sin\theta + \alpha\sin 2\theta}{\cos\theta + \alpha\cos 2\theta}\right) = \frac{g_m\left(\sin\theta + \alpha\sin 2\theta\right)}{2\pi C\left(1+\alpha\right)} \qquad (4\text{–}2)$$

$$= \frac{\left(\sin\theta + \alpha\sin 2\theta\right)}{\left(1+\alpha\right)} f_T$$

--With a given load resistance R, the maximum oscillation frequency is achieved by letting α=1 and θ=2π/5, as we have discussed in the previous chapter.

$$f_{MAX} = \frac{(\sin\theta + \sin 2\theta)}{2} f_T$$
$$= \frac{\left[\sin(2\pi/5) + \sin(4\pi/5)\right]}{2} f_T \sim 0.769\, f_T \quad (4\text{–}3)$$

Figure 4–2 compares the maximum achievable oscillation frequencies of conventional SPRO and the optimized five-stage FRO. It is shown that the five-stage FRO is fastest, except for the three-stage SPRO. Note that the five-stage SPRO is actually the same to the five-stage FRO with α=0. It implies that the five-stage FRO is always faster when it is operating in oscillation mode 1 than in other modes.

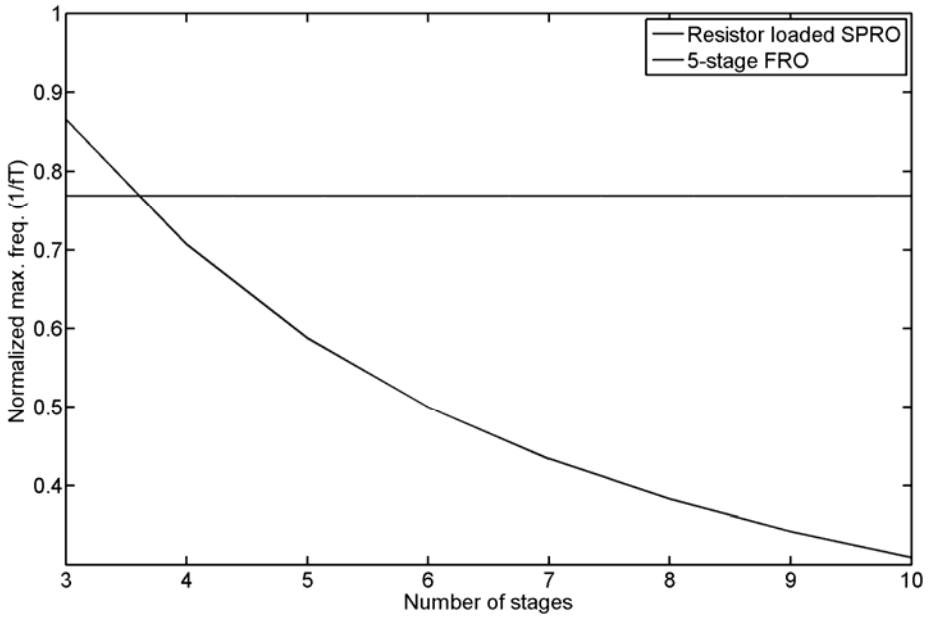

Figure 4-2. Comparison between maximum achievable oscillation frequencies of SPRO and the optimized five-stage FRO.

4-2. Speed maximization procedure of resistor loaded five–stage FRO with a finite r_{ds}

Recall that we have assumed that the NMOS transistor's output resistance r_{ds} is infinitely large, which is not true for the real MOS transistor, especially for the sub-micrometer CMOS processes where the channel length modulation effect is very severe. The finite r_{ds} lowers the amplitude response of the unit stage resulting a different optimum value of R and α. In other words, an α larger than one may give the maximum oscillation frequency.

In this case, we take a different approach to derive oscillation frequency as described below

--With a given load resistance R, the smaller α will result the higher oscillation frequency as long as the FRO is operating in mode 1. The minimum α can be calculated as a function of R:

$$\alpha_{MIN}(R) = -\frac{1 + A_{DC}(R)\cos\theta}{1 + A_{DC}(R)\cos 2\theta} \qquad (4\text{-}4)$$

, where $A_{DC}(R)$ is the DC gain of the unit stage. It is also a function of R, that is, $g_m(R||r_{ds})$.

Using HSPICE, the inverting amplifier's DC gain is simulated, while the load resistance R is being swept from 0Ω to 10kΩ. The simulated DC gain is shown in figure 4-3. The simulated DC gain is not a linearly increasing function of R because of the r_{ds} effect. As a result, the output resistance of the amplifier droops and so does the amplifier's DC gain.

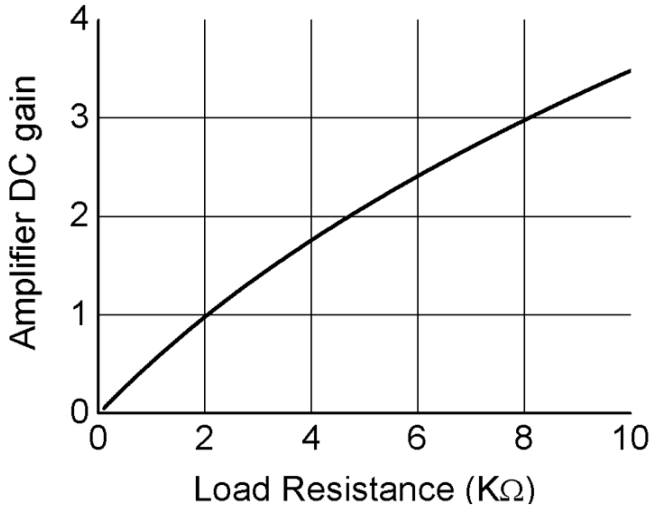

Figure 4-3. Simulated DC gain of the inverting amplifier.

With the DC gain curve, minimum feedforward ratio α_{MIN} for unit gain at the oscillation frequency can be calculated using (4–4). In other words, α_{MIN} represents for the minimum feedforward ratio required so that the FRO will operate in oscillation mode 1 at a given load resistance, R. Calculated α_{MIN} is shown in figure 4–4.

Finally, the oscillation frequency can be calculated. The calculated maximum frequency is plotted in figure 4–5. When R is around 5KΩ, the oscillation frequency reaches its maximum value of about 18GHz. At the same time, α_{MIN} is found at around 2.5. Interestingly, α_{MIN} is much larger than the optimal value of 1 derived in the previous chapter.

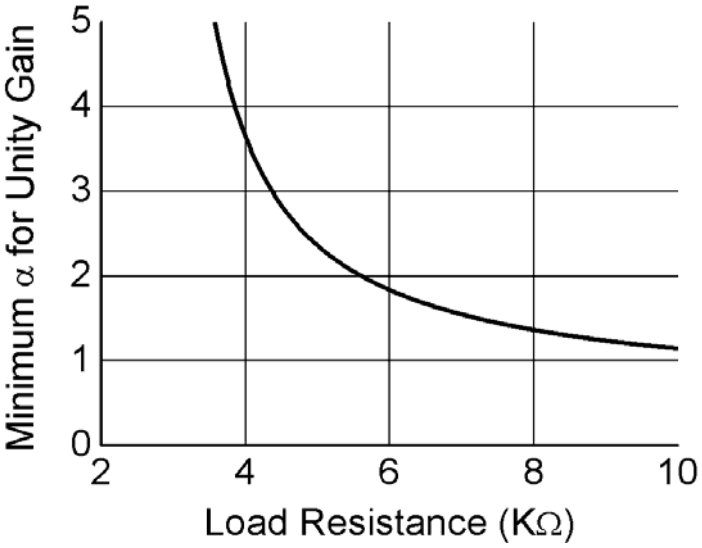

Figure 4-4. Calculated α_{MIN} required for mode 1 operation

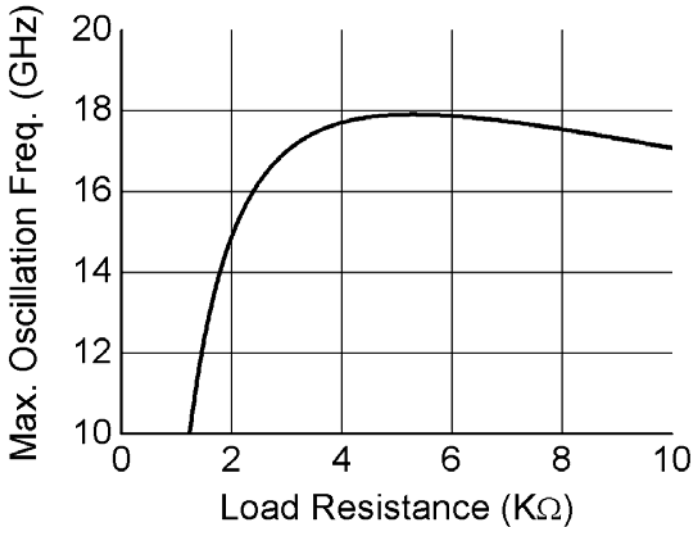

Figure 4-5. Calculated oscillation frequency

4-3. FRO implementation and measurement result

A five-stage FRO is optimized for the maximum oscillation frequency in the previous section, and the FRO is implemented with a typical 0.18–μm CMOS process. Figure 4–6 shows the schematic diagram of the implemented unit stage. As shown in the figure, two inverting amplifiers share single load resistance R/(1+α) which is a parallel combination of R and R/α. For frequency tuning, NMOS bias transistor M1 is added to the direct path.

For measurement, a single–ended open drain buffers were used, that can be terminated to the power supply voltage (1.8V) via a bias–T. Also, to emulate process variation, oscillators with load resistances varying by ±5% were included in the same die.

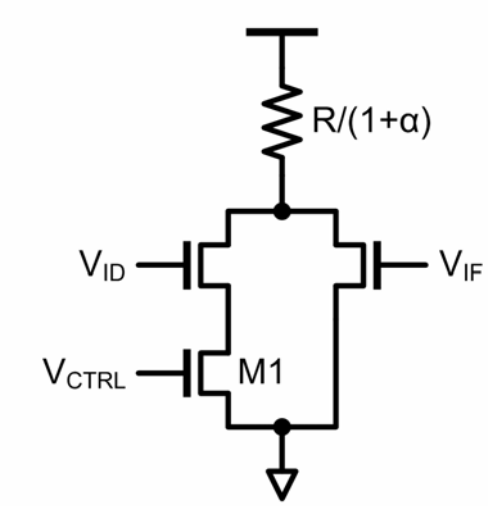

Figure 4-6. Schematic diagram of the implemented unit stage of the five-sage FRO.

Figure 4-7 shows the microphotograph of the implemented FRO. An electrical static discharge (ESD) protection circuit is also included. A probe station is used to access the input/output pads directly. Although it is a five-stage FRO, only one clock phase is routed to the output. It is because the main purpose of this design is to show and verify the maximum oscillation frequency achievable with the given CMOS technology, and also it will be too bulky if it has five signal pads to access every clock phases. The active area for the chip is less than $0.001mm^2$, which is much smaller than a typical LC oscillator.

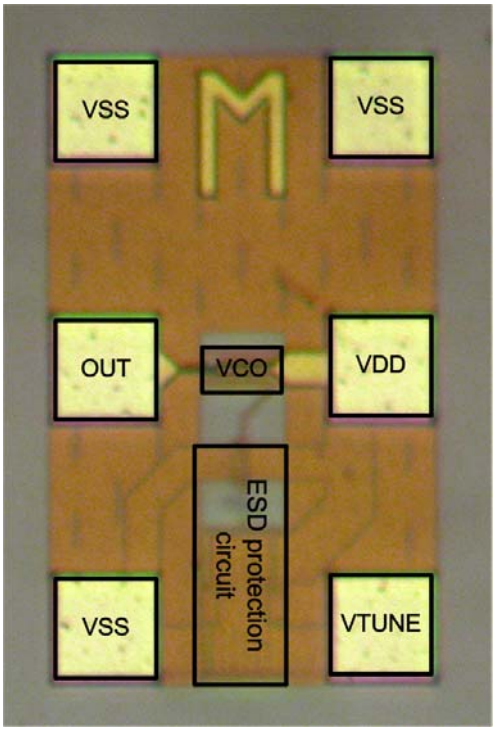

Figure 4-7. Microphotograph of the implemented five-stage FRO.

Figure 4-8 shows the measured VCO tuning curves. The maximum oscillation frequencies are around 16GHz, which are slightly lowered than the calculation results and it is due to the layout parasitic effect. Figure 4-9 shows the output spectrum of the FRO at 16Ghz.

Measured phase noise is shown in figure 4-10. Phase noises at 1MHz offset frequency is –78~–93dBc/Hz over the whole oscillation frequency range, which are comparable to other previously reported oscillators. Measured oscillator performance is summarized and compared in table 4–1 with other related works from recent publications.

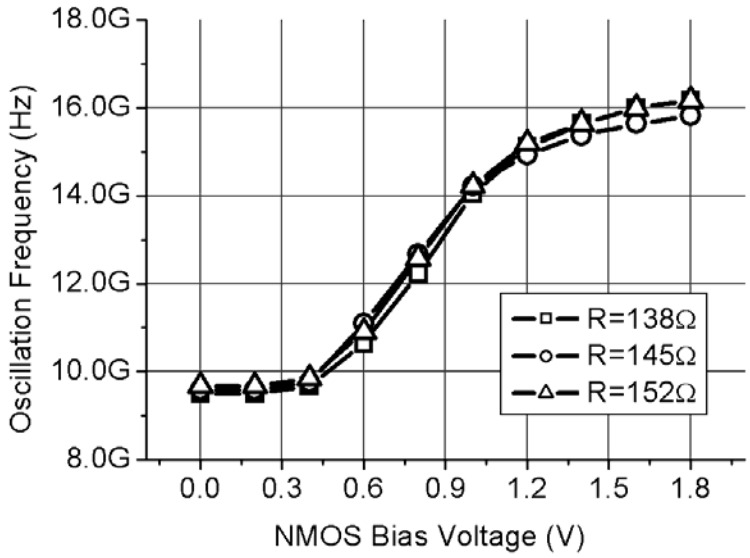

Figure 4-8. Measured oscillation frequency of the five-stage FRO.

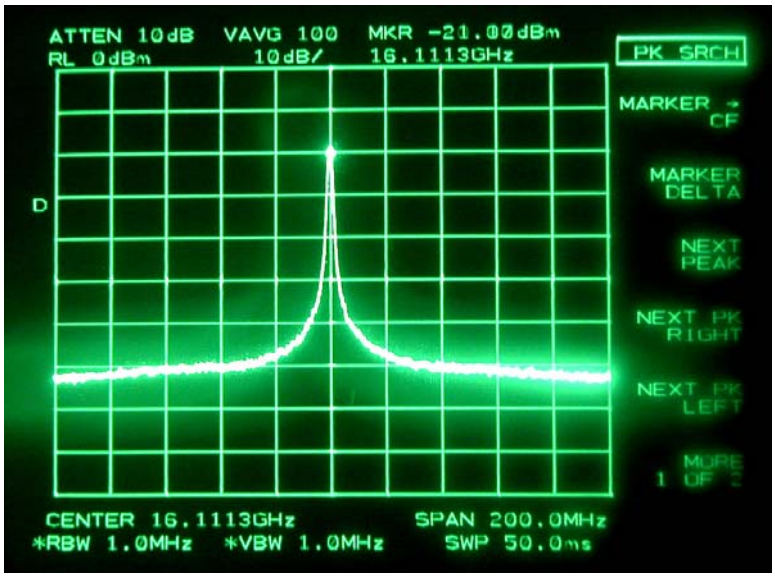

Figure 4-9. Output spectrum of the FRO at 16Ghz.

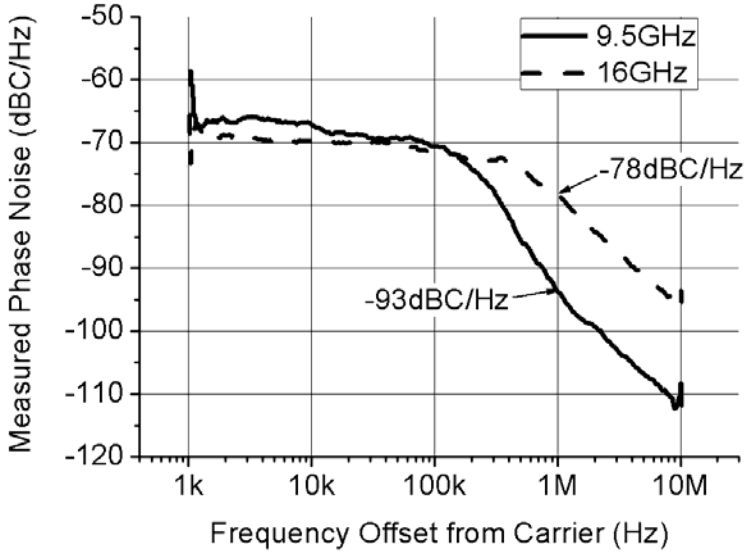

Figure 4-10. Measured output phase noise of the FRO.

Table 4–1. Measured oscillator performance and comparison with other related works from recent publications.

Frequency (Ghz)	Tech.	Power supply (V)	Power diss. (mW)	Phase noise (–dBc/Hz)	Offset (Mhz)	Area (mm^2)	Oscillator structure	Ref.
0.1~3.5	0.18µm	1.8	16	111~106	4	N/A	Four stage FRO	[9]
4.6	0.18µm	1.8	23	N/A	N/A	N/A	Five stage FRO	[11]
5.16~5.93	0.18µm	1.8	N/A	99.5	1	N/A	Three stage FRO	[10]
8.4~10.1	0.18µm	1.8	50	99.9	1	N/A	Three stage FRO	[12] *
8.4~10.6	0.12µm	1.5	52.5	85	1	N/A	Three stage SC3A	[18]
10.2~12.48	0.18µm RF	2.2	50	125.33	1	0.665	LC tank	[19]
9.5~16	0.18µm	1.8	48~54	78~93	1	0.001	Five stage FRO	This work

* Simulation result only

4-4. Simulation results of five-stage FRO with 65nm CMOS

Using 65nm CMOS technology, five-stage FRO is optimized for the maximum oscillation frequency following the same procedure shown in the previous section. Figure 4-11 shows the simulation results including layout parasitic components. Upper in the figure is signal waveform of clock signal. Lower in the figure is the oscillation frequency. It is shown that the FRO can oscillate up to 27GHz, while the output signal swing is about 300mVp2p.

The oscillation frequency is increased by 68%, which is a little lower than expected. It seems that as the process technology scales down, the effects of parasitic components on the circuit operation speed becomes more serious.

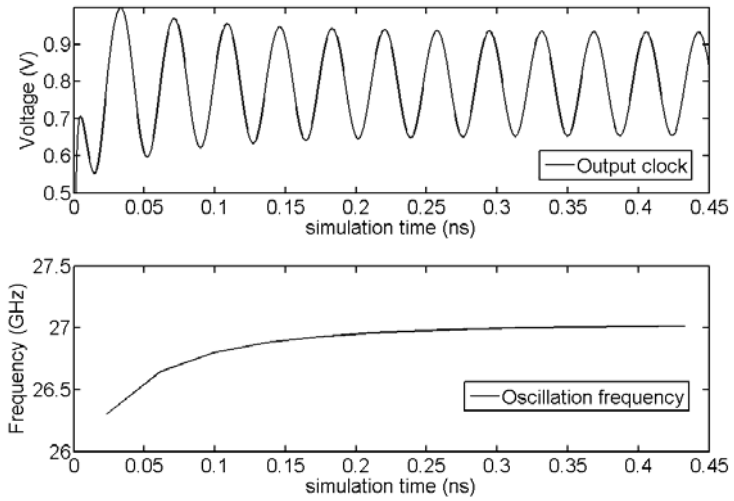

Figure 4-11. Simulation results of five-stage FRO in 65nm CMOS technology

Chapter 5. Generalized FRO model

In the previous chapter, we have discussed FROs with only one feedforward path, In other words, the FRO's unit stage consists of two delay elements. In this chapter, the proposed model and analysis method are extended to FROs with more than two feedforward paths. For convenience, we will call them multi feedforward ring oscillator (MFRO).

5-1. MFRO analysis

With an N-stage FRO, the generalized unit stage structure can be depicted as shown in figure 5-1. A slightly different signaling convention from the previous chapter is used. Since an N-stage FRO has N nodes, the unit stage can have maximally up to N-1 paths, including the direct path. The direct path is depicted as i^{th} path in the figure. The path ratios are noted as α_1, α_2, … and α_{N-1} in a sequential order. If there is no path from a specific node, the α corresponding the path is set to zero. In this manner, a set of αs or a vector [α_1, α_2, … α_{N-1}] can define the MFRO completely. For instance, the four-stage FRO and five-stage FRO which we have discussed can be represented by a vector [1, α, 0] and [1, α, 0, 0], respectably. The first element α_1 which corresponds to the direct path is set to one.

The small signal equivalent circuit of the unit stage is shown in figure 5-2. The output resistance is a parallel combination of the output resistances of each inverters; $R/\Sigma(\alpha_k)$. The load capacitance is also a parallel combination of the load capacitances from each inverters; $C\Sigma(\alpha_k)$, where k is an index from 1 to N-1. The resultant time constant

at the output node of the unit stage is the same to that of a single inverter, RC.

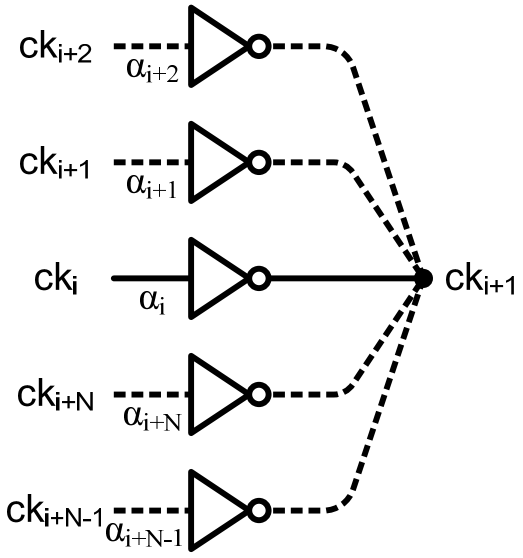

Figure 5-1. Generalized unit stage structure of MFRO.

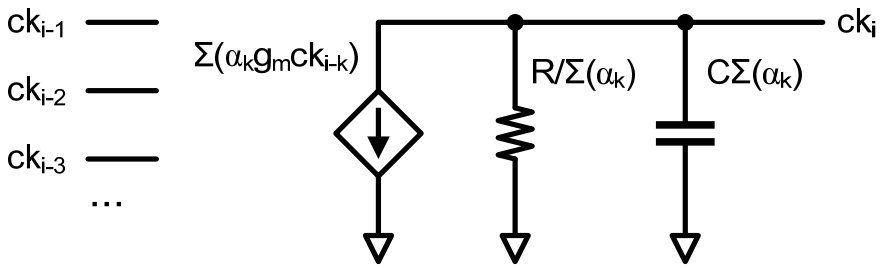

Figure 5-2. A small signal equivalent circuit of the unit stage.

Total current drawn from two trans-conductors is:

$$I = -\sum_{k=1}^{N-1} \alpha_k g_m ck_{i-k} \tag{5–1}$$

ck_i can be calculated by multiplying the output impedance to (5–1):

$$CK_i = \frac{-R\left[\sum_{k=1}^{N-1} \alpha_k g_m \angle(1-k)\theta\right] CK_{i-1}}{\left(\sum_{k=1}^{N-1} \alpha_k\right)(1+j\omega RC)}$$

$$= \left(-R \Big/ \sum_{k=1}^{N-1} \alpha_k\right) \frac{g_m \left\{\sum_{k=1}^{N-1}\left[\alpha_k \cos(1-k)\theta\right] + j\sum_{k=1}^{N-1}\left[\alpha_k \sin(1-k)\theta\right]\right\}}{(1+j\omega RC)} CK_{i-1}$$

$$= \frac{-g_m R_{EQ}(X+jY)}{(1+j\omega RC)} CK_{i-1} \tag{5–2}$$

, where $X=\Sigma[\alpha_k \cos(1-k)\theta]$, $Y=\Sigma[\alpha_k \sin(1-k)\theta]$ and $R_{EQ}=R/\Sigma(\alpha_k)$. The unit stage's transfer function $H(\alpha)$ can be derived as (5–3). Interestingly, it is the exactly same to that from the previous chapter.

$$H(\alpha) = \frac{-g_m R_{EQ}(X+jY)}{(1+j\omega_0 RC)} \tag{5–3}$$

The amplitude response of $H(\alpha)$ can be easily found by following the similar procedure:

$$\left|H(\alpha)\right| = -g_m R_{EQ}(X\cos\theta + Y\sin\theta) \tag{5–4}$$

Restoring X and Y in (5-4) with $X=\Sigma[\alpha_k\cos(1-k)\theta]$, $Y=\Sigma[\alpha_k\sin(1-k)\theta]$, we have:

$$\begin{aligned}
\left|H(\alpha)\right| &= -g_m R_{EQ}\left\{\sum_{k=1}^{N-1}\left[\alpha_k\cos(1-k)\theta\cos\theta\right]+\sum_{k=1}^{N-1}\left[\alpha_k\sin(1-k)\theta\sin\theta\right]\right\} \\
&= -g_m R_{EQ}\sum_{k=1}^{N-1}\left\{\alpha_k\left[\cos(1-k)\theta\cos\theta+\sin(1-k)\theta\sin\theta\right]\right\} \\
&= -g_m R_{EQ}\sum_{k=1}^{N-1}\left(\alpha_k\cos k\theta\right) \\
&= \left(-g_m R\Big/\sum_{k=1}^{N-1}\alpha_k\right)\left[\sum_{k=1}^{N-1}\left(\alpha_k\cos k\theta\right)\right]
\end{aligned} \tag{5–5}$$

The frequency independent phase shift β can be found as:

$$\beta=\begin{cases}\tan^{-1}(Y/X), \text{ if } X>0\\ \tan^{-1}(Y/X)+\pi, \text{ if } X<0\end{cases}$$

$$\text{, where } \frac{Y}{X}=\left\{\frac{\sum_{k=1}^{N-1}\left[\alpha_k\sin(1-k)\theta\right]}{\sum_{k=1}^{N-1}\left[\alpha_k\cos(1-k)\theta\right]}\right\} \tag{5–6}$$

The oscillation frequency is:

$$f_0=\left(\frac{-1}{2\pi RC}\right)\left[\frac{\sum_{k=1}^{N-1}\left(\alpha_k\sin k\theta\right)}{\sum_{k=1}^{N-1}\left(\alpha_k\cos k\theta\right)}\right] \tag{5–7}$$

Newly derived (5–2), (5–5), (5–6) and (5–7) are actually the same to, but extended version of the equations for FRO's counterparts, that were derived in the previous chapter. Table 5-1 compares two groups of equations.

Table 5–1. Comparison of equations for FRO and MFRO.

	FRO	MFRO
H(α)	$H(\alpha)=\frac{-g_m R_{EQ}(X+jY)}{(1+j\omega_0 RC)}$	$H(\alpha)=\frac{-g_m R_{EQ}(X+jY)}{(1+j\omega_0 RC)}$
X	$1+\alpha\cos\theta$	$\sum_{k=1}^{N-1}\left[\alpha_k\cos(1-k)\theta\right]$
Y	$-\alpha\sin\theta$	$\sum_{k=1}^{N-1}\left[\alpha_k\sin(1-k)\theta\right]$
|H(α)|	$-\frac{g_m R}{1+\alpha}(\cos\theta+\alpha\cos 2\theta)$	$\left(-g_m R\Big/\sum_{k=1}^{N-1}\alpha_k\right)\left[\sum_{k=1}^{N-1}(\alpha_k\cos k\theta)\right]$
γ	$\theta-\beta-\pi$	$\theta-\beta-\pi$
β	$\beta=\begin{cases}\tan^{-1}(Y/X), \text{ if } X>0\\ \tan^{-1}(Y/X)+\pi, \text{ if } X<0\end{cases}$	$\beta=\begin{cases}\tan^{-1}(Y/X), \text{ if } X>0\\ \tan^{-1}(Y/X)+\pi, \text{ if } X<0\end{cases}$
f_0	$\left(\frac{-1}{2\pi RC}\right)\left(\frac{\sin\theta+\alpha\sin 2\theta}{\cos\theta+\alpha\cos 2\theta}\right)$	$\left(\frac{-1}{2\pi RC}\right)\left[\frac{\sum_{k=1}^{N-1}(\alpha_k\sin k\theta)}{\sum_{k=1}^{N-1}(\alpha_k\cos k\theta)}\right]$

5-2. Simulation of MFROs

Various MFOs' dominant oscillation mode and the oscillation frequencies are determined and calculated. Figure 5-3 though 5-7 show the calculation result for [1, α_2, α_3], [1, α_2, α_3, 0], …, [1, α_2, α_3, 0, 0, 0, 0]. In other words, N=3~8 stage MFROs with only the first and the second feedforward paths.

On the left side of the figures are shown the dominant oscillation modes mapped two dimensional α space, [α_2, α_3]. α_2, α_3 are swept from zero to two. On the right side of the figures are shown the calculated oscillation frequency, normalized by f_T. The DC gain of CMOS inverter is assumed to be 15.

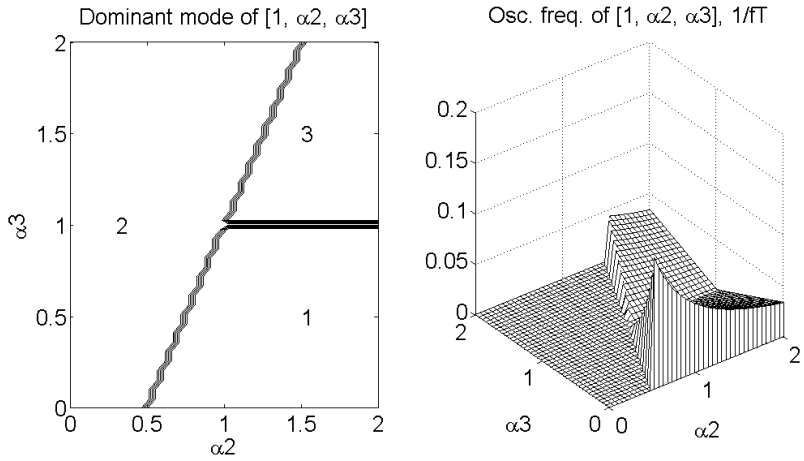

Figure 5-3. An example of four-stage MFRO.
Left: Determined dominant mode of four-stage MFRO, [1, α_2, α_3]
Right: Calculated oscillation frequency (1/fT)

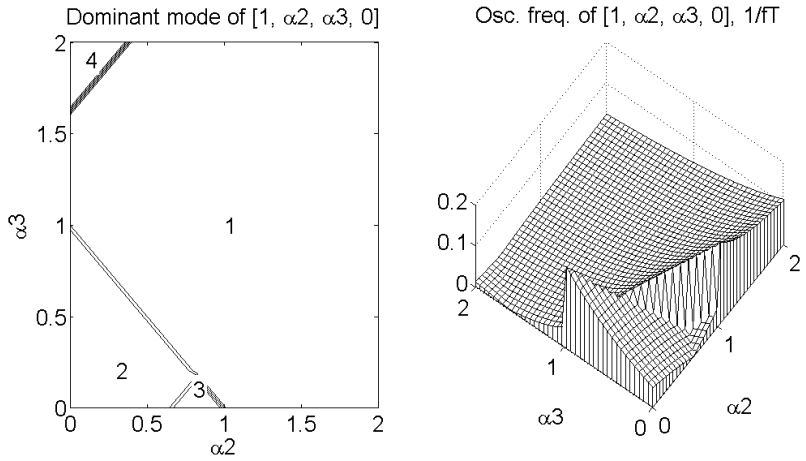

Figure 5-4. An example of five-stage MFRO.

Left: Determined dominant mode of five-stage MFRO, [1, α_2, α_3, 0]

Right: Calculated oscillation frequency (1/fT)

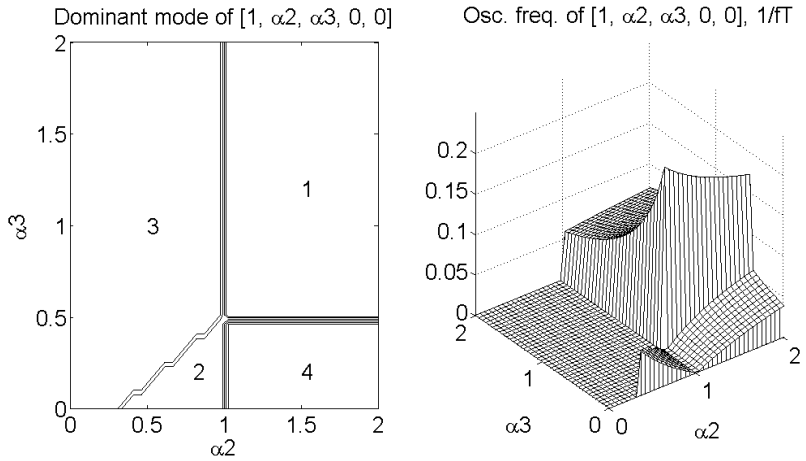

Figure 5-5. An example of six-stage MFRO.

Left: Determined dominant mode of five-stage MFRO, [1, α_2, α_3, 0, 0]

Right: Calculated oscillation frequency (1/fT)

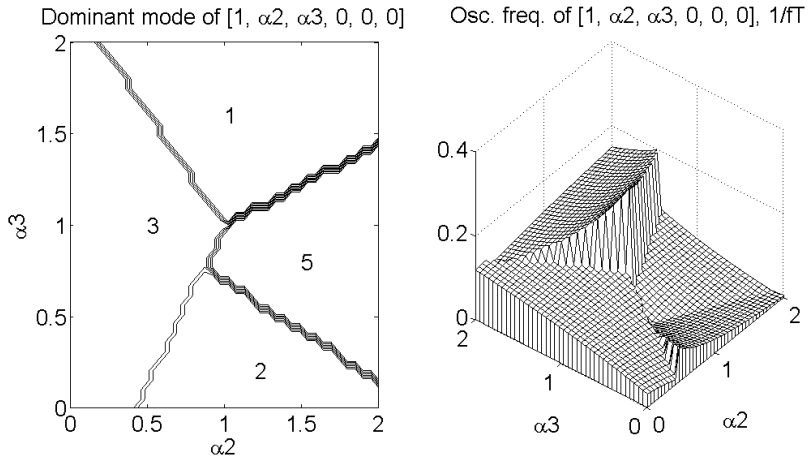

Figure 5-6. An example of seven-stage MFRO.

Left: Determined dominant mode of five-stage MFRO, [1, α_2, α_3, 0, 0, 0]

Right: Calculated oscillation frequency (1/fT)

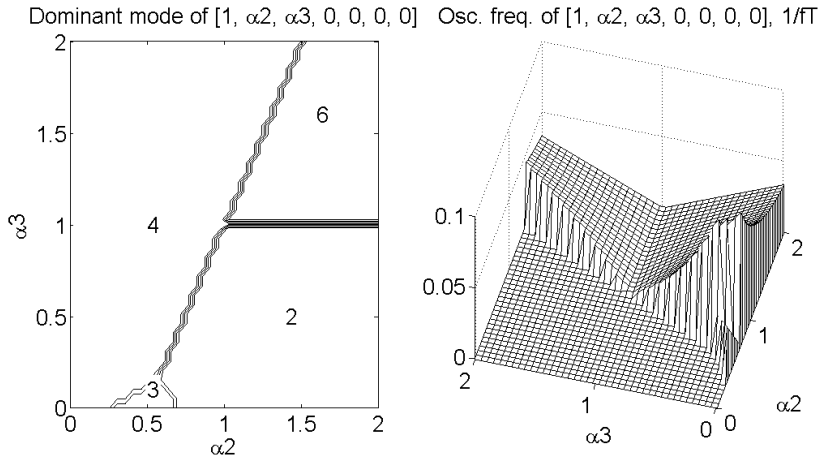

Figure 5-7. An example of eight-stage MFRO.

Left: Determined dominant mode of five-stage MFRO, [1, α_2, α_3, 0, 0, 0, 0]

Right: Calculated oscillation frequency (1/fT)

The MFRO examples shown above through figure 5–3 ~ figure 5–7 are simulated for the same α space, [α_2, α_3] using HSPICE with a standard 0.18–μm CMOS parameter. The simulated oscillation frequencies are measured 400 at points over α space [0~2, 0~2] for each MFRO. The simulation results are shown in figure 5–8 ~ figure 5–12. Throughout the comparison, it is shown that the calculation using the proposed MFRO model can predict the simulated MFRO's oscillation behavior and the oscillation frequency very well. Also, the comparison between the calculation results and the simulated oscillation frequencies show that specific corner values of α can be predicted relatively accurately.

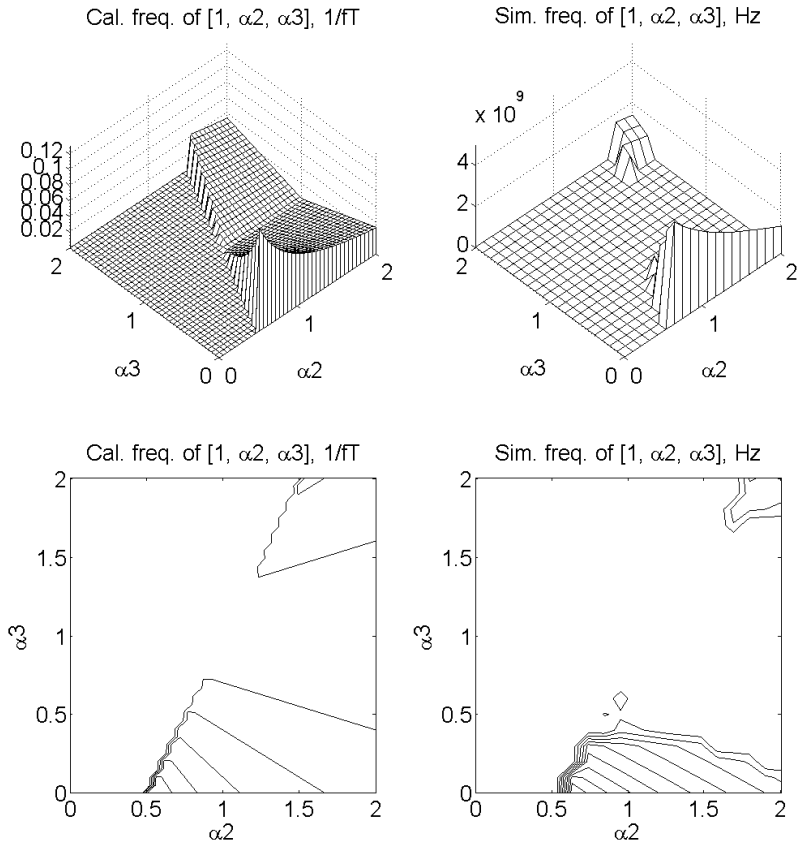

Figure 5-8.

Upper left: Calculated oscillation frequency of [1, α2, α3], depicted in three-dimensional space. The oscillation frequencies are normalized by f_T.

Upper right: Calculated oscillation frequency of [1, α2, α3]

Lower left: Calculated oscillation frequency of [1, α2, α3], depicted in two-dimensional space.

Lower right: Simulated oscillation frequency of [1, α2, α3], depicted in two-dimensional space.

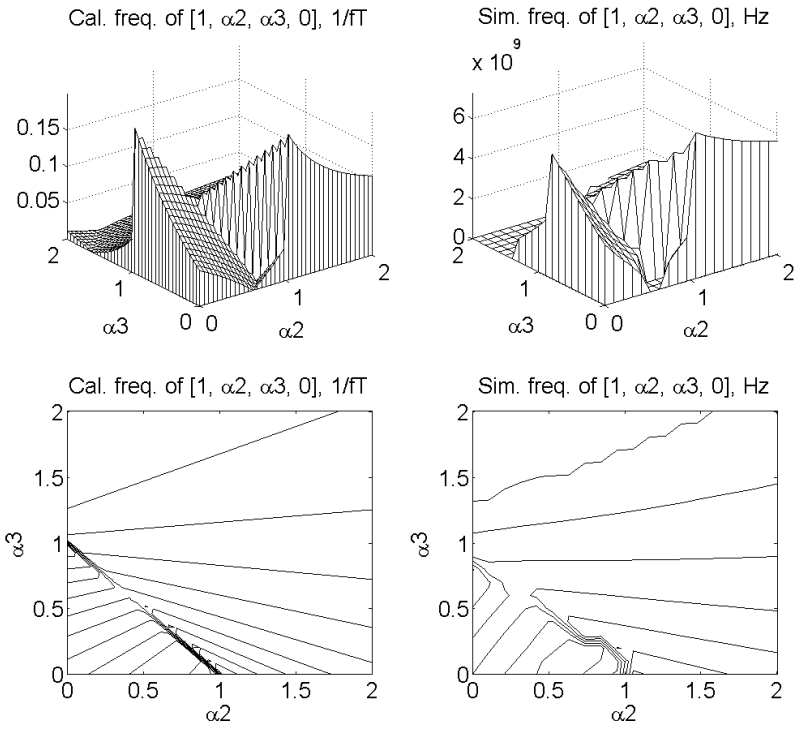

Figure 5-9.

Upper left: Calculated oscillation frequency of [1, α2, α3, 0], depicted in three-dimensional space. The oscillation frequencies are normalized by f_T.

Upper right: Calculated oscillation frequency of [1, α2, α3, 0]

Lower left: Calculated oscillation frequency of [1, α2, α3, 0], depicted in two-dimensional space.

Lower right: Simulated oscillation frequency of [1, α2, α3, 0], depicted in two-dimensional space.

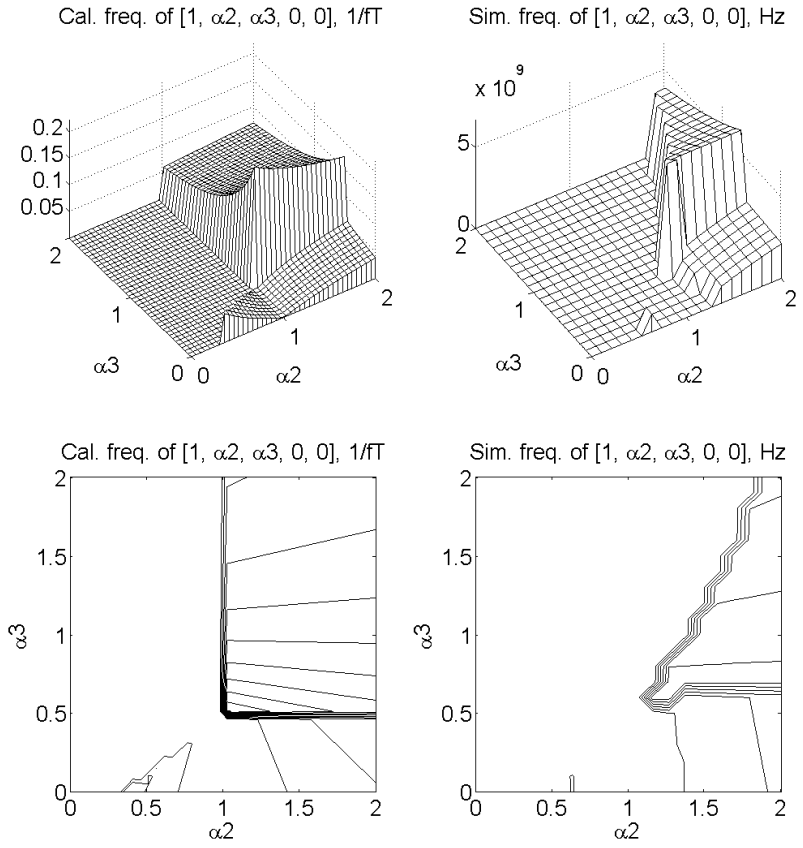

Figure 5-10.

Upper left: Calculated oscillation frequency of [1, α2, α3, 0, 0], depicted in three-dimensional space. The oscillation frequencies are normalized by f_T.

Upper right: Calculated oscillation frequency of [1, α2, α3, 0, 0]

Lower left: Calculated oscillation frequency of [1, α2, α3, 0, 0], depicted in two-dimensional space.

Lower right: Simulated oscillation frequency of [1, α2, α3, 0, 0], depicted in two-dimensional space.

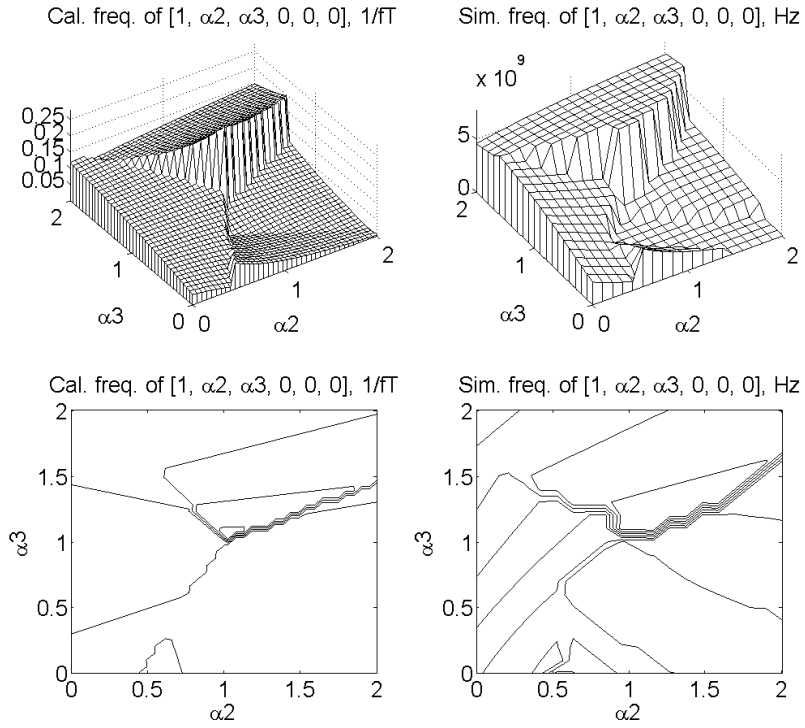

Figure 5-11.

Upper left: Calculated oscillation frequency of [1, α2, α3, 0, 0, 0], depicted in three-dimensional space. The oscillation frequencies are normalized by f_T.

Upper right: Calculated oscillation frequency of [1, α2, α3, 0, 0, 0]

Lower left: Calculated oscillation frequency of [1, α2, α3, 0, 0, 0], depicted in two-dimensional space.

Lower right: Simulated oscillation frequency of [1, α2, α3, 0, 0, 0], depicted in two-dimensional space.

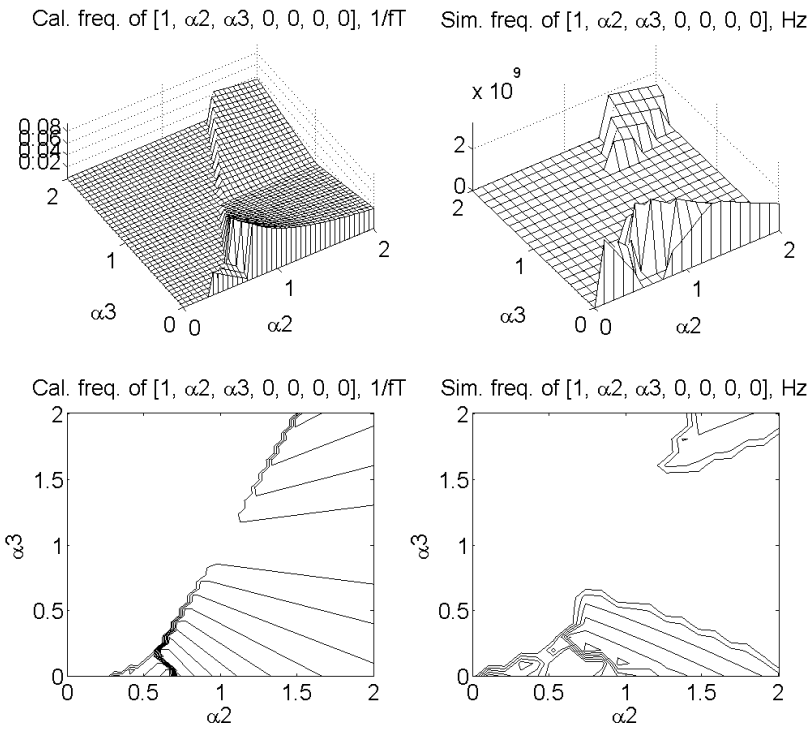

Figure 5-12.

Upper left: Calculated oscillation frequency of [1, α2, α3, 0, 0, 0, 0], depicted in three-dimensional space. The oscillation frequencies are normalized by f_T.

Upper right: Calculated oscillation frequency of [1, α2, α3, 0, 0, 0, 0]

Lower left: Calculated oscillation frequency of [1, α2, α3, 0, 0, 0, 0], depicted in two-dimensional space.

Lower right: Simulated oscillation frequency of [1, α2, α3, 0, 0, 0, 0], depicted in two-dimensional space.

MFRO's advantage over FRO is that it can be much faster. Several MFROs shown in figure 5–8 ~ 5–12 can generate very high frequency clock over 5Ghz at some range of α_2 and α_3. It is because the newly added feedforward paths can change the frequency dependent phase shift requirement for oscillation; the more phase shift, the higher oscillation frequency. In addition to its capability of high oscillation frequency generation, MFRO's another advantage over FRO and SPRO is: if they are properly designed, they can generate more clock phases at high frequency.

Although the MFRO's advantages we described above, it is difficult to find a proper α values for the desired design goal of MFRO. For instance, eight-stage MFRO has a seven dimensional α–space, that is too large to be searched by simulation. With the proposed MFRO model, the searching can be done very quickly.

For example, the eight-stage MFRO [1, α_2, α_3, 0, 0, 0, 0] in figure 5-7 has the same problem we have discussed in chapter three, that is, it hardly generate eight-phase clocks but four-phase clocks.

Using the proposed MFRO mode, we have found another eight-stage MFRO with a different α value, [1, 0, 0, α_4, 0, α_6, 0]. Figure 5-13 shows that its dominant oscillation mode and the expected oscillation frequency. It is shown that the MFRO operate in mode 3, a true eight phase mode, over a very large range of α. The expected oscillation frequencies are relatively high. Finally, figure 5-14 compares the calculation and the simulation results. Although the latch-up mode that is shown in the calculation does not appear in the simulation results, the overall oscillation behavior of the simulated MFRO agrees to the calculation very well.

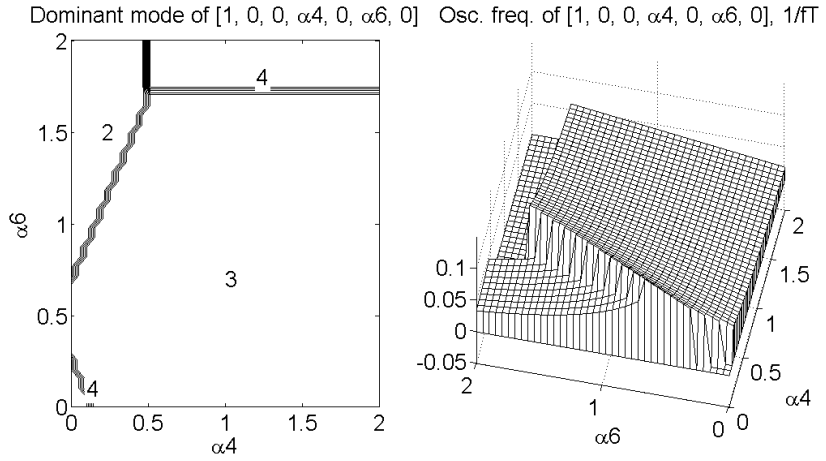

Figure 5-13. Another example of eight-stage MFRO.

Left: Determined dominant mode of five-stage MFRO, [1, 0, 0, α_4,0, α_6,0]

Right: Calculated oscillation frequency (1/fT)

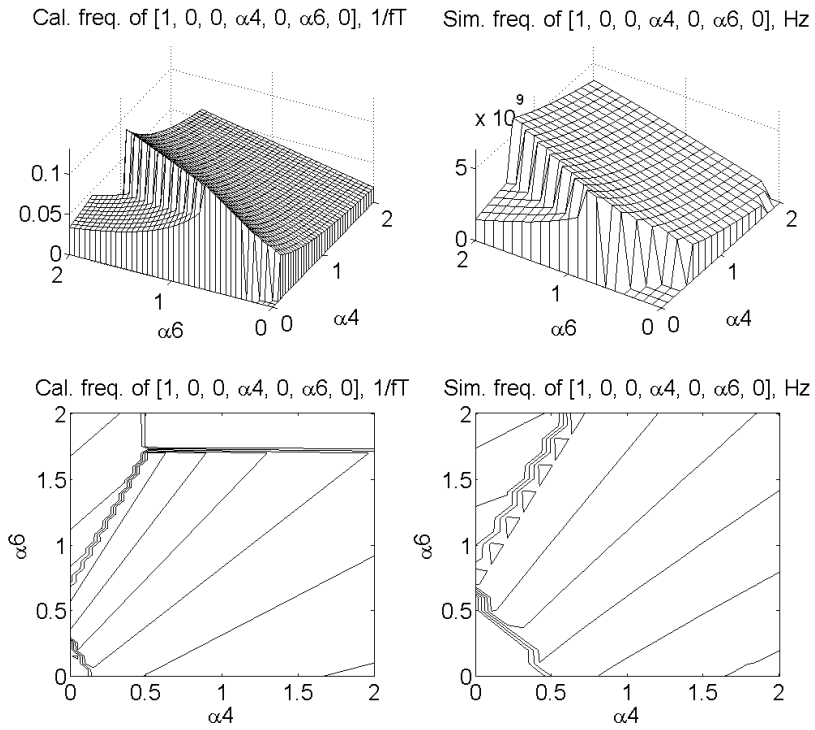

Figure 5-14.

Upper left: Calculated oscillation frequency of [1, 0, 0, α_4,0, α_6,0], depicted in three-dimensional space. The oscillation frequencies are normalized by f_T.

Upper right: Calculated oscillation frequency of [1, 0, 0, α_4,0, α_6,0]

Lower left: Calculated oscillation frequency of [[1, 0, 0, α_4,0, α_6,0], depicted in two-dimensional space.

Lower right: Simulated oscillation frequency of [1, 0, 0, α_4,0, α_6,0], depicted in two-dimensional space.

Chapter 6. 10-Gb/s CDR design using an eight–stage CMOS MFRO

Using some bandwidth extension techniques such as inductive peaking, capacitive degeneration, etc., high-speed CDRs over 10Gbps are realizable in inexpensive CMOS technology. Precise models of on-chip inductors as realistic simulation techniques using electro-magnetic (EM) field solvers are already available to circuit designers [20-23]. Indeed, on-chip inductor became a popular option for CMOS circuit designers who are in pursuit of high-speed [24-29]. However, on-chip inductors usually occupy much larger silicon area than the actual circuit core. Simple survey on the area-utilization of the CDR circuits designed with inductive peaking technique indicates that the die-area ratio of on-chip inductors to the entire chip easily exceeds 50%, even excluding bonding pads.

An alternative approach to realize a high-speed CDR circuit over 10Gbps in CMOS technology is to design it in multiphase clocking structure [30-32]. Operating in parallel but triggered in sequence with a $2\pi/N$ clock phase delay, N-data samplers can effectively achieve N-times faster sampling rate than that of a single data sampler triggered by full-rate clock. Another advantage of this approach over using on-chip inductors is that it saves a lot of die area. Typical on-chip inductors occupy much larger area than additional data samplers require. Since inductor's physical dimensions does not scale down, area-saving effect becomes more conspicuous when the CMOS technologies support smaller channel lengths are used.

Designing phase detectors (PDs) is also an issue of important concern in realizing high-speed CDR circuits. Bang-bang PD (BBPD) structure is usually chosen for high-speed CDR due to its simple structure and resulting capability of high-speed operation [27, 28, 33-35]. In addition, using BBPD removes need of a separate data slicer flip-flop, since the data slicer flip-flop is already embedded in the PD structure.

However, using BBPD often accompanies a problem due to its non-linear output characteristics. Designing the loop dynamics and finding appropriate loop filter parameters is much more difficult than with linear PDs. Also, linear PDs generally result in smaller jitter than bang-bang PDs in the extracted clock signals [36-38].

In this chapter, a one-fourth rate CDR circuit is designed in four-phase clocking structure. With a sampler array consists of eight low speed samplers triggered in sequence by 2.5GHz eight-phase clock, totally 10Gbps throughput is achieved without bulky on-chip inductors. It is also shown that a BBPD-similar structure with analog samplers instead of flip-flops generates output signals proportional to the actual clock phase error, resulting a linear PD.

6-1. Analog-sampler based linear PD

In this section, an analog sampler based linear PD is introduced. It has a similar structure to BBPD, however, the sampled data signal is not recovered into its logical value but is held until the phase error signal is extracted. To achieve analog sampling, the flop-flops of BBPD are replaced by analog samplers and additional slicers.

A schematic diagram of BBPD is shown in fig. 6-1. It consists of four flip-flops and two XOR gates. Fig. 6-2 depicts its operation in brief.

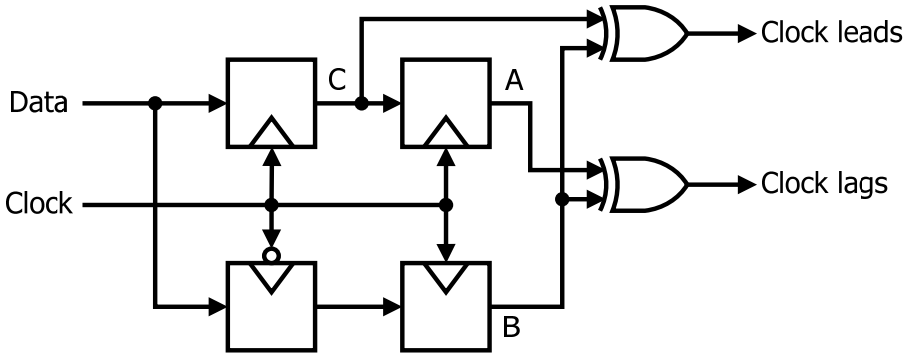

Figure 6-1. A schematic diagram of bang-bang PD

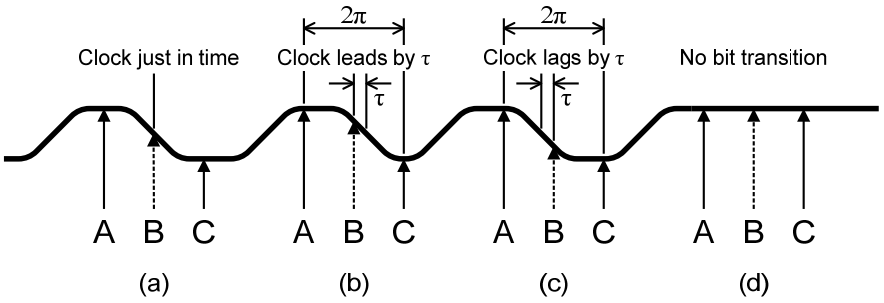

Figure 6-2. Operation of bang-bang PD

In fig. 6-2, A and C are sampled at the center of bit-interval therefore they represent retimed data bits, while B is sampled at bit-boundaries. If there is no bit-switching between A and C, as depicted in fig. 6-2(d), A, B and C has the same logic value the PD does not generate zero error signal. In the other hand, if the data bit is switched, the boundary sample B has the same logic value either to A or B after decision according to direction the clock phase error. Since output signals of the regenerative flip-flops are latched to binary logic levels, phase error signals of a BBPD are also in binary logic levels. This results in a BBPD response curve with infinity gain.

In the other hand, the actual data input signals require a certain amount of slewing time to complete bit switching as depicted in fig. 6-3. If analog samplers are used in the PD structure instead of regenerative latches, edge sample B has magnitudes that are proportional to the amount of phase error. Since XOR is basically the same to multiplication, resultant PD output is calculated as:

$$PD_{OUT} = \left| SR_D A_X \right| \frac{T}{2\pi} \tau \quad , \tag{6-1}$$

where SR_D is slew rate of input data signal, A_X is amplitude gain of the XOR gate, T is bit interval and τ is the phase error. Fig. 6-3 compares output characteristic curves of proposed linear PD and conventional BBPD.

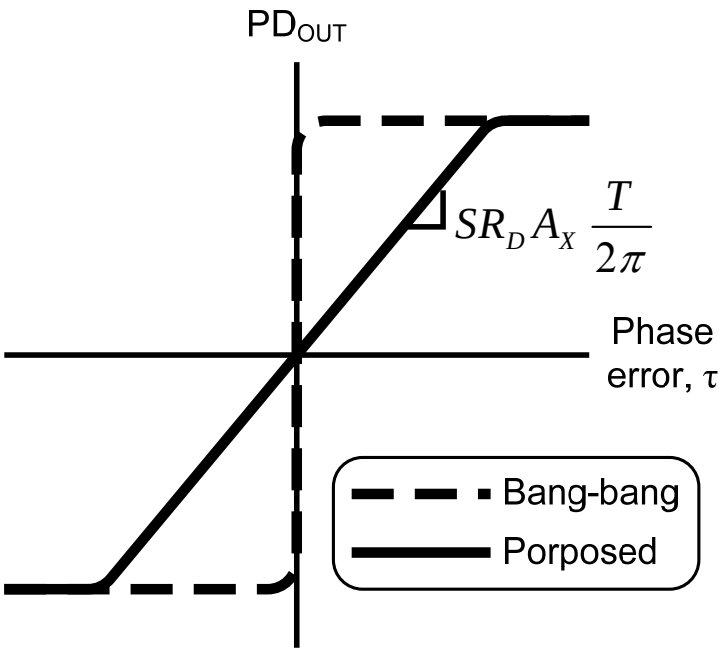

Figure 6-3. PD output response curves of proposed linear PD

The proposed linear PD can be realized in eight-phase clocking structure as depicted in fig. 6-4. Since the sampled signals are not aligned perfectly, the resultant PD output has correct value only over its 5/8 period. Although the other fraction of the output is determined by the random input data pattern, it has zero-DC value if the data is balanced. Consequently after filtered by loop-filter, the output of the PD has only the component proportional to the phase error.

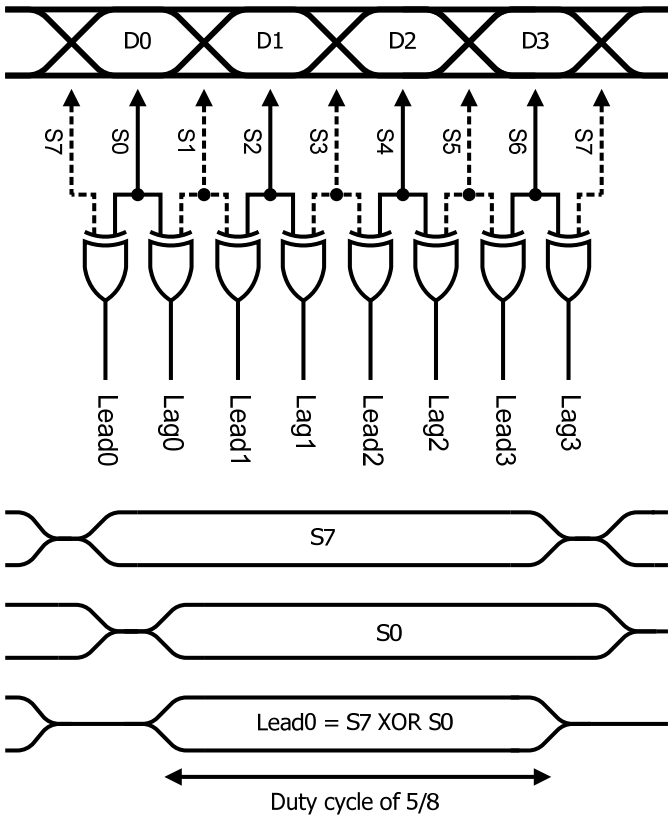

Figure 6-4. XOR array in PDs with eight-data samples

The analog samplers are designed with PMOS switches. The schematic diagram of the sampler is shown in figure 6-5(a). Clock and data waveforms of the sampler are shown in figure 6-5(b). The sampler's operation has three phases, and they are explained below.

--Clearing phase: Clearing pulse is applied. The PMOS transistor M3 is turned on and the voltage difference between the two capacitors are equalized. In other words, the data samples stored in the sampler is cleared. This clearing phase helps to minimize the inter-symbol interference in the data sampler.

--Tracking phase: M3 is turned off and sampling pulse is applied. The PMOS transistor M1 and M2 is turned on and the capacitors are charged to the input signal's voltage level. In the sampler implementation, no explicit capacitors are used. Instead, the parasitic capacitance at the input buffer's input terminals are utilized.

--Holding phase: M1, M2 and M3 are turned off. The stored charge in the capacitors is isolated and the sampled voltage level is held. The output buffer amplifies the sampled voltage to the logic level.

Since the sampled voltage is stored in parasitic capacitances, even a small leakage of electric charge through the PMOS switch can corrupt the stored voltage level. In the other hand in tracking phase, the PMOS switch should have as low resistance as possible for fast tracking. Consequently, a rail-to-rail swinging pulses are strongly desired.

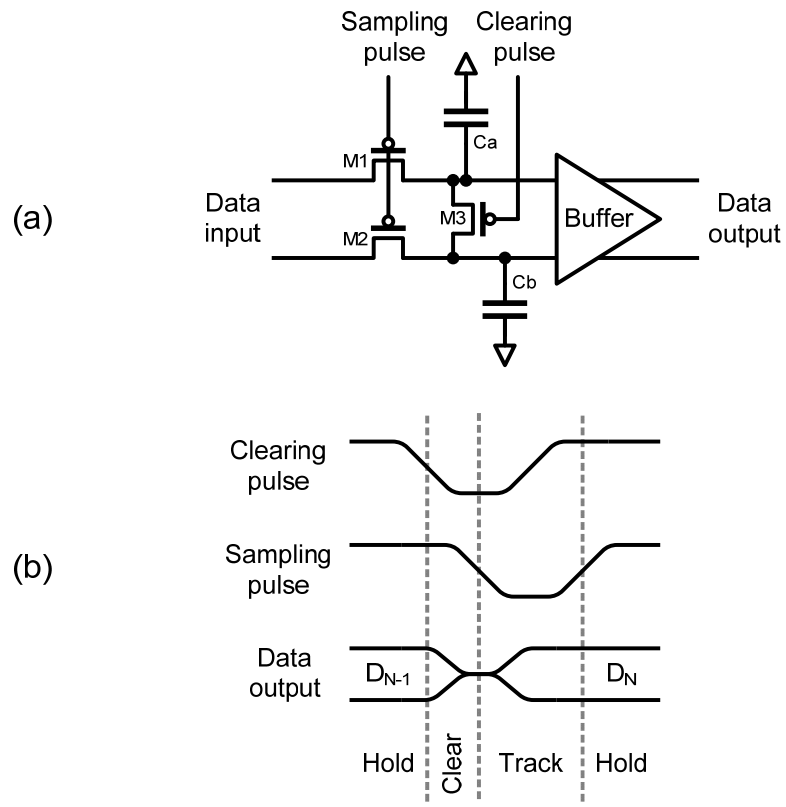

Figure 6-5. (a) Schematic diagram of data sampler. (b) Sampler operation.

Designed PD requires short pulse trains, clearing and sampling pulses, to operate properly as shown in the previous section. Figure 6-9 shows how to the sampling and clearing pulses are generated. The required pulse width is one fourth of the clock period. The desired pulse width is achieved from a NAND operation of ck_i and ck_{i-2}.

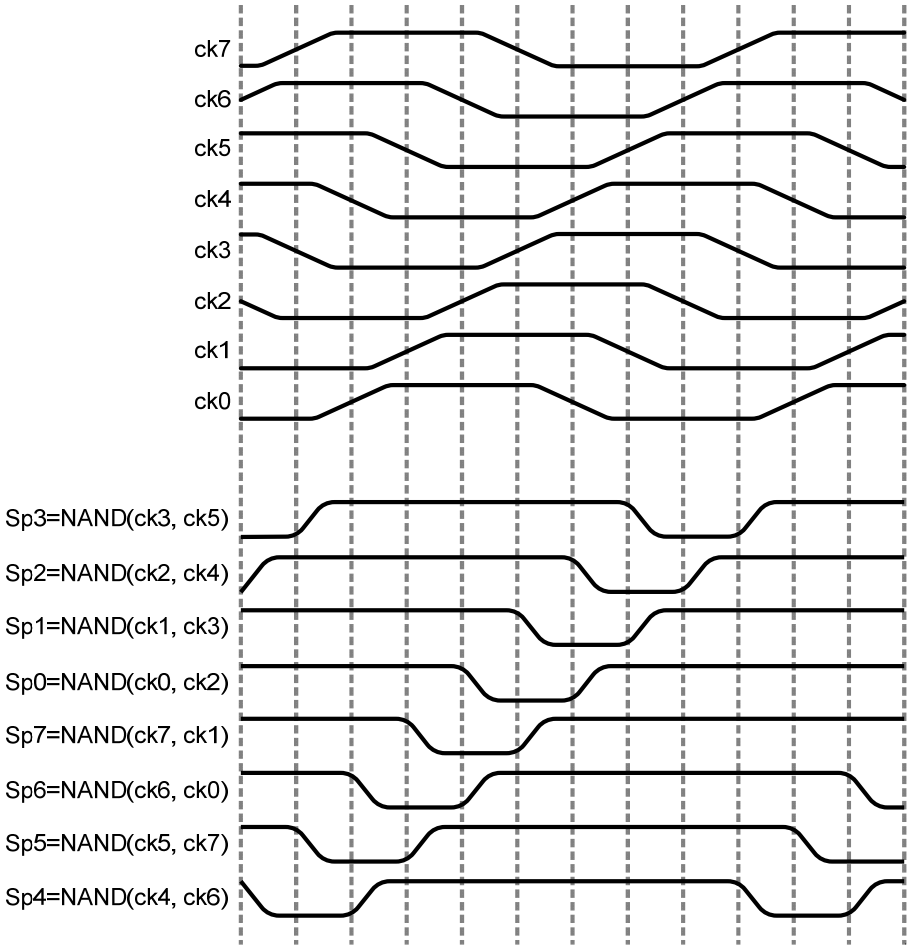

Figure 6-6. Sampling and clearing pulse generation using eight–phase clock.

6-2. Multiphase clock generation

In the chapter six, it is shown that the eight-stage MFRO [1, 0, 0, α4, 0, α6, 0] can generate eight-phase clock over very wide range of feedforward path ratios. Figure 6-7 shows the MFRO's oscillation modes and oscillation frequencies. The oscillation mode 4 represents latch-up state which should be avoided. In the other hand, the MFRO will generate four–phase clock in mode 2 which is not desired, too.

As we mentioned, process variation can cause mismatches between fabricated devices, and they lead to different feedforward ratios from what they are supposed to be. Considering those effect, feedforward ratios should be chosen to have enough margins from critical boundaries where oscillation mode changes abruptly. Since the design target frequency is 2.5Ghz, which is one fourth of 10Ghz, a moderate value of $0.1f_T$ and an α vector of [1, 0, 0, 0.46, 0, 1, 0] is chosen.

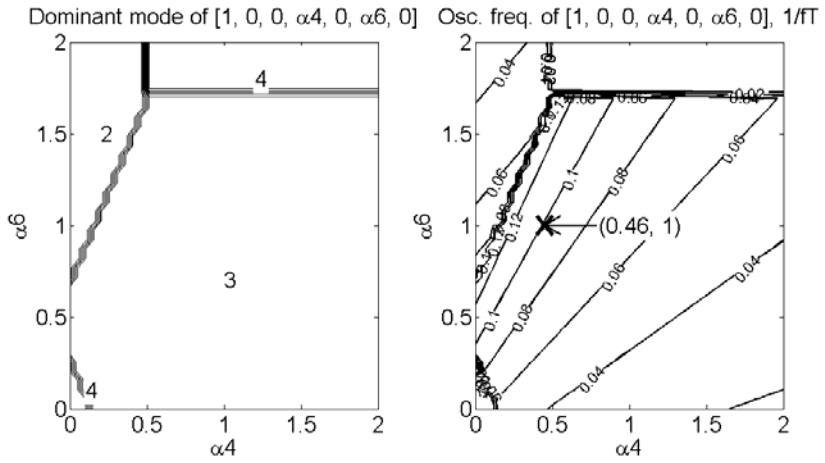

Figure 6-7. Determining feedforward ratio of eight-phase MFRO.

Figure 6-8 shows the delay element used for the designed MFRO. Basically it is a CMOS inverter with current-limiting MOS transistors. The MOS transistors are split into two for dual-frequency tuning: One is for fine frequency tuning and the other is for coarse frequency control. The coarse control terminal will be used for manual frequency acquisition, while the fine tuning node is connected the charge pumps through the loop filter. The simulated VCO gain is 1Ghz/V for the fine tuning voltage.

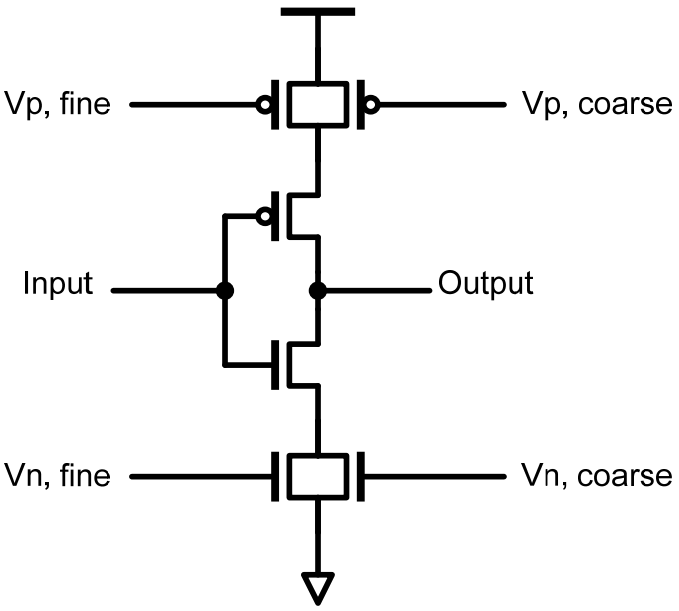

Figure 6-8. Delay element for MFRO.

6-3. One-fourth rate CDR circuit

Figure 6-9 shows the schematic diagram of designed CDR. It is designed with 0.13-μm CMOS parameters. Since we have used analog sampler to realize linear PD, which only track and samples the input data and does not regenerate its sampled signal, additional data slicers should be added in the circuit. They are included in the data aligner preceding the output buffers.

Figure 6-10 shows simulated VCO control voltage during phase acquisition. It is shown that the control voltage transition is smooth and requires about 100ns to achieve phase lock.

Figure 6-11 shows the layout of the designed CDR core which occupies only 88μm by 130μm. Figure 6-11 shows the microphotograph of fabricated chip. The total chip area is 1520μm by 1920μm.

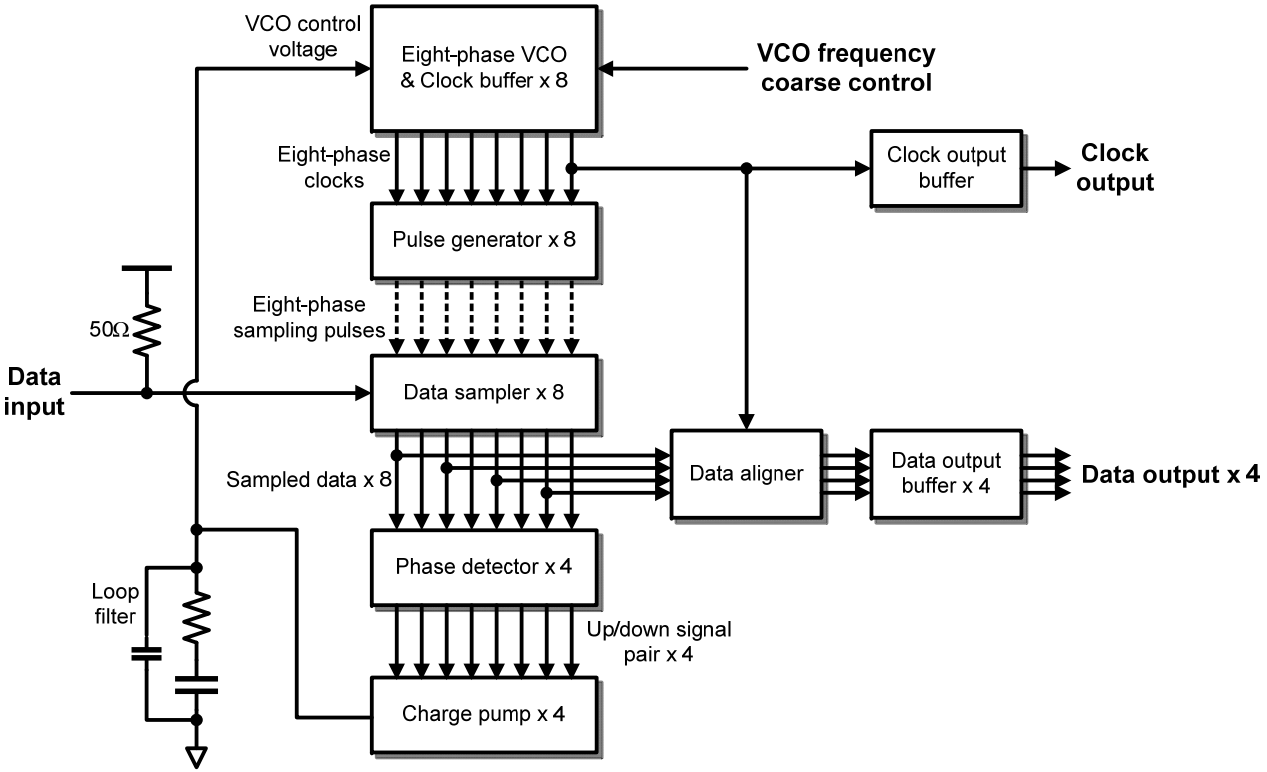

Figure 6-9. Schematic diagram of designed CDR.

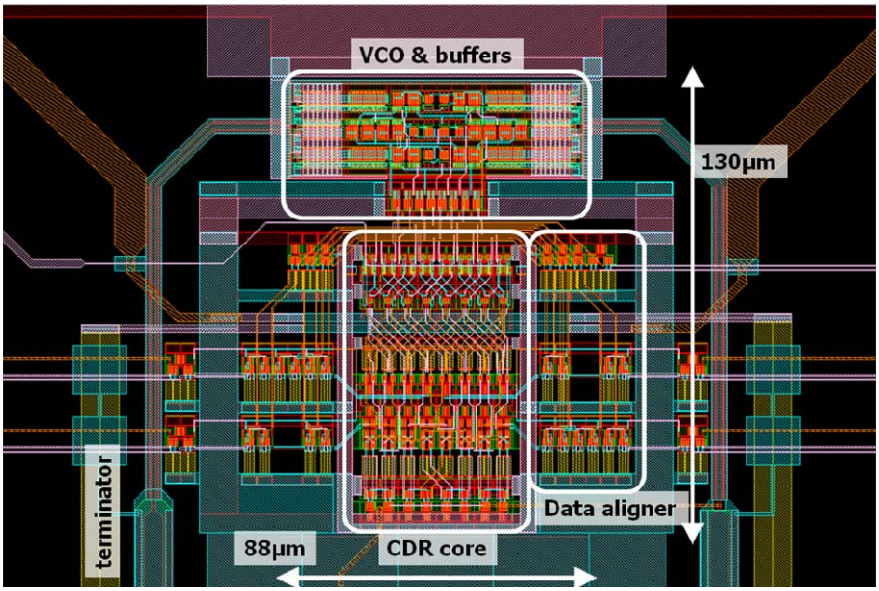

Figure 6-10. Layout close-up of designed CDR

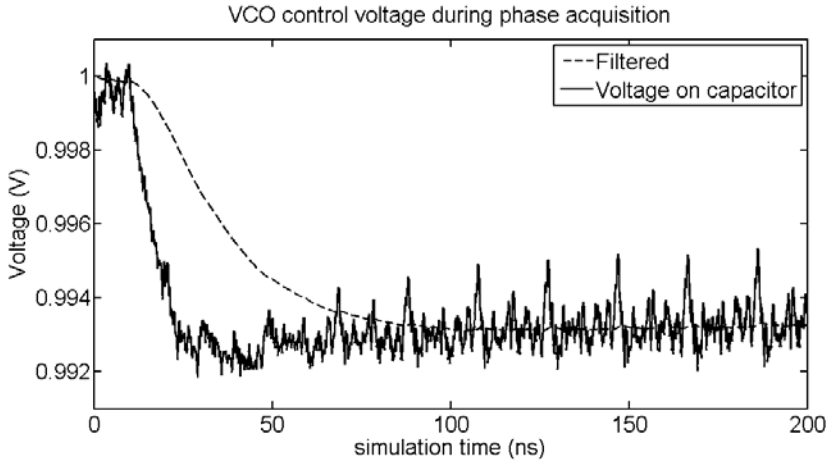

Figure 6-11. Simulated VCO control voltage during phase acquisition

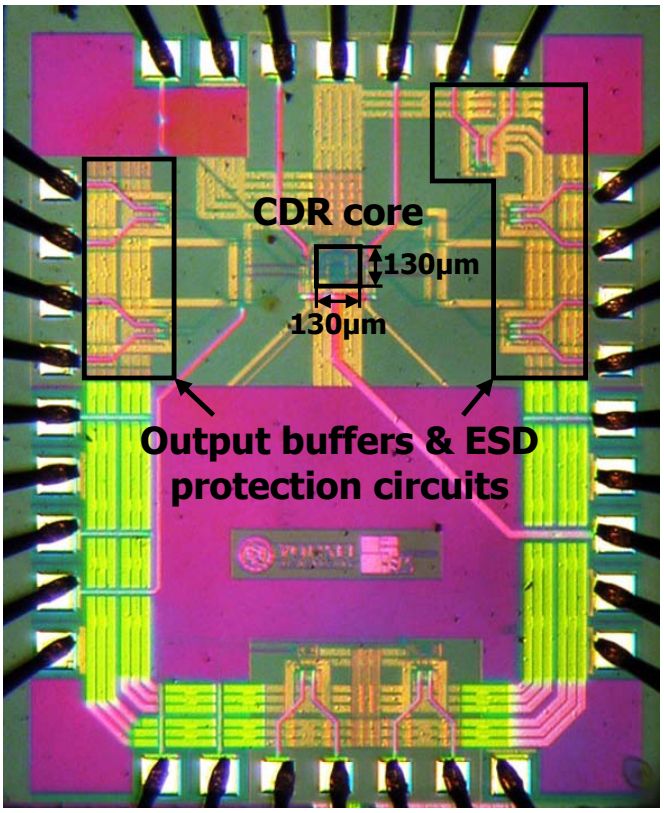

Figure 6-12. Microphotograph of fabricated CDR circuit

6-4. Measurement results

Fabricated chip was glued on test PCB and electrically connected using bonding wires. Logic bias voltages, charge pump bias voltages and VCO free-running frequency were controlled by potentiometers assembled on the test PCB. Figure 6-12 shows the diagram of measurement setup. Since it is a one-fourth rate clock recovery circuit, the extracted clock frequency is one-fourth of input data rate. For data input, 11~12.5Gbps PRBS31 pattern is used.

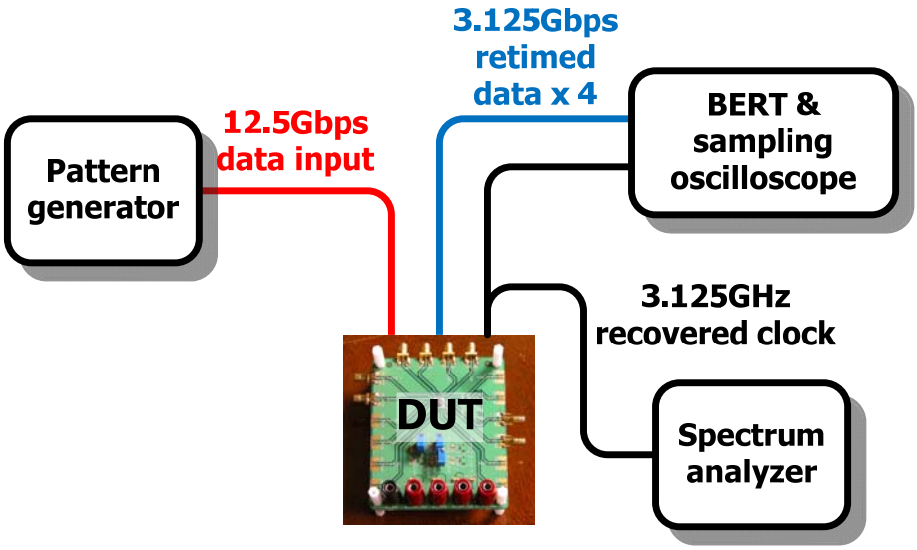

Figure 6-13. Measurement setup diagram

Figure 7-13 and 7-14 show the eye-diagram of recovered data and BER contour overlapped on the eye-diagram. PRBS31 data pattern was used. BER contour indicates sampling windows that guarantee a certain BER, therefore the wide opening of BER contour implies that the output of the CDR gives the larger timing and voltage margin to the circuit follows it. However, it cannot perfectly account for the actual BER performance of the CDR since it is estimated metric from the shape of eye-diagram. Actual BER can be measured by BER tester. BER measurement results are shown in figure 6-16. No error was reported over a 10-minute run with PRBS31 pattern at 12.5Gbps.

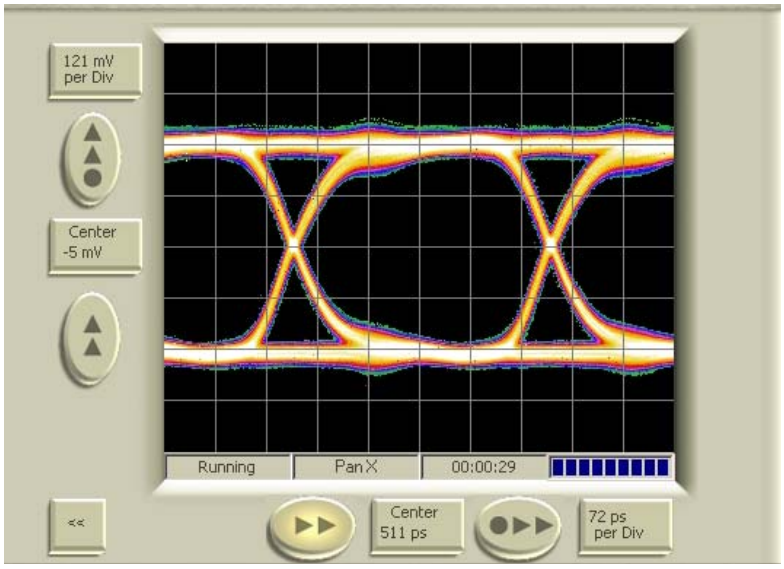

Figure 6-14. Eye-diagram of recovered data with PRBS pattern

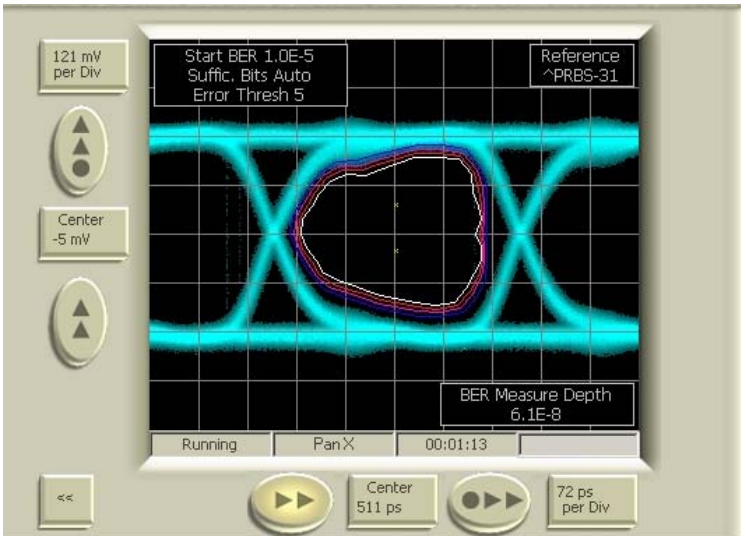

Figure 6-15. BER contour overlapped on the eye-diagram of recovered data

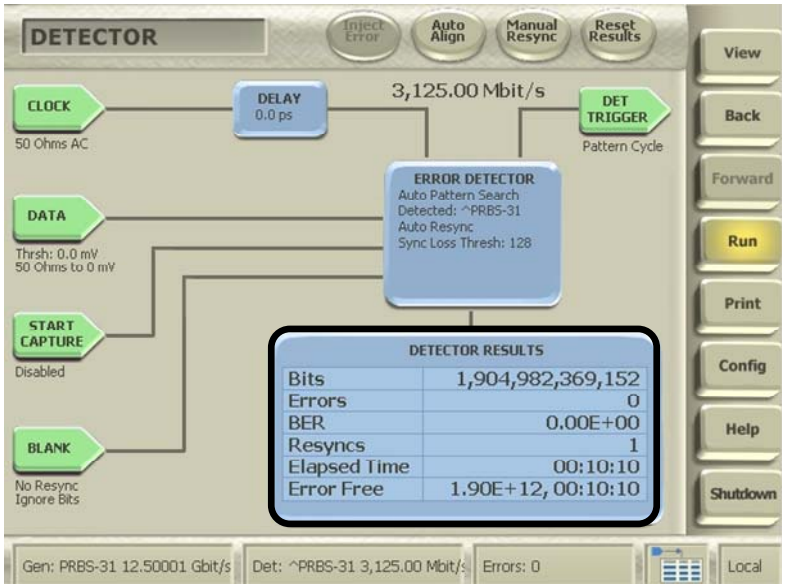

Figure 6-16. BER measurement results

Bit error probability can be estimated at a statistical confidence level following the method used in the Monte-Carlo simulation section in chapter three [17]. In the measurement no bit error was reported, and the total number of bit received per channel is more than 1.9×10^{12}. Simple calculation can show that the actual BER is less than 2.4×10^{-12} with 99% confidence for the measured data output channel.

The CDR circuit can operate up to 12.5Gbps with 1.6V power supply. The CDR draws 146mA from 1.6V power supply. The total power consumption is 234mW. The CDR core dissipates 20mW, VCO 44mW and the output buffer 170mW. Measured RMS clock jitter is less than 8ps. Measurement results are summarized in Table 6-1.

Table 6-1. Measurement results

Technology	0.13μm Low power, CIS CMOS
Power supply	1.6V
Input data rate	12.5 Gbps
Output data rate	3.125 Gbps (four channel)
Output clock frequency	3.125 Gbps
Recoverd Clock jitter	Less than 8ps(RMS)
Power consumption	272mW (including output buffers)
Core area	$0.011mm^2$
BER test results	Less than 2.4×10^{-12} with 99% confidence for PRBS31

Chapter 7. Summary

In the introduction of this dissertation, electrical oscillator is divided into two major groups: oscillators with explicit resonators and without. The representative examples of those two groups are LC-tank oscillator and RO. They show very different and distinctive characteristics in various aspects. Since electrical resonators usually consist of an inductor and a capacitor occupies a great chip area when they are fabricated on-chip, they are used only for the applications in which not very high area-utilization is required but very low phase noise is important.

In the other hand, since RO occupies very small die area, they are desired almost every time when the phase noise requirement is not so strict but available chip area is very small. Another great feature of RO is that it is very easy to have multiphase clock using RO since it has symmetrical structure. The number of clock phase is usually the same to the number of delay stages in the RO. Multiphase clock is often utilized for high-speed data processing circuits such as ADC and CDR.

Unfortunately, oscillation frequency of RO is inversely proportional to the number of the stage, therefore it is impossible to have high-frequency clock and larger number of clock phases at the same time with conventional RO structure. A popular way to overcome conventional RO's speed limitation is adding feedforward paths to the RO structure. Those ROs with additional signal paths are called FRO, and it was shown that FRO can achieve very high oscillation frequency even with large number of stages. Several publications gives good explanations for the high-speed operation of FROs, however, they are only successful to give qualitative understanding but not quantitative

design guides since they are not based on strict mathematical analysis, which is essential for optimized and robust design.

In this dissertation, an analysis method as well as design models and equations of FRO are proposed. The model is applicable to any number-stage FROs. It is discovered that FRO can have multiple oscillation modes during analysis, and calculation and simulation results are compared to verify the usefulness of the proposed model. The proposed design equations can predict FRO's behavior with a great accuracy.

Using the equations, five-stage FRO is optimized for its maximum oscillation frequency. Optimized FRO is fabricated 0.18μm CMOS technology, and it achieves up to 16GHz oscillation, which is the highest frequency ever reported with 0.18μm CMOS. Simulation results of optimized FRO with 65nm CMOS technology is also shown.

The proposed models and equations are investigated farther to extend them to MFRO analysis. Also, a new naming convention for MFRO is proposed using a vector of feedforward ratios α. Since an N-stage RO can have up to N-1 feedforward paths, which leads to a N-1 dimensional α space, it is difficult to find a proper value of αs without simple and fast searching method. In the dissertation, for example, the design equation is programmed into MATLAB script to test and find eight-stage MFRO structure having eight-phase clock output over a wide range of α space.

In the last part of the dissertation, a one-fourth rate 10Gbps CDR circuit is designed with eight-phase MFRO. At such a high-speed, inductive peaking technique with on-chip inductors is usually utilized to increase data throughput at a cost of huge die area. Instead of on-

chip inductors, eight -phase clocking structure can be used to decrease actual operation frequency to one-fourth rate while the total data throughput is kept to the same.

An analog sample based linear PD is also proposed. It has a BBPD-like structure but analog samplers are utilized to achieve linear phase error response. Designed CDR circuit is fabricated using 0.13μm CMOS technology and occupies very small chip area due to the lack of on-chip inductors. It can successfully operate with up to 12.5Gbps input having PRBS31 bit pattern.

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Appendix

MATLAB m-file for FRO analysis

fro.m

```
%
%   Written by Pyung-Su Han, 2008
%
%   Input
%   ====================================
%   n: number of stages
%   a1min: min. feedforward ratio
%   a1max: max. feedforward ratio
%   a1p: number of calculations
%   dcgain: DC gain of inverting amplifier
%
%   Output
%   ====================================
%   gain: unit stage gain, a1p x n-1 matrix
%   gamma: frequency dependet phase shift, a1p x n-1
matrix
%   a1: feedfoward ratio vector, a1p vector
%   pc: mode flag, a1p x n-1 matrix;
%             1(phase condition sufficed)
%             0(phase condition is not sufficed)
%             -1(latch-up)
%   mode: determined dominant mode, a1p vector
%   ff: calculated oscillation frquency, 1/fT


function [gain gamma a1 pc mode ff] = fro(n, a1min, a1max,
a1p, dcgain)

th = 2 * pi / n;

a1 = linspace(a1min, a1max, a1p);

g1 = 0;
g2 = 0;

for(i=1:1:length(a1))
   for(k=1:1:n-1)
      t = k* th;
```

```
        g1 = cos(t) + a1(i) * cos(2 * t);
        g3 = sin(t) + a1(i) * sin(2 * t);
        g2 = 1 + a1(i);
        ccc = 1 + a1(i) * cos(t);
        sss = -a1(i) * sin(t);
        gain(i, k) = -g1 / g2;
        temp = atan(sss / ccc);
        if(ccc < 0)
            temp = temp + pi;
        end
        betha(i, k) = temp;
        gamma(i, k) = t - betha(i,k) - pi;
        temp = mod(gamma(i, k) + pi, 2 * pi);
        gamma(i, k) = temp - pi;
        gg1(i, k) = g1;
        gg3(i, k) = g3;
    end
end

gamma = 1 / pi * gamma;
gain = dcgain * gain;

for(i=1:1:length(a1))
    for(k=1:1:n-1)
        if(gamma(i, k) <= 0 && gamma(i, k) > -0.5)
            pc(i, k) = 1;
        else
            pc(i, k) = 0;
        end
        if (gamma(i, k) > -1e-5 && gamma(i, k) < 1e-5)
            pc(i, k) = -1;
        end
        if (gamma(i, k) > 1 - 1e-5 && gamma(i, k) < 1 +
1e-5)
            pc(i, k) = -1;
            gain(i, k) = -gain(i, k);
        end

    end
end

for(i=1:1:length(a1))
    mode(i) = 0;
    gtemp = 1;
    for(k=1:1:n-1)
        if(pc(i, k) ~= 0 && gain(i, k) > gtemp)
```

```
            mode(i) = k;
            gtemp = gain(i, k);
        end
    end
end

for(i=1:1:length(a1))
    if(mode(i) == 0)
        ff(i) = 0;
    else
        ff(i) = -1/15 * gg3(i, mode(i)) / gg1(i, mode(i));
    end
end
```

MATLAB m-file for MFRO with two feedforward paths

mfro.m

```
%
%   Written by Pyung-Su Han, 2008
%
%   Input
%   ====================================
%   n: number of stages
%   f1: feedforward path index 1
%   a1min: min. feedforward ratio 1
%   a1max: max. feedforward ratio 1
%   a1p: number of calculations 1
%   f2: feedforward path index 2
%   a2min: min. feedforward ratio 2
%   a2max: max. feedforward ratio 2
%   a2p: number of calculations 2
%   dcgain: DC gain of inverting amplifier
%
%   Output
%   ====================================
%   gain: unit stage gain, a1p x n-1 matrix
%   gamma: frequency dependet phase shift, a1p x n-1
matrix
%   a1: feedforward ratio vector 1
%   a2: feedforward ratio vector 2
%   pc: mode flag, a1p x n-1 matrix;
%             1(phase condition sufficed)
%             0(phase condition is not sufficed)
%             -1(latch-up)
%   mode: determined dominant mode, a1p vector
%   ff: calculated oscillation frquency, 1/fT

function [gain gamma a1 a2 pc mode ff] = mfro(n, f1,
a1min, a1max, a1p, f2, a2min, a2max, a2p, dcgain)

th = 2 * pi / n;

a1 = linspace(a1min, a1max, a1p);
a2 = linspace(a2min, a2max, a2p);

g1 = 0;
```

```
g2 = 0;

for(i=1:1:length(a1))
   for(j=1:1:length(a2))

   for(k=1:1:n-1)
      t = k* th;
      g1 = cos(t) + a1(i) * cos((1+f1) * t) + a2(j) *
cos((1+f2) * t);
      g3 = sin(t) + a1(i) * sin((1+f1) * t) + a2(j) *
sin((1+f2) * t);
      g2 = 1 + a1(i) + a2(j);
      ccc = 1 + a1(i) * cos(f1 * t) + a2(j) * cos(f2 *
t);
      sss = -a1(i) * sin(f1 * t) -a2(j) * sin(f2 * t);
      gain(i, j, k) = -g1 / g2;
      temp = atan(sss / ccc);
      if(ccc < 0)
         temp = temp + pi;
      end
      betha(i, j, k) = temp;
      gamma(i, j, k) = t - betha(i, j, k) - pi;
      temp = mod(gamma(i, j, k) + pi, 2 * pi);
      gamma(i, j, k) = temp - pi;
      gg1(i, j, k) = g1;
      gg3(i, j, k) = g3;
   end
   end
end

gamma = 1 / pi * gamma;
gain = dcgain * gain;

for(i=1:1:length(a1))
   for(j=1:1:length(a2))
      for(k=1:1:n-1)
      if(gamma(i, j, k) <= 0 && gamma(i, j, k) > -0.5)
         pc(i, j, k) = 1;
      else
         pc(i, j, k) = 0;
      end
      if (gamma(i, j, k) > -1e-5 && gamma(i, j, k) < 1e-
5)
         pc(i, j, k) = -1;
      end
      if (gamma(i, j, k) > 1 - 1e-5 && gamma(i, j, k) <
```

```
1 + 1e-5)
          pc(i, j, k) = -1;
          gain(i, j, k) = -gain(i, j, k);
       end
       end

   end
end

for(i=1:1:length(a1))
   for(j=1:1:length(a2))
   mode(i, j) = 0;
   gtemp = 1;
   for(k=1:1:n-1)
      if(pc(i, j, k) ~= 0 && gain(i, j, k) > gtemp)
         mode(i, j) = k;
         gtemp = gain(i, j, k);
      end
   end
   end
end

for(i=1:1:length(a1))
   for(j=1:1:length(a2))
   if(mode(i, j) == 0)
      ff(i, j) = 0;
   else
      ff(i, j) = -1/15 * gg3(i, j, mode(i, j)) / gg1(i,
j, mode(i, j));
   end
   end
end
```