Design Optimization of Hybrid-Integrated 20-Gb/s Optical Receivers

Hyun-Yong Jung, Jin-Sung Youn, and Woo-Young Choi*

Abstract—**This paper presents a 20-Gb/s optical receiver circuit fabricated with standard 65-nm CMOS technology. Our receiver circuits are designed with consideration for parasitic inductance and capacitance due to bonding wires connecting the photodetector and the circuit realized separately. Such parasitic inductance and capacitance usually disturb the high-speed performance but, with careful circuit design, we achieve optimized wide and flat response. The receiver circuit is composed of a transimpedance amplifier (TIA) with a DC-balancing buffer, a post amplifier (PA), and an output buffer. The TIA is designed in the shunt-feedback configuration with inductive peaking. The PA is composed of a 6-stage differential amplifier having interleaved active feedback. The receiver circuit is mounted on a FR4 PCB and wire-bonded to an equivalent circuit that emulates a photodetector. The measured transimpedance gain and 3-dB bandwidth of our optical receiver circuit is 84 dBΩ and 12 GHz, respectively. 20-Gb/s $2^{31}-1$ electrical pseudo-random bit sequence data are successfully received with the bit-error rate less than 10^{-12}. The receiver circuit has chip area of 0.5 mm × 0.44 mm and it consumes excluding the output buffer 84 mW with 1.2-V supply voltage.**

Index Terms—**Bonding wire, CMOS, hybrid integration, optical receiver circuit**

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I. INTRODUCTION

Recently, the demands for optical interconnects are greatly increasing in short-reach applications such as chip-to-chip and board-to-board interconnects due to tremendous bandwidth requirement growth for many data-processing applications. Although monolithically integrated optical receivers that contain both photodetectors (PDs) and electronic circuits are highly desirable [1], most integrated optical receivers for high-speed applications are based on III-V semiconductors which may have disadvantages in cost consideration. A hybrid approach in which photodetectors and receiver circuits are implemented in different technologies and electrically connected on a board is routinely used. However, such a hybrid approach necessarily includes undesired parasitic capacitance and inductance [2], which can limit the high-speed operation and distort the frequency response of the optical receiver. One possibility of mitigating the influence of such parasitic effects is adding compensation circuits between PD and transimpedance amplifier (TIA) [3, 4]. However, such an approach increases the overall chip size. In this paper, we take another approach in which we include the parasitic effects in our TIA design so that it can be used for enhancing the receiver bandwidth. For this, we first characterize characterize the influence of parasitic capacitance and inductance due to bonding wires and, with this knowledge, optimize our receiver circuit design. It is found that the influence of parasitic inductance of bonding wires can be optimized with careful design for the receiver circuit bandwidth using less passive inductors. With our design-optimized receiver circuit realized in 65-nm CMOS, we demonstrate 20-Gb/s

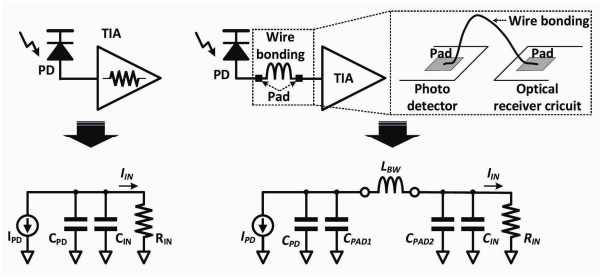


Fig. 1. Equivalent circuit model for (a) monolithic integration, (b) hybrid integration.

operation. This paper is organized as follows. We firstly examine design consideration for successful hybrid integration involving pad capacitances and bonding wire inductances in Section II. Section III discusses optical receiver circuit design. Measurement results of our optical receiver circuit are presented in Section IV. Finally, Section V concludes the paper.

II. Bandwidth Optimization of Hybrid Integration

There are many packaging methods for hybrid integration such as wire bonding, ball grid array, and flip-chip bonding. Among these, our investigation is focused on hybrid integration with wire bonding as it is simplest and most cost-effective. Figs. 1(a) and (b) show the equivalent circuit model for monolithic and hybrid integration of the part connecting PD and the receiver circuit, respectively. I_{PD} and C_{PD} represent the photocurrent and junction capacitance of PD; C_{IN} and R_{IN} indicate the input capacitance and resistance of TIA; C_{PAD1} and the C_{PAD2} are pad capacitances for PD and TIA; L_{BW} denotes bonding wire inductance.

The 3-dB bandwidth of a monolithically integrated optical receiver can be continuously increases by reducing R_{IN} as the transfer function for I_{IN}/I_{PD} is given as $1/2\pi R_{IN}(C_{PD}+C_{IN})$. However, for hybrid integration, smaller R_{IN} does not guarantee larger bandwidth. In this case, the transfer function is given as

$$\frac{I_{IN}}{I_{PD}} = \frac{1}{s^3 L_{BW} C_1 C_2 R_{IN} + s^2 L_{BW} C_1 + s(C_1 + C_2) R_{IN} + 1} \quad (1)$$

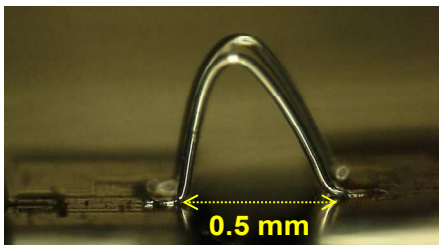


Fig. 2. Microphotograph of wire-bonding face in profile.

where $C_1 = C_{PD} + C_{PAD1}$ and $C_2 = C_{PAD2} + C_{IN}$. In optical receiver design, R_{IN} is usually small so that we can assume $R_{IN} \ll |1/sC_2|$ in the frequency range of interest. Then, Eq. (1) can be simplified as second-order system as

$$\frac{I_{IN}}{I_{PD}} \sim \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2)$$

with ω_n, the natural frequency, given as $1/\sqrt{L_{BW}C_1}$ and, ζ, the damping ratio, given as . With $\zeta = \sqrt{2}/2$, ω_n becomes the largest 3-dB bandwidth with flat response, which is determined by C_1 and L_{BW}.

Among the parameters used above, C_1 is determined by the characteristics of the target PD and pad capacitance. For our investigation, the target PD has C_{PD} of 177-fF and C_{PAD1} of 50-fF, resulting in C_1 of 227-fF. According to Eq. (2), in order to achieve large bandwidth, L_{BW} should be minimized. Fig. 2 shows a microphotograph of a bonding wire connecting two chips. Because the minimum distance between two chips for wedge bonding is 0.5 mm with the wedge bonder available to us, the smallest bonding wire length we can have is about to 1 mm. Since the wire-bonding inductance for the wire used in our investigation is 0.8 nH/mm [5]. The minimum L_{BW} that we can have is about 0.8 nH.

Since , we can determine the relationship between R_{IN} and C_{IN} for the parameter values determined above as shown in Fig. 3. For C_{PAD2}, 50-fF is used assuming the pad size is 90 μm ×50 μm.

Selecting R_{IN} so that $\zeta = \sqrt{2}/2$ is important in our optical receiver design since this condition produces the largest bandwidth without pronounced peaking in the second-order system [6]. Fig. 4(a) shows the simulation frequency responses of hybrid-integrated optical

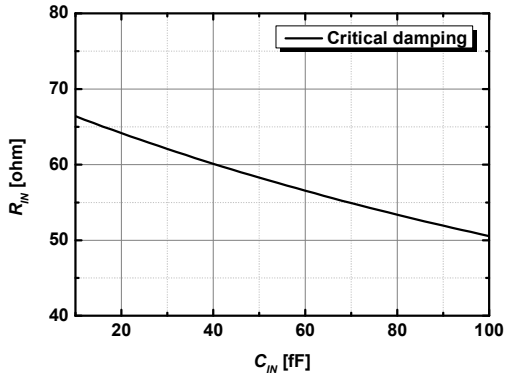
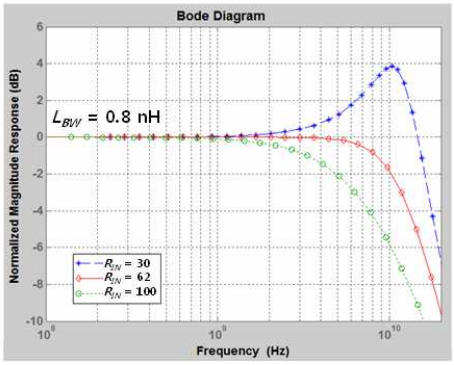
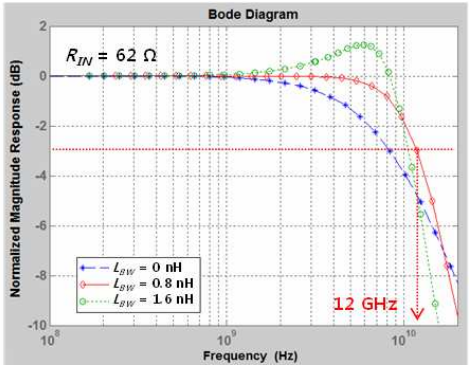


Fig. 3. Relation between R_{IN} and C_{IN} for $\zeta = \sqrt{2}/2$.



(a)



(b)

Fig. 4. Simulated normalized magnitude response for various (a) R_{IN}, (b) L_{BW} in hybrid-integrated optical receiver design.

receivers having various R_{IN}. For this simulation, parasitic capacitance and inductance values estimated above are used along with 30 fF of C_{IN}. Unlike the case of monolithic integration, the receiver bandwidth does not get better with smaller R_{IN}. For example, R_{IN} = 30 Ω produces peaking in the frequency response that can distort the received data eye. Fig. 4(b) shows how the frequency response changes with different values of L_{BW} for R_{IN} = 62 Ω. As can be seen, the optimal frequency response requires an optimal value of L_{BW}, which shows larger bandwidth than the case of no bonding wire inductance. We find that there is about +/− 10-% variance in L_{BW} due to the bonding wire length difference in actual wire bonding operation.

III. CMOS Optical Receiver Circuit Design

Fig. 5 shows the block diagram of our optical receiver circuit. An equivalent circuit for PD is used for evaluating receiver circuit performance. The receiver circuit includes TIA with DC-balancing buffer, post amplifier (PA) and output buffer with 50-Ω termination, for measurement with test instruments.

1. TIA with DC-Balancing Buffer

Although several TIA configurations are possible for high-speed TIA operation such as current-mode TIA [4], TIAs with regulated cascode input stage [7] or π-type inductive peaking [8], these have relatively low gain-bandwidth products, large chip area, and high input noises. Instead, a shunt-feedback TIA is used in our design. Fig. 6(a) shows the schematic diagram of our shunt-feedback TIA. It consists of two feedback resistors and a core amplifier which is a two-stage differential amplifier with inductive peaking. The core amplifier employs two center-tap inductors to achieve large bandwidth with a small chip area. C_{IN} of shunt-feedback TIA is determined by the input MOSFET size of TIA core amplifier and R_{IN} is simply given as $R_F/(1+A_{core})$ where R_F indicates feedback resistance and A_{core} is voltage gain of TIA core amplifier. C_{IN} of 30-fF is used for our design that provides sufficient gain and bandwidth for the TIA core amplifier. Then, with A_{core} of 12 dB [V/V] and R_F of 300 Ω, R_{IN} is determined to 60 Ω. Fig. 7 shows the normalized magnitude response of the designed TIA in post-layout simulation done with the PD equivalent. As can be seen in the figure, 3-dB bandwidth is enhanced from 8 GHz to 12 GHz with 0.8-nH of L_{BW}. Responses with L_{BW} = 0.7 and 0.9 nH are also shown, corresponding to roughly +/−10-% variance in L_{BW}. As can be seen, the influence of L_{BW} variance on the transimpedance response is not significant.

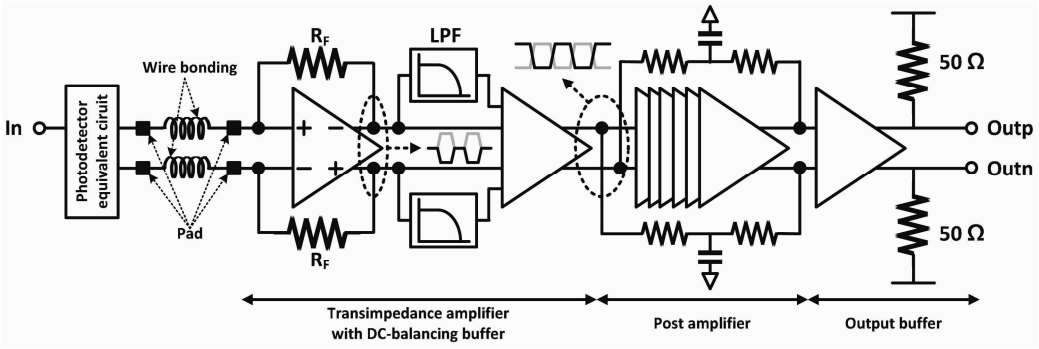
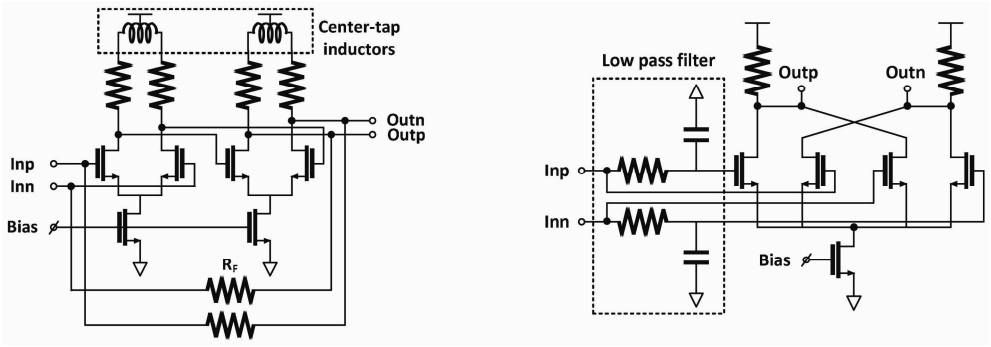


Fig. 5. Block diagram of the fabricated optical receiver circuit.



(a) (b)

Fig. 6. Schematic diagram of designed (a) transimpedance amplifier, (b) DC-balancing buffer.

Since the photo-generated currents are supplied to only one port of differential TIA inputs, TIA produces output differential signals with a DC offset, which causes a decision threshold problem. To solve this, a DC-balancing buffer is added at the TIA output. Fig. 6(b) shows the schematic of the DC-balancing buffer which consists of two low-pass filters and f_T-doubler. The low cut-off frequency of the buffer is set to 5 MHz to avoid any DC wander.

2. Post Amplifier

The PA provides additional gain to drive the following stage, which can be output buffers in our present design or a clock and data recovery circuit in an optical receiver with additional blocks integrated. Fig. 8(a) shows the simplified block diagram of the PA composed of six gain stages with interleaved active feedback [4], which allows sufficient gain and bandwidth for 20-Gb/s operation. Fig. 8(b) shows the schematic diagram for the part inside the box in Fig. 8(a).

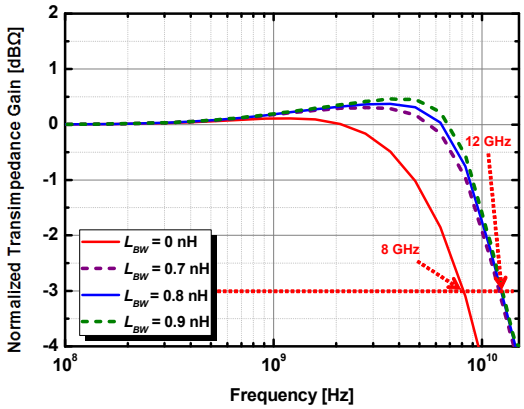
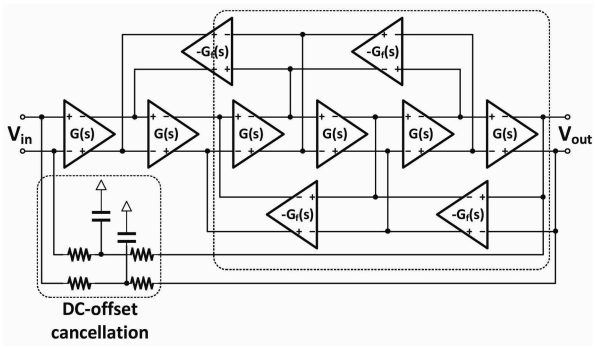


Fig. 7. Normalized transimpedance response.

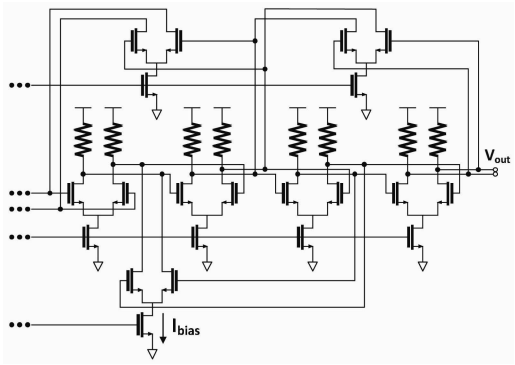
IV. Measurement Results

Fig. 9 shows the chip photograph of the optical receiver fabricated with standard 65-nm CMOS technology. Our receiver circuit occupies 0.44 mm × 0.5 mm of chip area, and consumes 84 mW with 1.2-V supply excluding output buffers.

Fig. 10 shows the measurement setup. The photodetector equivalent circuit realized with the same



(a)



(b)

Fig. 8. (a) Block diagram, (b) schematic diagram.

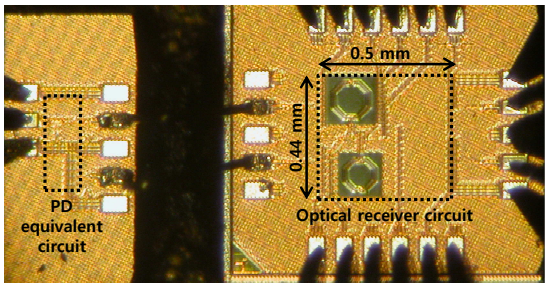


Fig. 9. Microphotograph of the fabricated optical receiver.

65-nm CMOS technology and the optical receiver circuit are connected with bonding wires on a FR4 test board. The measurements are done with on-wafer probing. The PD equivalent circuit includes a 50-Ω matching resistor, a 5-kΩ resistor that converts applied voltages into currents, and two 177-fF MIM capacitors emulating PDs. Fig. 11 shows measured and simulated transimpedance frequency responses. The measured transimpedance gain and 3-dB bandwidth is 86 dBΩ and 12 GHz, respectively. Fig. 12(a) shows the measured bit-error rate (BER) performance as a function of input current swing. 20-Gb/s 2^{31}−1 PRBS data detection is successfully achieved with BER less than 10^{-12}. Fig. 12(b) also shows the

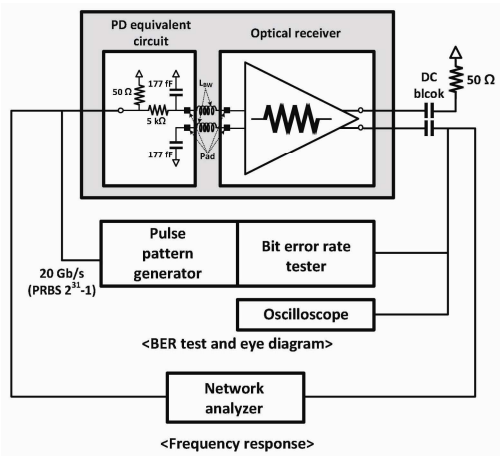


Fig. 10. Measurement setup.

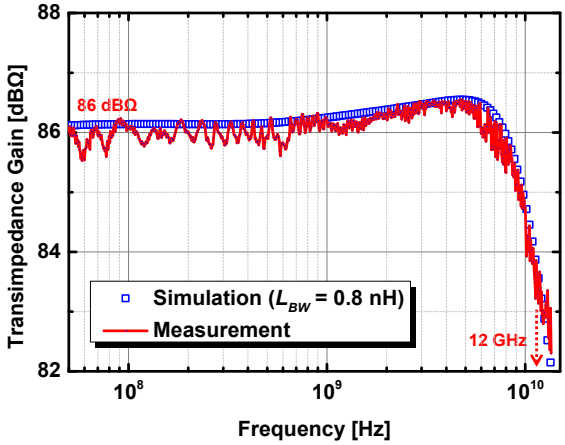


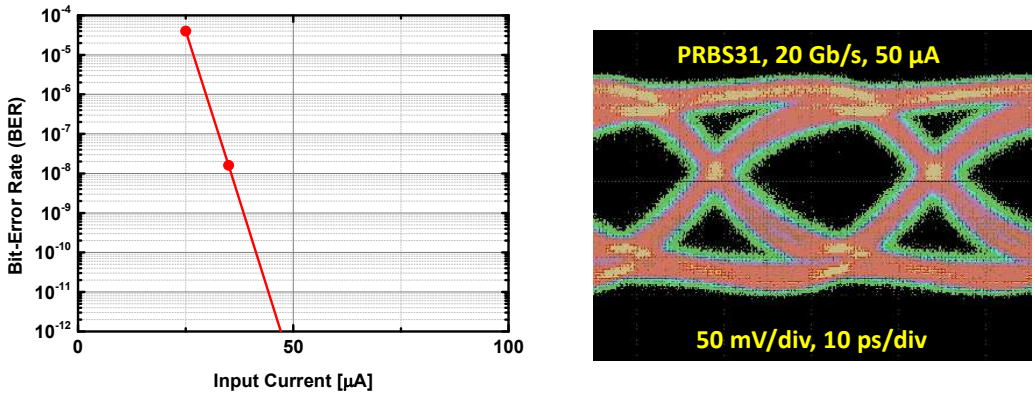
Fig. 11. Measured and simulated magnitude response.

measured 20-Gb/s eye diagram with input current swing of 50 μA_{pp}. Fig. 13 shows measured and simulated output noise voltage density without the PD equivalent circuit. The measurement result is well matched with the simulation result. The extracted input-referred noise current density ($i_{n,in}$) with C_I = 227 fF and L_{BW} = 0.8 nH is also shown in Fig. 13. The input-referred rms noise current can be calculated as [9]

$$I_{n,Rx}[A_{rms}] = \sqrt{\frac{f_{BW,N}}{f_{BW,S}} \int_{100MHz}^{f_{BW,S}} \overline{i_{n,in}^2} df} = 2.55\mu A_{rms} \quad (3)$$

where $f_{BW,S}$ and $f_{BW,N}$ is the signal and equivalent noise bandwidth of the receiver circuit, respectively. The extracted average input-referred noise current density is

$$I_{n,in,avg} = \frac{I_{n,Rx}}{\sqrt{f_{BW,S}}} = 23.3pA/\sqrt{Hz} \quad (4)$$



(a) (b)

Fig. 12. (a) Measured bit-error rate versus input current, (b) measured 20-Gb/s single-ended eye diagram.

Table 1. Performance comparison for the optical receiver

	[4]	[11]	[12]	This work
Technology [nm]	130-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS
Data rate [Gb/s]	20	25	25	20
Bandwidth [GHz]	12.6	22.8	21.4	12
Supply [V]	1.2	1.8 (TIA) / 1.0 (PA)	3.3 (TIA) / 1.0 (PA)	1.2
Power dissipation [mW]	38.3	74	90.9	84
Transimpedance [dBO]	60	69.8	76.8	86
$I_{n,in,avg}$ [pA/$\sqrt{Hz}$]	42.2	23.2	17.8	23.3
Chip area [mm^2]	0.22	0.4	0.32	0.22
FOM [GHzO/mW]	329	952	1629	2850

The sensitivity of our optical receiver circuit for BER less than 10^{-12} can be estimated using the following equation [10]

$$Sensitivity \approx 10\log\left[\frac{14.1I_{n,Rx}(r_e+1)}{2\rho(r_e-1)}1000\right] \quad (5)$$

where ρ is the PD responsivity and r_e is the extinction ratio of the modulator. With ρ = 0.5 A/W and r_e = 5 dB, above equation gives sensitivity of −12.7 dBm for $I_{n,Rx}$ of 2.55 μA_{rms}.

Table 1 shows performance comparison with previously reported 20- and 25-Gb/s receivers. For fair comparison, we use the following figure of merit (FOM) given in [11]:

$$FOM = \frac{Transimpedance\ gain \times Bandwidth}{Power\ dissipation}[GHz\Omega / mW] \quad (6)$$

The FOM includes gain-bandwidth product, power dissipation. Our receiver has the highest FOM of 2850 GHzΩ/mW. This is because our receiver does not use any inductors for compensating the parasitic inductance between PD and receiver circuit and the parasitic inductance is used for enhancing the receiver bandwidth.

V. Conclusion

A 20-Gb/s optical receiver circuit is realized in 65-nm CMOS technology. Bonding-wire inductance and pad capacitance are considered in our design so that the optimum receiver circuit can be achieved. The receiver circuit can successfully detect 20-Gb/s $2^{31}-1$ PRBS data with BER less than 10^{-12} measured with a PD equivalent circuit.

ACKNOWLEDGMENTS

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REFERENCES

[1] J.–S. Youn, M.–J. Lee, K.–Y. Park, and W.–Y. Choi, "10-Gb/s 850-nm CMOS OEIC receiver with a silicon avalanche photodetector," *IEEE J. Quantum Electron*., vol. 48, no. 2, pp. 229-236, Feb. 2012.

[2] Y. Dong, and K. W. Martin, "A high-speed fully-integrated POF receiver with large-area photo detectors in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2080-2092, Sep. 2012.

[3] S. J. Koester, C. L. Schow, G. Dehlingher, J. D. Schaub, F. E. Doany, R. A. John, "Ge-on-SOI-detector/Si-CMOS-amplifier receivers for high-perfomance optical-communication applications," *J. Lightw. Technol*., vol. 25, no. 1, pp. 46-57, Jan. 2007.

[4] J. Han, B. Choi, M. Seo, J. Yun, D. Lee, T. Kim, Y. Eo, and S. M. Park, "A 20-Gb/s transformer-based current-mode optical receiver in 0.13-μm CMOS," *IEEE Trans. Circuits Syst. II*, vol. 57, no. 5, pp. 348-352, May 2010.

[5] J. Lu, H. Jia, X. Wang, K. Padmanabhan, W. G. Hurley, and Z. J. Shen, "Modeling, design, and characterization of multiturn bondwire inductors with ferrite epoxy glob cores for power supply system-on-chip or system-in-package applications," *IEEE Trans. Power Electron*., vol. 25, no. 8, pp. 2010-2017, Aug. 2010.

[6] A. S. Sedra, K. C. Smith, Microelectronic circuits, 4th ed. New York: Oxford, ch. 11, 1998.

[7] C. Kromer, G. Sialm, T. Morf, M. L. Schmatz, F. Ellinger, D. Erni, and H. Jäckel, "A low-power 20-GHz 52-dBΩ transimpedance amplifier in 80-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 885-894, Jun. 2004.

[8] J.–D. Jin and S. S. H. Hsu, "A 40 Gb/s transimpedance amplifier in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1449-1457, Jun. 2008.

[9] J.–S. Youn, M.–J. Lee, K.–Y. Park, H. Rücker, and W.–Y. Choi, "SNR characteristics of 850-nm OEIC receiver with a silicon avalanche photodetector," *Opt. Express*, vol. 22, no. 1, pp. 900-907, Jan. 2014.

[10] W.–Z. Chen, Y.–L. Cheng, and D.–S. Lin, "A 1.8-V 10-Gb/s fully integrated CMOS optical receiver analog front-end," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 548-552, Jun. 2005.

[11] T. Takemoto, F. Yuki, H. Yamashita, Y. Lee, T. Saito, S. Tsuji, and S. Nishimura, "A compact 4 x 25-Gb/s 2.0 mW/Gb/s CMOS-based optical receiver for board-to-board interconnects," *IEEE J. Lightwave Tech*., vol. 28, no.23, pp. 3343-3350, Dec. 2010.

[12] T. Takemoto, H. Yamashita, T. Yazaki, N. Chunjo, Y. Lee, and Y. Matsuoka, "A 4 x 25-to-28Gb/s 4.9mW/Gb/s -9.7dBm high sensitivity optical receiver based on 65nm CMOS for board-to-board interconnects," *in Proceedings of IEEE International Solid-State Circuits Conference*, pp. 118-120, 2013.

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