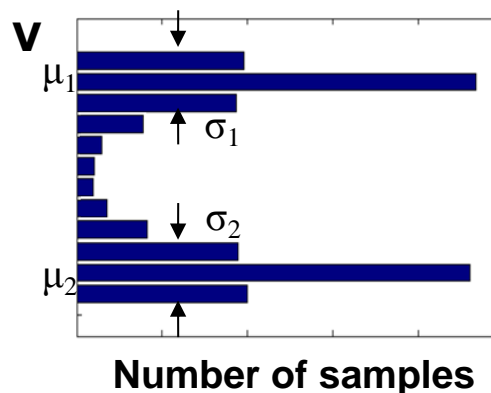
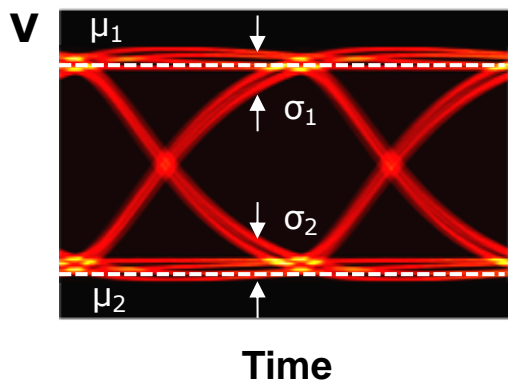
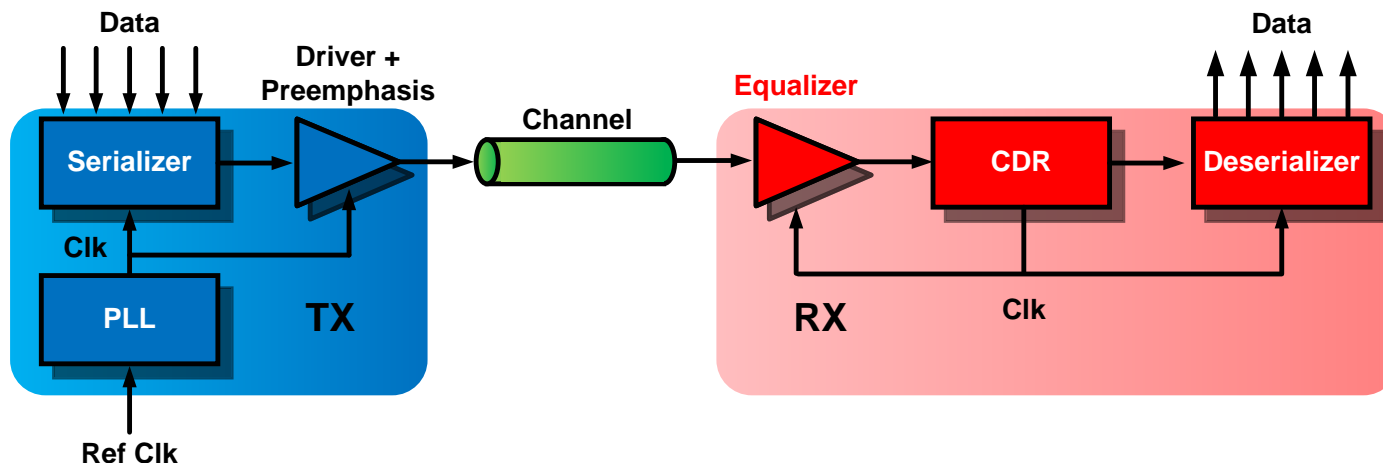


Asynchronous Under-Sampling Histogram

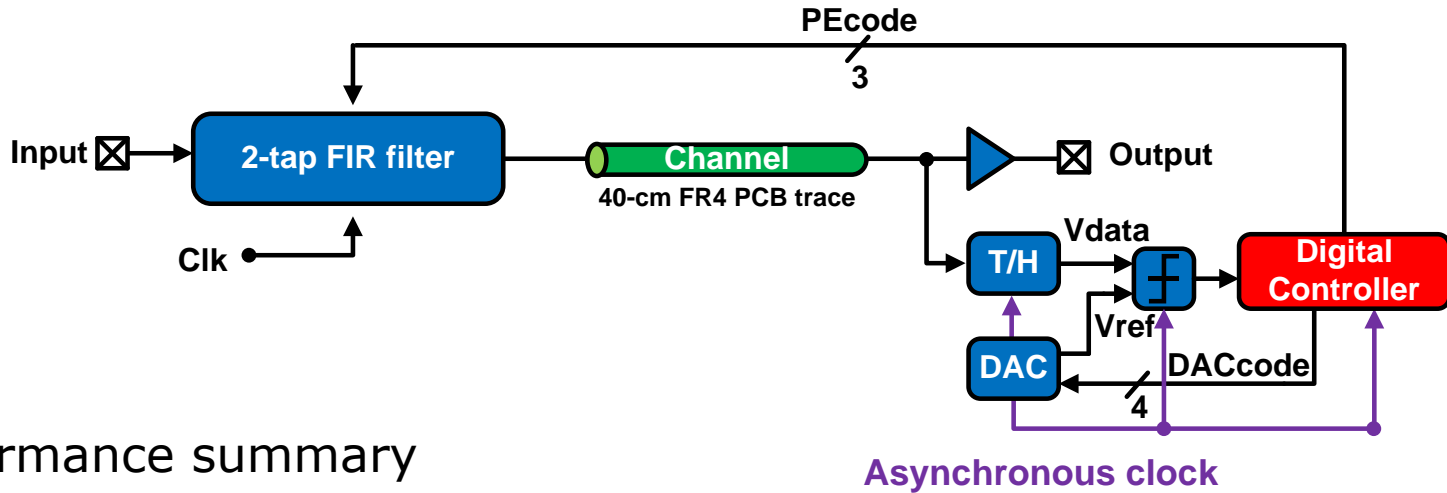
- Adaptive Equalizer using histogram algorithm
 - Signal amplitude distribution with asynchronous sampling
 - Signal quality monitoring by histogram information



$$Q = \frac{\mu_1 - \mu_2}{\sigma_1 + \sigma_2}$$

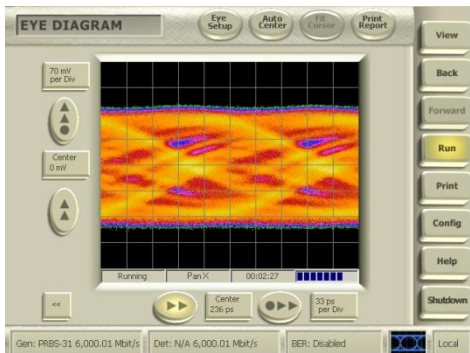
$$BER = erfc(Q)$$

6-Gb/s Adaptive 2-tap Pre-emphasis

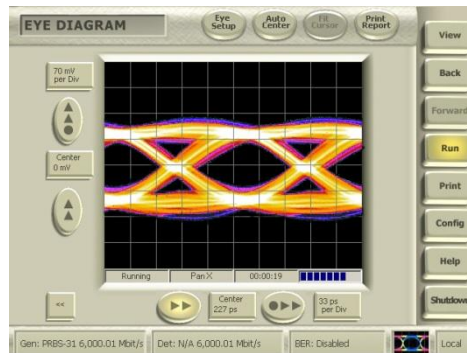


- Performance summary

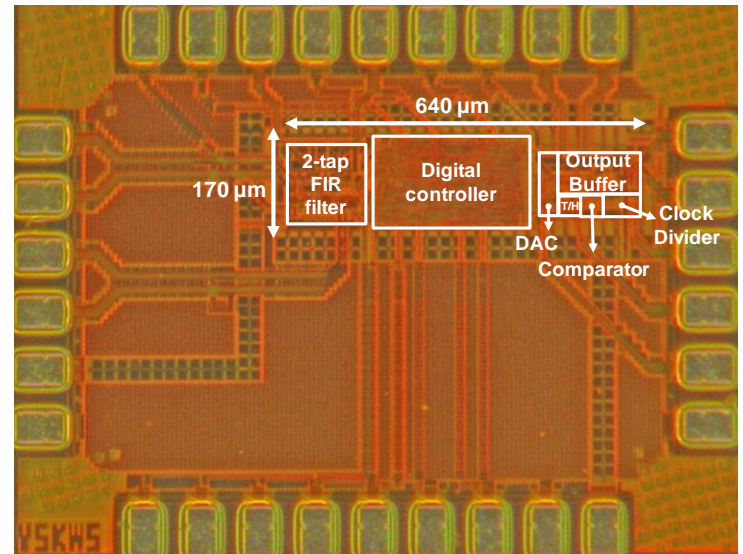
- Samsung 90-nm standard CMOS process
- 6-Gb/s PRBS $2^{31}-1$ data transmission for 40-cm PCB trace
- Less than 10^{-13} BER & 59.4-ps peak to peak Jitter
- 64.5-mW power consumption and 0.077-mm² area



Without PE

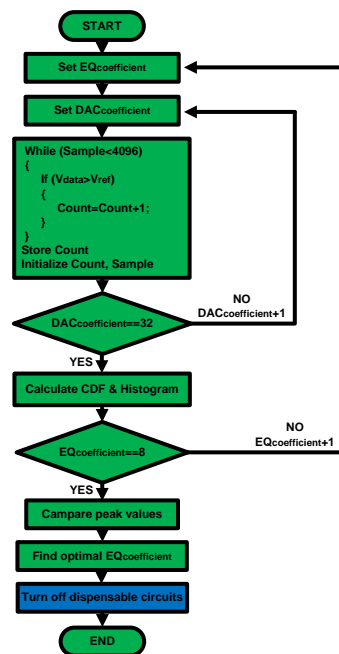
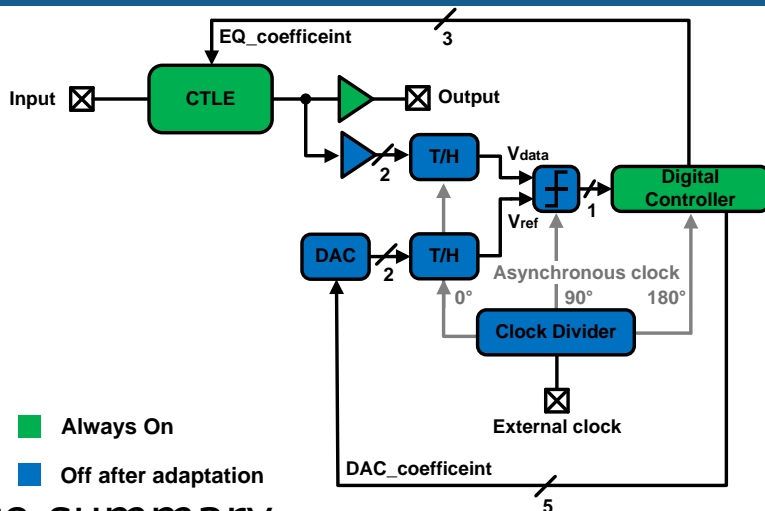


With PE



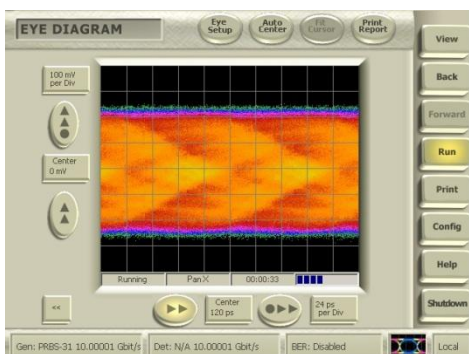
Chip photography

10-Gb/s Low-Power Adaptive Equalizer

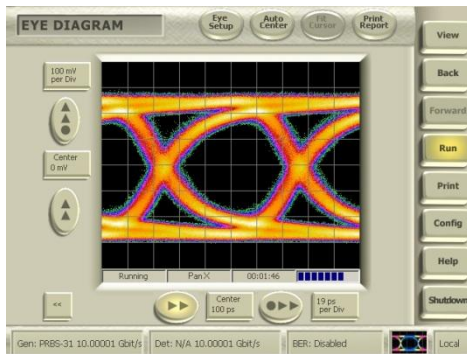


Performance summary

- Samsung 65-nm standard CMOS process
- 10-Gb/s PRBS $2^{31}-1$ data transmission for 40-cm PCB trace
- 4.66-mW during adaptation and 2.49-mW after adaptation
- Less than 10^{-13} BER & 26.6-ps peak to peak Jitter

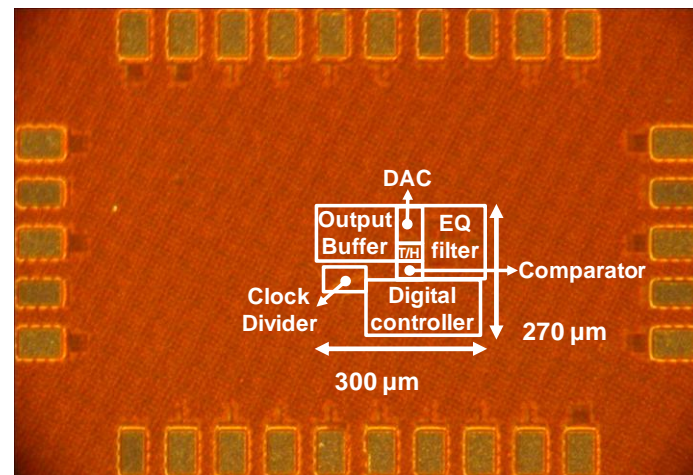


Without EQ



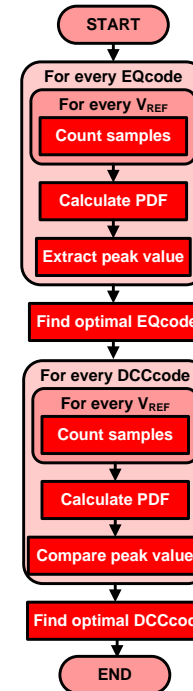
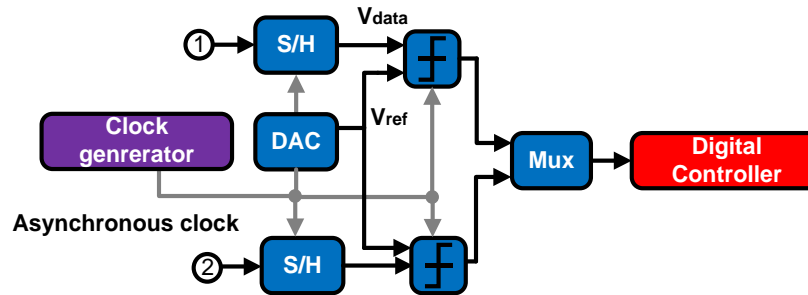
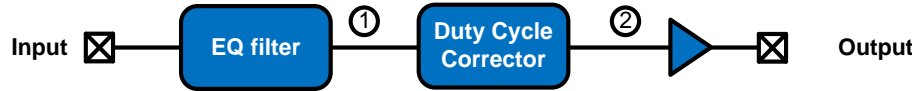
With EQ

3



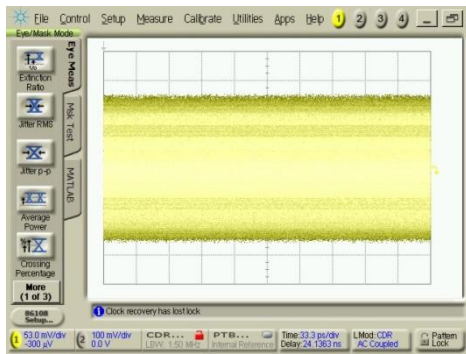
Chip photography

Adaptive Equalizer & Duty Cycle Corrector

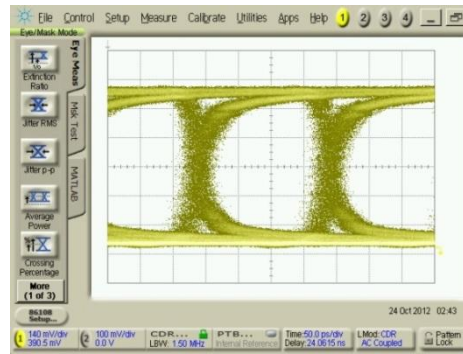


- Performance summary

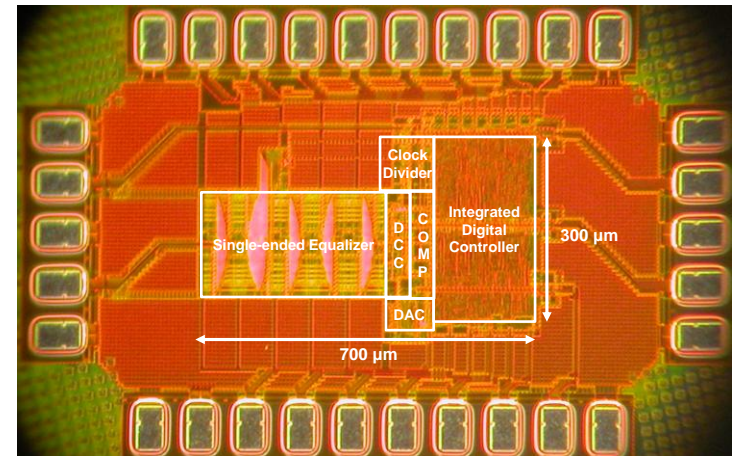
- Samsung 130-nm standard CMOS process (1P6M)
- 5-Gb/s PRBS 2³¹-1 data transmission for 80cm PCB trace
- Less than 10⁻¹³ BER & 56.67-ps peak to peak Jitter
- 25-mW power consumption and 0.21-mm² chip area



Without EQ



With EQ



Chip photography