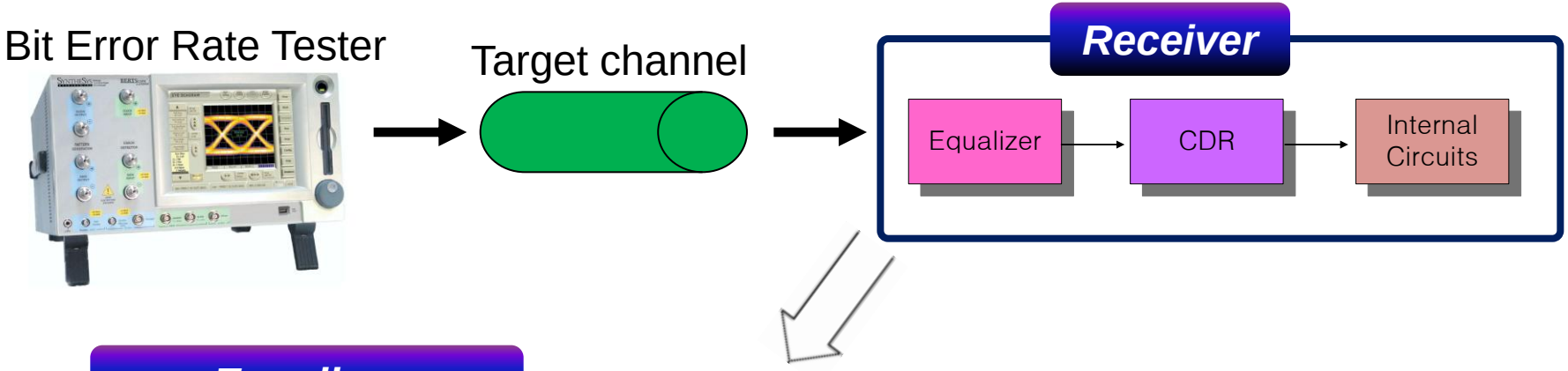
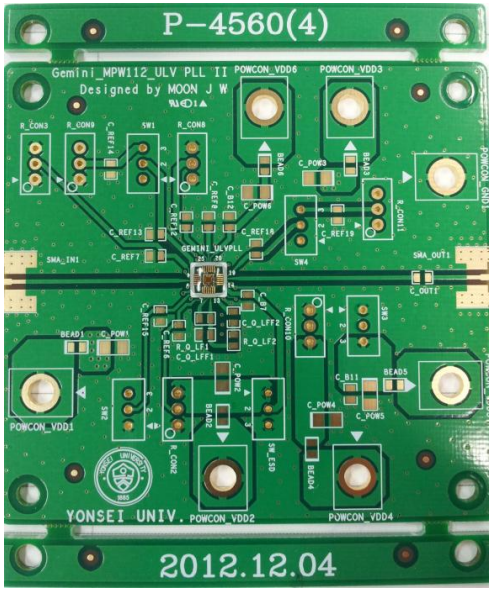
Low-Power Adaptive Passive Equalizer



An 8-Gb/s Inductorless daptive passive equalizer in 0.18–um CMOS technology

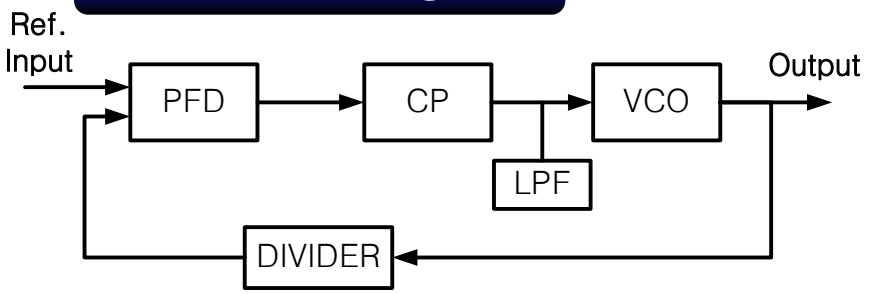
- Self power-comparison method for the adaptation block.
- Power effciency = 0.84 mW/Gbps
- Total area = 0.84 mm^2

Ultra-Low Voltage Phase-Locked Loops



First ULV PLL

PLL Block diagram



0.4V Ultra-low voltage PLL

- Samsung 65nm CMOS technology
- Two versions are fabricated
  - Self-regulated Active Loop Filter PLL
  - & ALF PLL w/ Automatic Frequency Control

ULV Challenges

- Low voltage headroom (multiple-stacks are not allowed)
- Process, Voltage, and Temperature (PVT) variation immunity
- Vulnerable to power noise