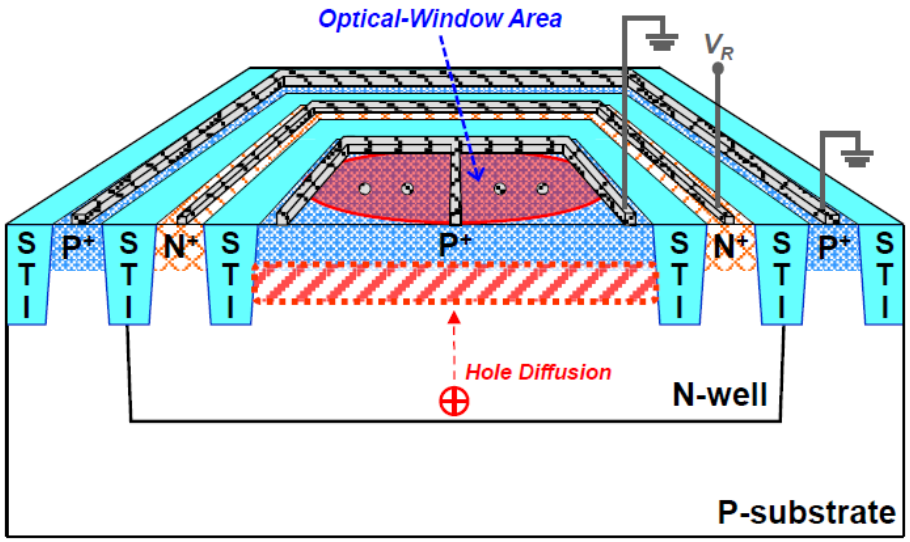
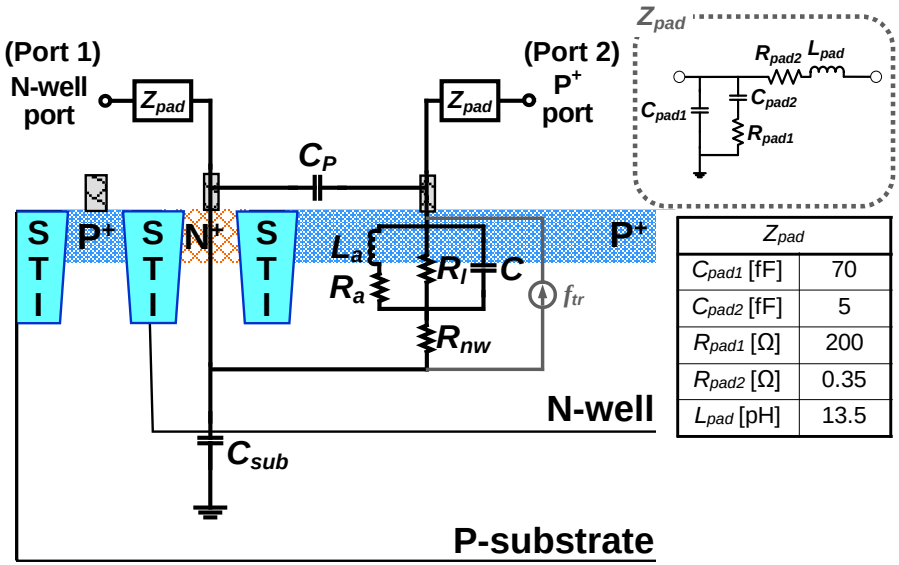
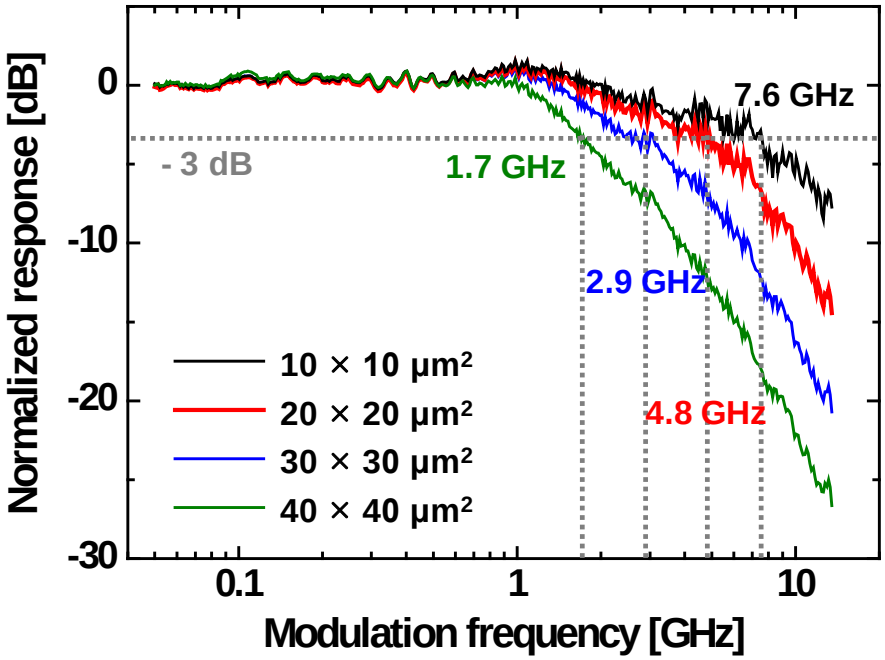
CMOS-Compatible Avalanche Photodetector





Z_{pad}	
C_{pad1} [fF]	70
C_{pad2} [fF]	5
R_{pad1} [Ω]	200
R_{pad2} [Ω]	0.35
L_{pad} [pH]	13.5

(to be published in IEEE Transactions on Electron Devices, 2013)



- **CMOS-APDs having 10 × 10-μm² device area**
  ➔ Photodetection bandwidth increased to 7.6 GHz

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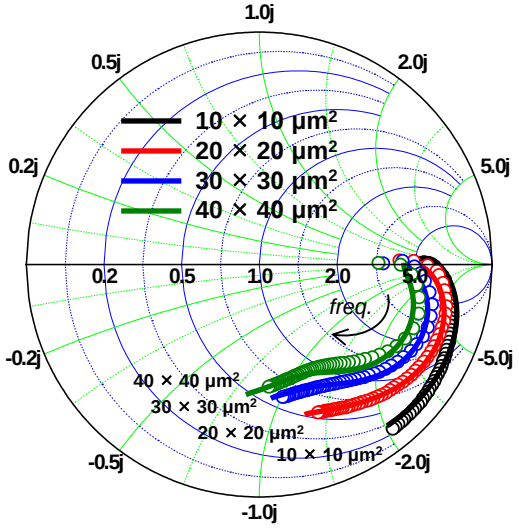

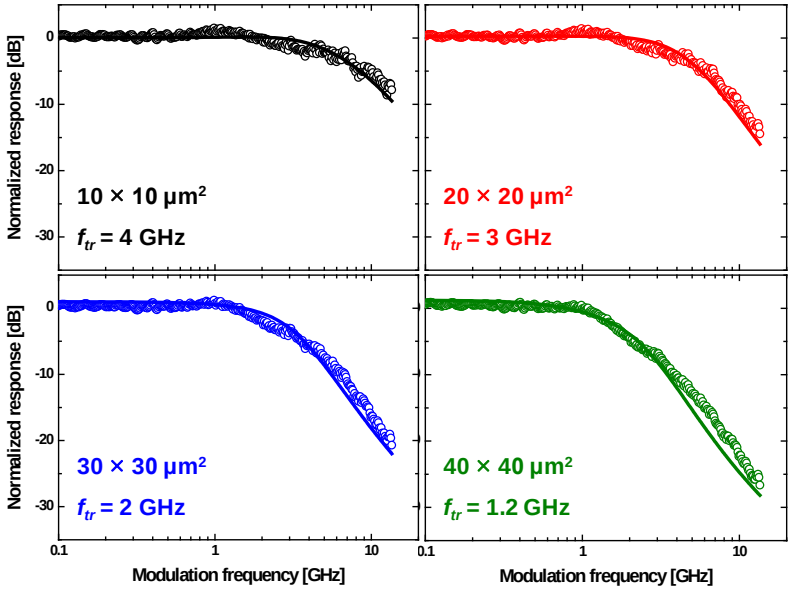

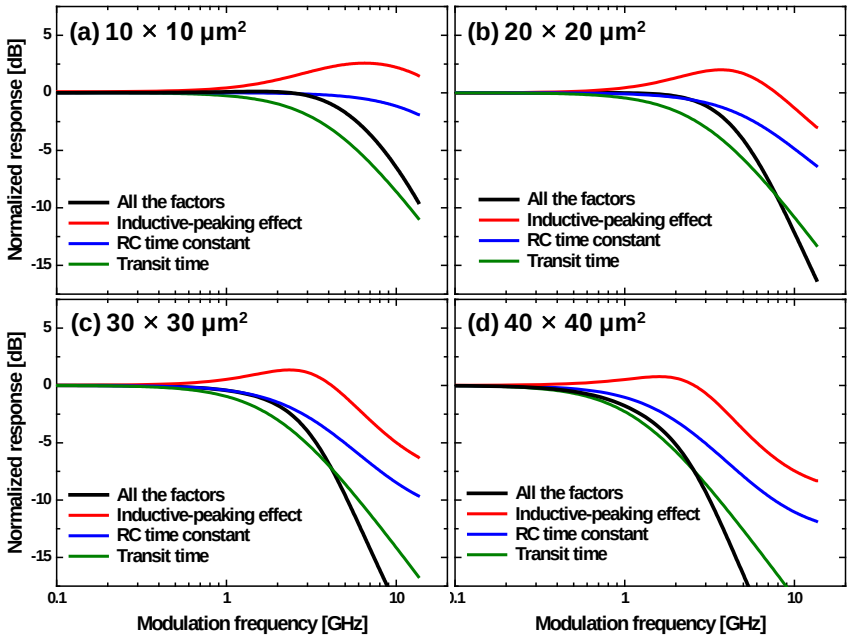

	Other Work	Other Work	Other Work		This work
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS
Structure	Multiple p⁺-p-n APD	P⁺/P⁻/N⁺ lateral PIN	Strip SMPD*	Meshed SMPD*	P⁺/N-well APD
R	0.74 A/W	0.073 A/W	0.057 A/W	0.029 A/W	**0.48 A/W**
BW	1.6 GHz	1.9 GHz	1.8 GHz	6.9 GHz	**7.6 GHz**
C_{PD}	345 fF	1600 fF	213 fF	206 fF	35 fF
A	50 × 50 μm² (Square)	50 × 50 μm² (Square)	55 × 55 μm² (Octagon)	55 × 55 μm² (Octagon)	10 × 10 μm² (Square)
V_R	14.3 V	6 V	14.2 V	14.2 V	10.25 V

*SMPD: spatially modulated photodetector
R: responsivity, *BW*: bandwidth, C_{PD}: intrinsic photodetector capacitance, *A*: optical-window area, V_R: reverse bias voltage

➔ ***World record among silicon PDs in standard CMOS technology***